

SWITCHING  
N-CHANNEL POWER MOS FET

## DESCRIPTION

The 2SK3740 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, designed for high voltage applications such as lamp drive, DC/DC converter, and actuator driver.

## FEATURES

- Gate voltage rating:  $\pm 30$  V
- Low on-state resistance  
 $R_{DS(on)} = 160$  m $\Omega$  MAX. ( $V_{GS} = 10$  V,  $I_D = 10$  A)
- Low gate charge  
 $Q_G = 47$  nC TYP. ( $V_{DD} = 200$  V,  $V_{GS} = 10$  V,  $I_D = 20$  A)
- Surface mount package available

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0$ V)	$V_{DSS}$	250	V
Gate to Source Voltage ( $V_{DS} = 0$ V)	$V_{GSS}$	$\pm 30$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 20$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 60$	A
Total Power Dissipation	$P_{T1}$	1.5	W
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T2}$	100	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	20	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	40	mJ

**Notes 1.**  $PW \leq 10$   $\mu\text{s}$ , Duty Cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 125$  V,  $R_G = 25$   $\Omega$ ,  $V_{GS} = 20 \rightarrow 0$  V,  $L = 100$   $\mu\text{H}$

## THERMAL RESISTANCE

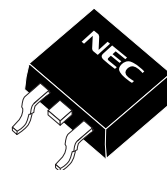
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.25	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

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## ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3740-ZK	TO-263 (MP-25ZK)

(TO-263)

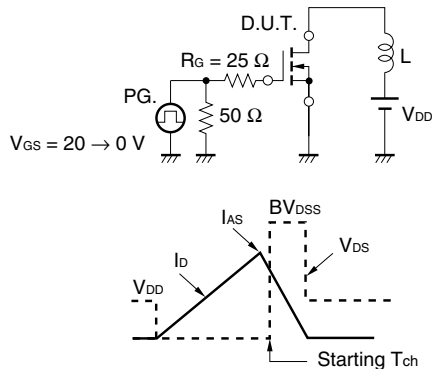


**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

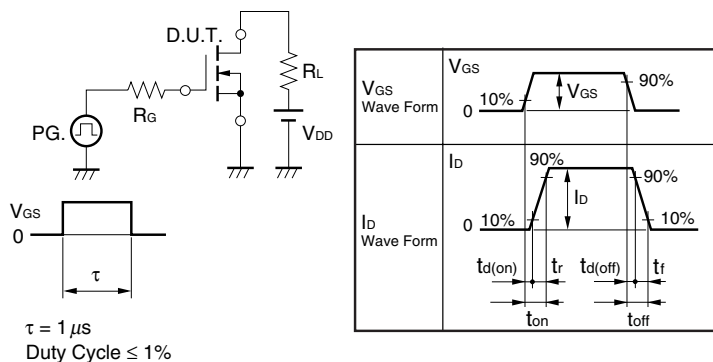
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 250 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 mA	2.5	3.5	4.5	V
Forward Transfer Admittance <b>Note</b>	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A	7.0	15		S
Drain to Source On-state Resistance <b>Note</b>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.12	0.16	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		1720		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		330		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1.0 MHz		170		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 10 A		17		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		17		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		49		ns
Fall Time	t <sub>f</sub>			9		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 200 V		47		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		7		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 20 A		25		nC
Body Diode Forward Voltage <b>Note</b>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		0.91		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		210		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		1.4		μC

**Note** Pulsed

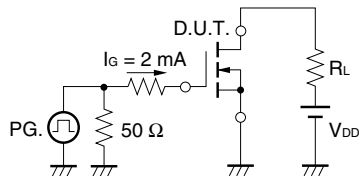
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



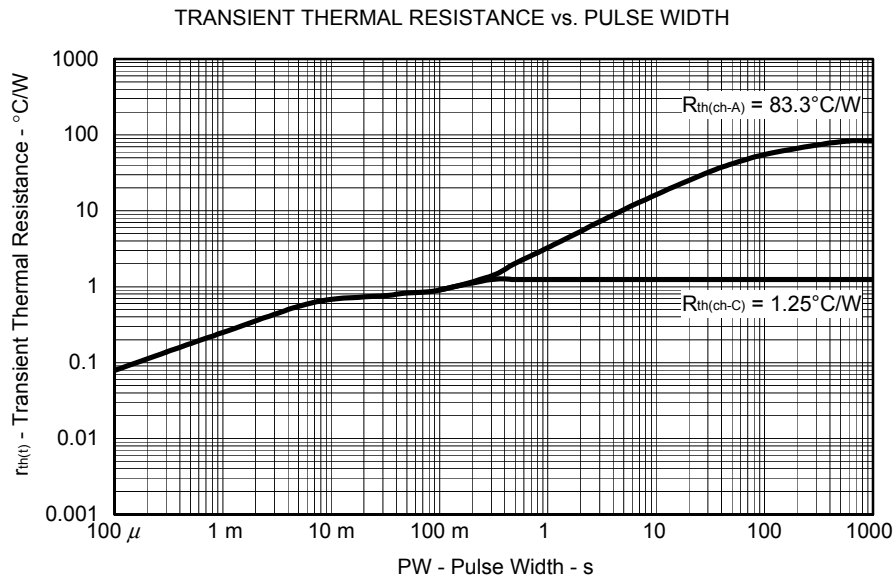
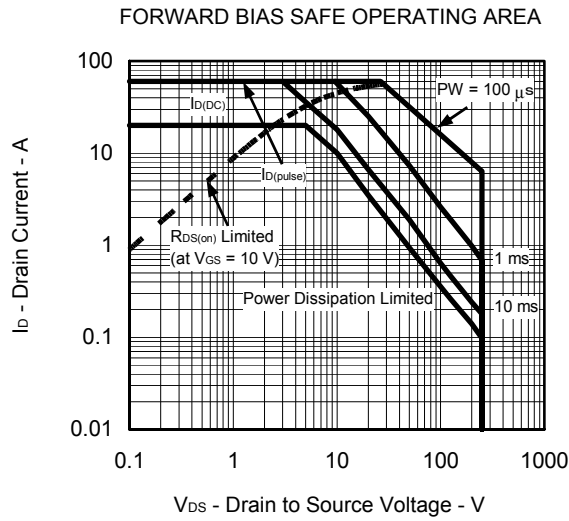
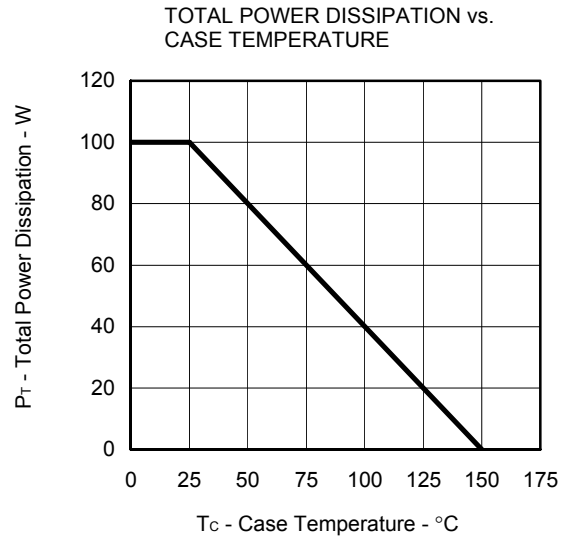
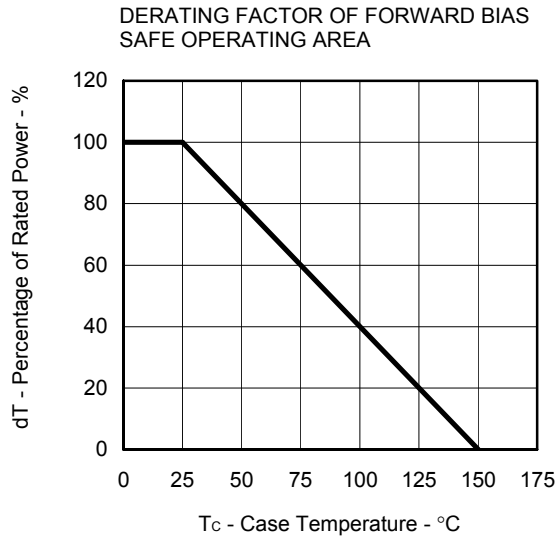
**TEST CIRCUIT 2 SWITCHING TIME**



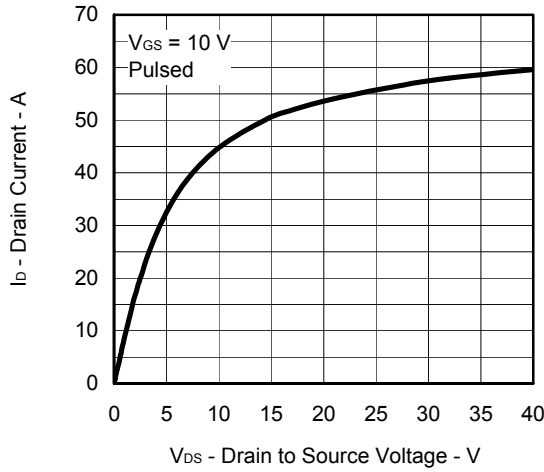
**TEST CIRCUIT 3 GATE CHARGE**



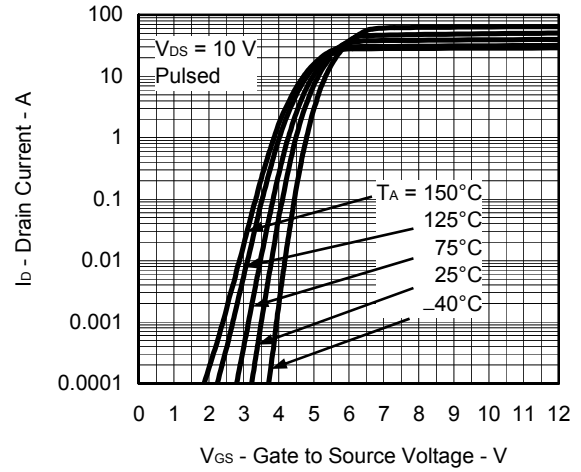
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)



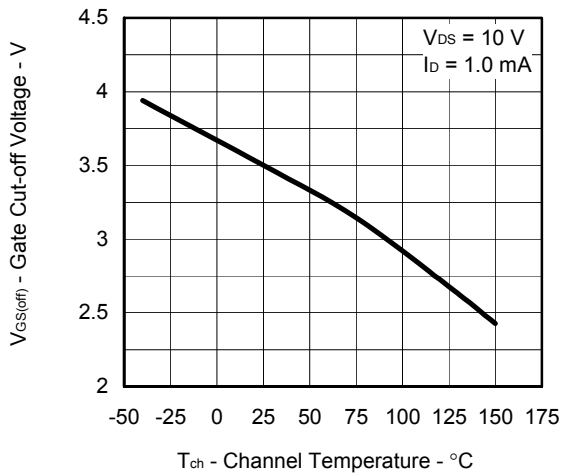
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



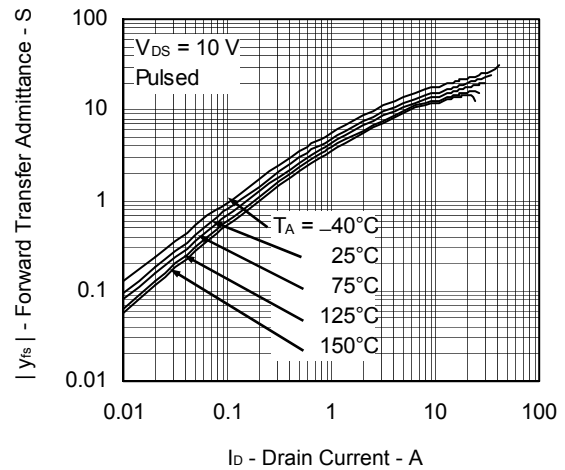
FORWARD TRANSFER CHARACTERISTICS



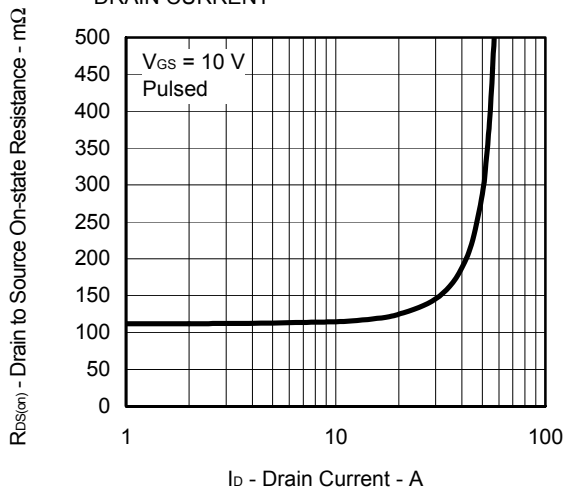
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



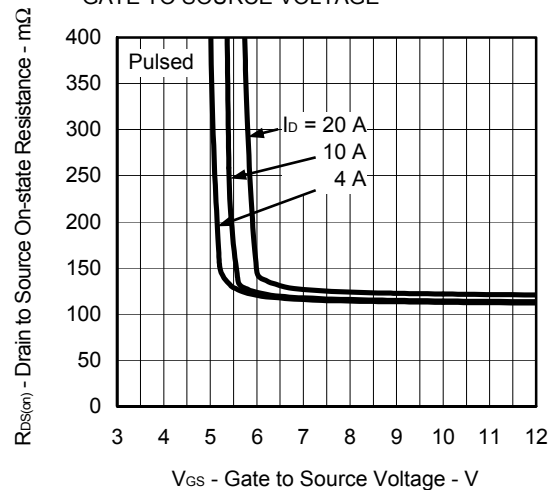
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



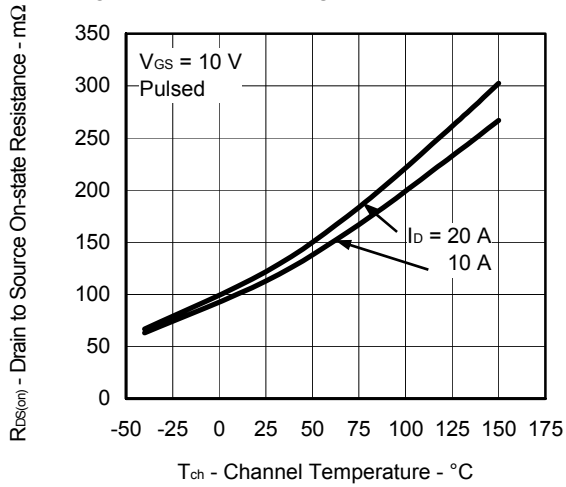
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



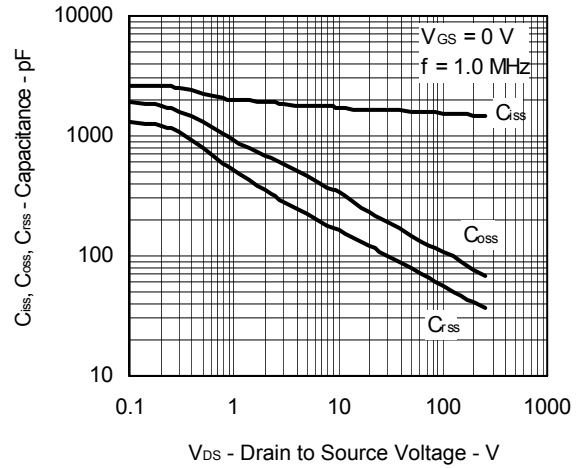
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



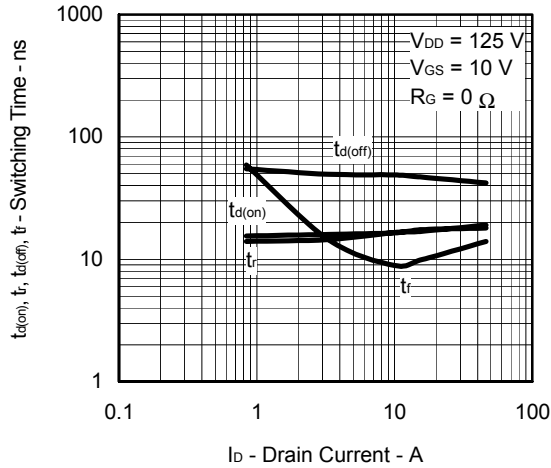
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



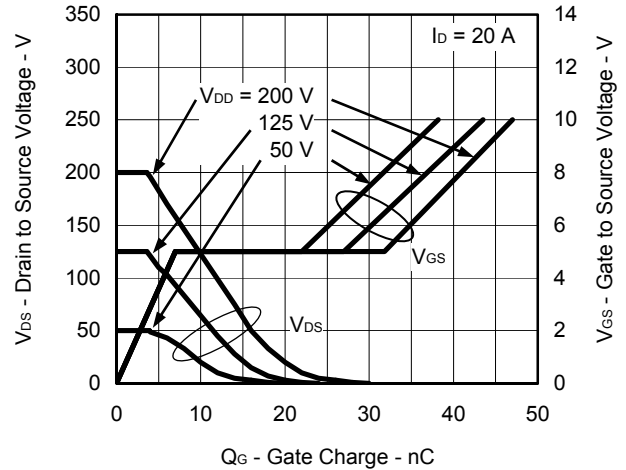
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



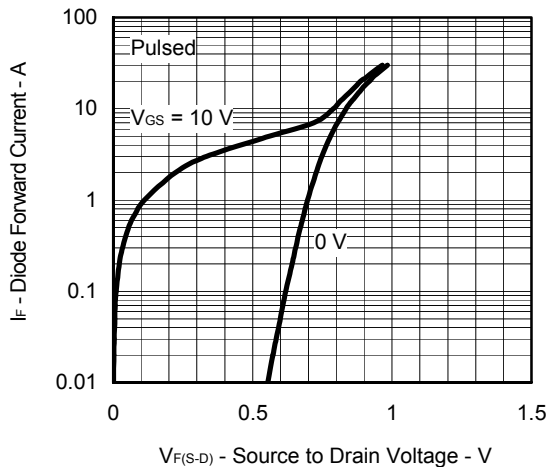
SWITCHING CHARACTERISTICS



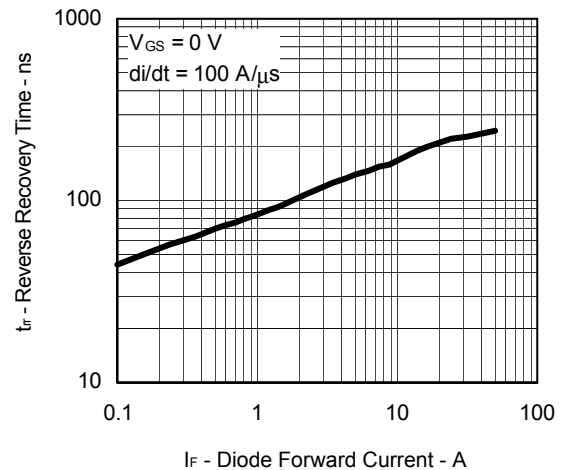
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



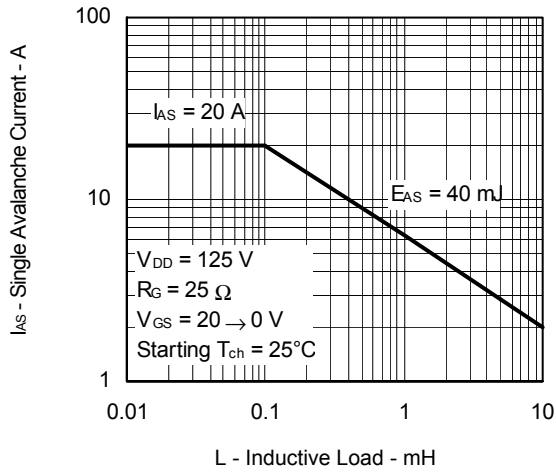
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



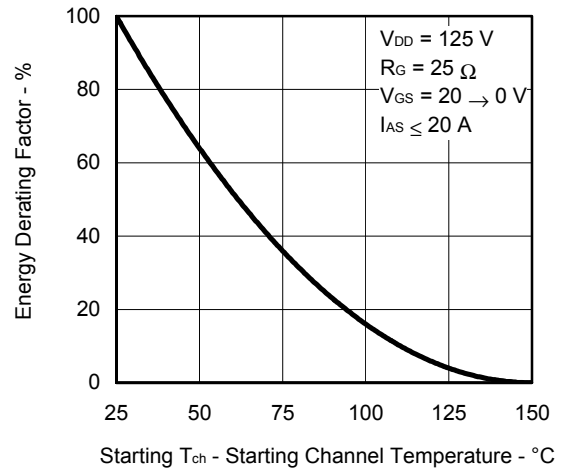
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

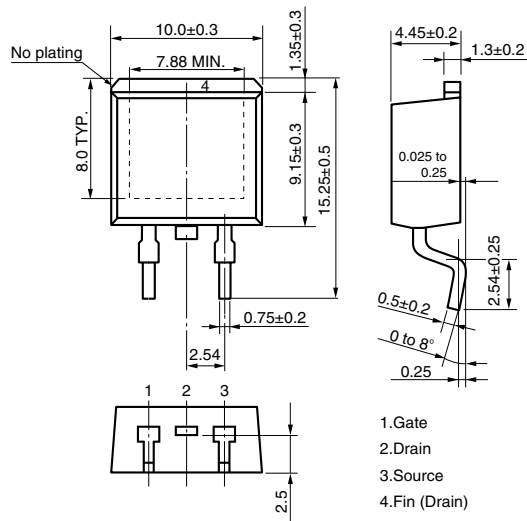


SINGLE AVALANCHE ENERGY DERATING FACTOR

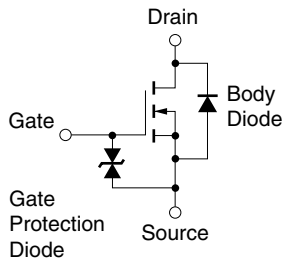


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD.  
 When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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