DATA SHEET

MOS FIELD EFFECT TRANSISTOR
2SK3668

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3668 is N-channel DMOS FET device that features a low on-state resistance, low charge and excellent switching characteristics, designed for high voltage applications such as high intensity discharge lamp drive.

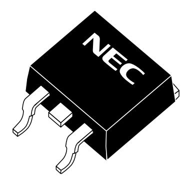
FEATURES

- Low gate charge
  Q_G = 26 nC TYP. (V_{DD} = 320 V, V_{GS} = 10 V, I_D = 10 A)
- Gate voltage rating: ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 0.55 Ω MAX. (V_{GS} = 10 V, I_D = 5.0 A)
- Surface mount package available

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3668-ZK	TO-263 (MP-25ZK)

(TO-263)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

	Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	400	V
	Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
	Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±10	A
	Drain Current (pulse) Note1	$I_{D(pulse)}$	±34	A
	Total Power Dissipation (T_A = 25°C)	P_{T1}	1.5	W
	Total Power Dissipation (T_C = 25°C)	P_{T2}	100	W
	Channel Temperature	T_{ch}	150	°C
	Storage Temperature	T_{stg}	–55 to +150	°C
	Single Avalanche Current Note2	I_{AS}	10	A
★	Single Avalanche Energy Note2	E_{AS}	8	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

★ **2.** Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.25	°C/W
Channel to Ambient Thermal Resistane	$R_{th(ch-A)}$	83.3	°C/W

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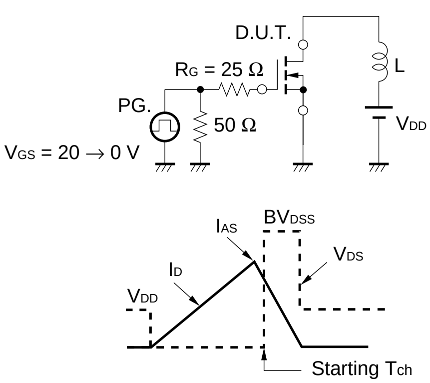
The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

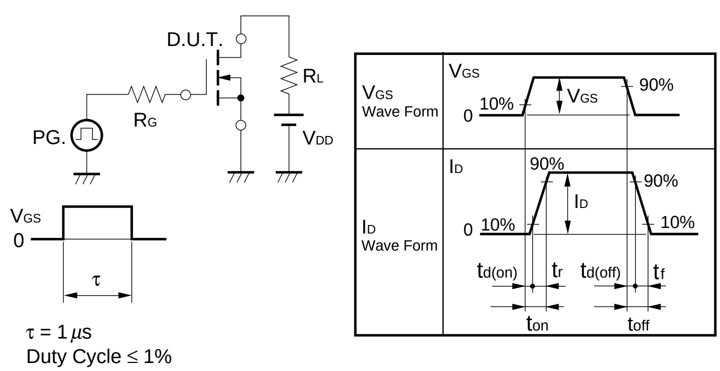
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1.0 mA	2.5		3.5	V
★ Forward Transfer Admittance Note	$\lvert y_{fs} \rvert$	V_{DS} = 10 V, I_D = 5.0 A	3.0	5.6		S
★ Drain to Source On-state Resistance Note	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5.0 A		0.40	0.55	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V		1320		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		230		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		13		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 150 V, I_D = 5.0 A		18		ns
Rise Time	t_r	V_{GS} = 10 V		8		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		44		ns
Fall Time	t_f			4		ns
Total Gate Charge	Q_G	V_{DD} = 320 V		26		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		7		nC
Gate to Drain Charge	Q_{GD}	I_D = 10 A		11		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 10 A, V_{GS} = 0 V		0.90		V
Reverse Recovery Time	t_{rr}	I_F = 10 A, V_{GS} = 0 V		350		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		2.7		μC

Note Pulsed: PW ≤ 800 μs, Duty Cycle ≤ 2%

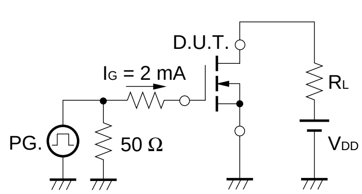
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

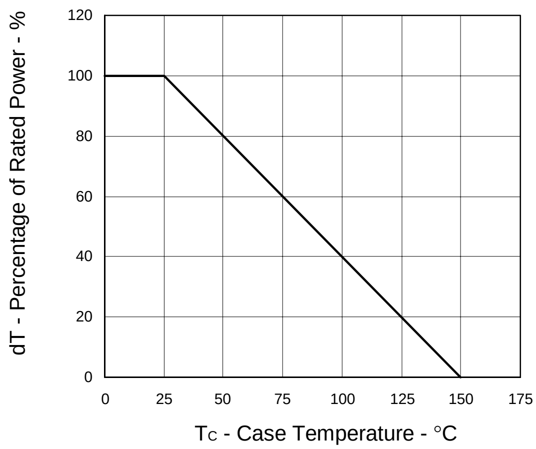


TEST CIRCUIT 3 GATE CHARGE

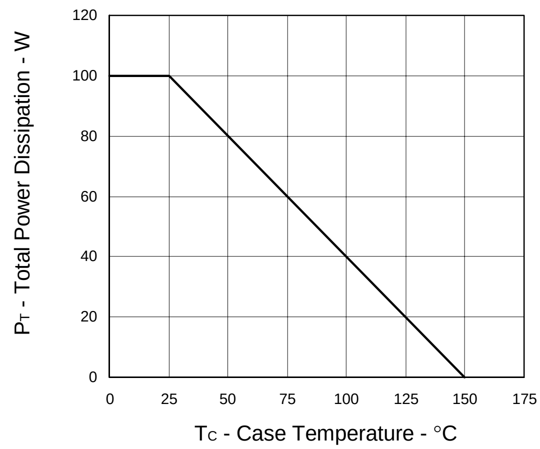


TYPICAL CHARACTERISTICS (T_A = 25°C)

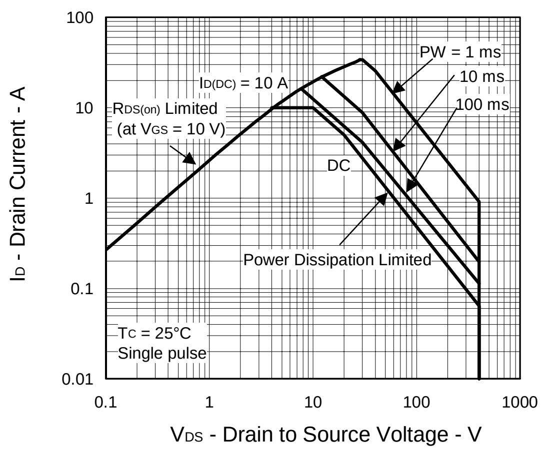
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



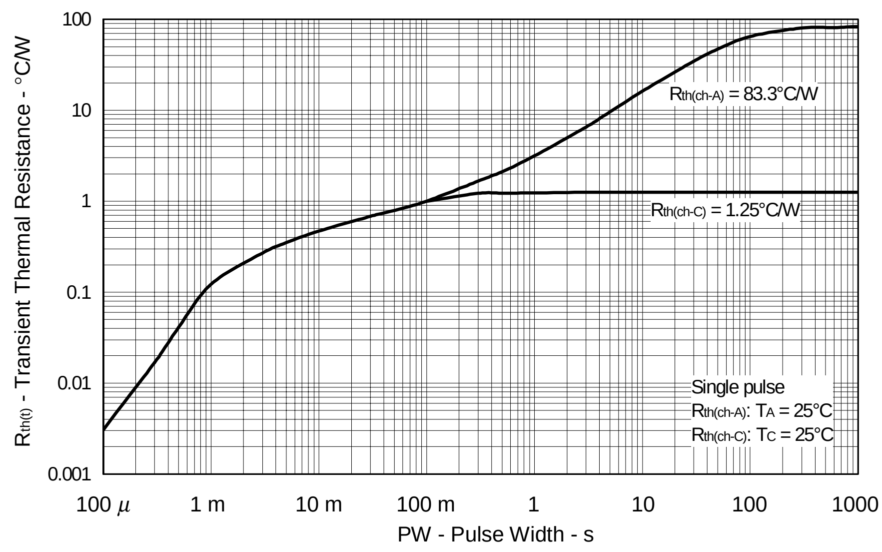
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



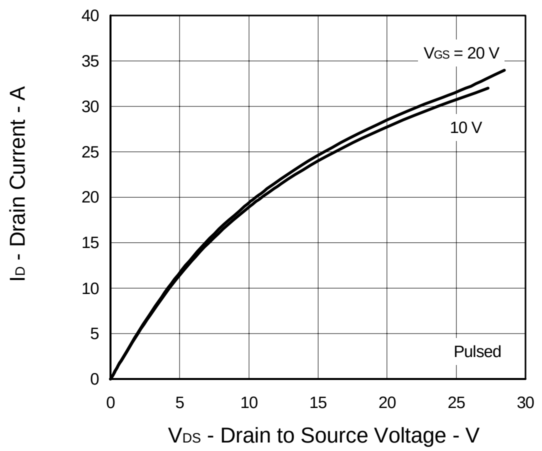
★ FORWARD BIAS SAFE OPERATING AREA



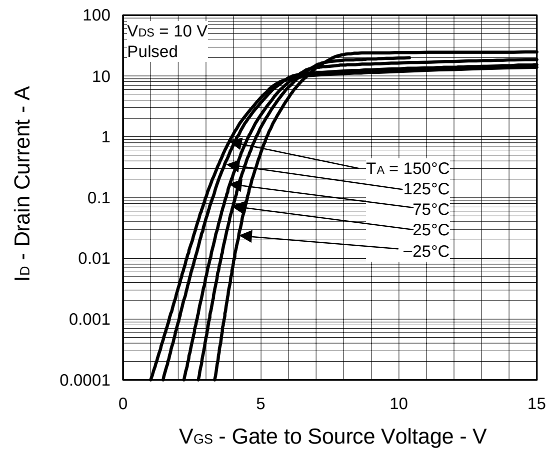
★ TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



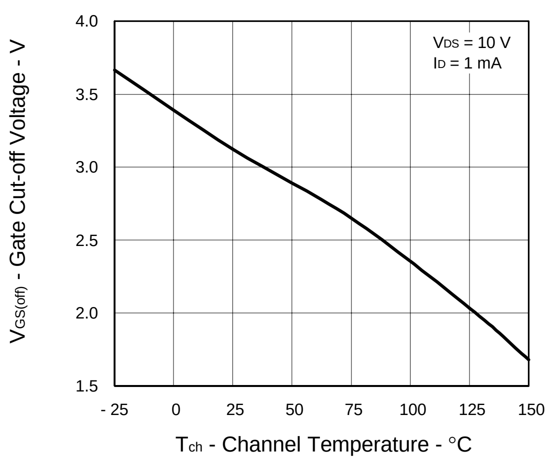
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



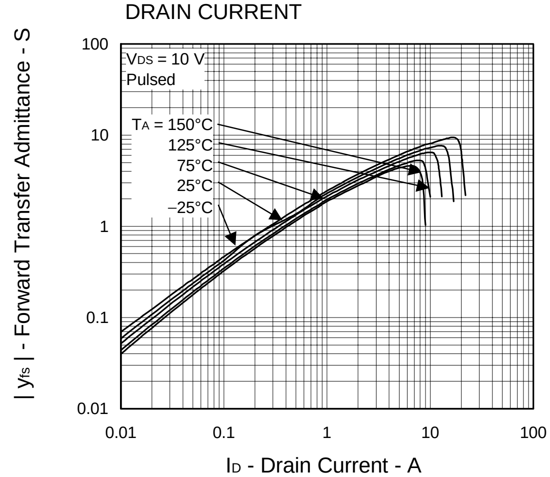
FORWARD TRANSFER CHARACTERISTICS



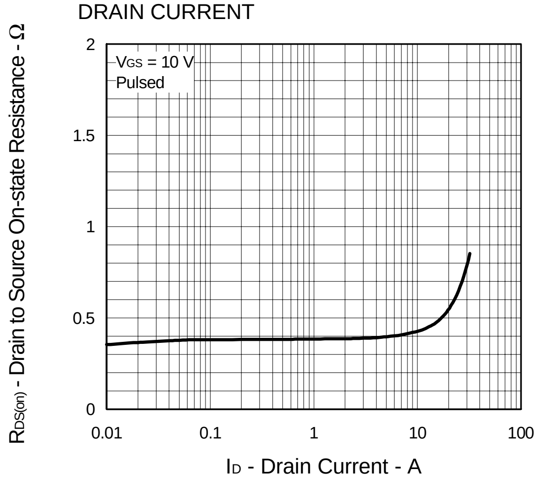
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



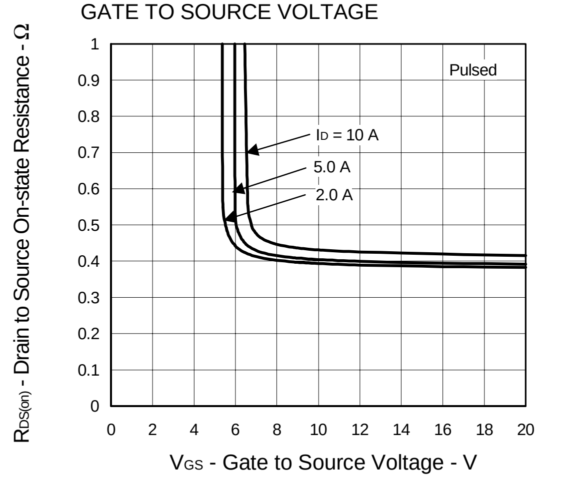
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



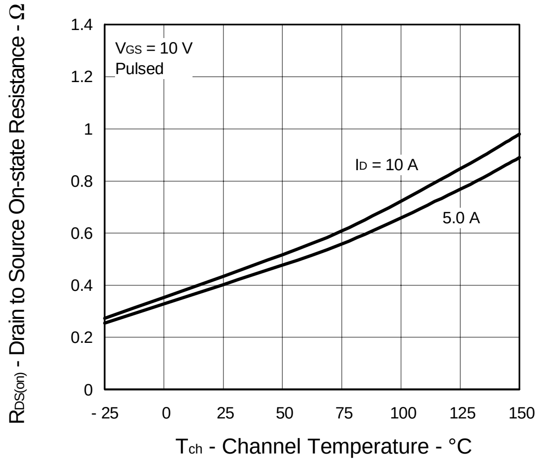
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



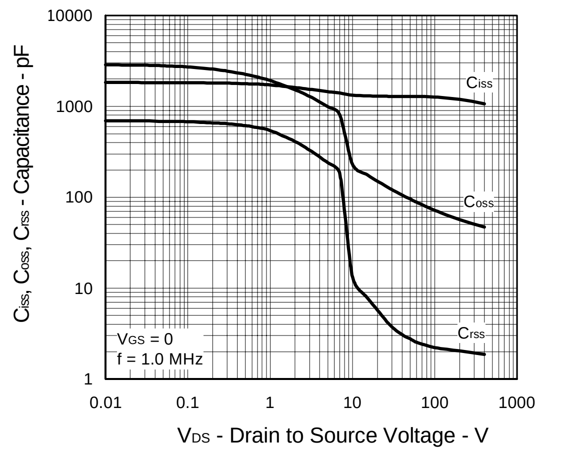
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



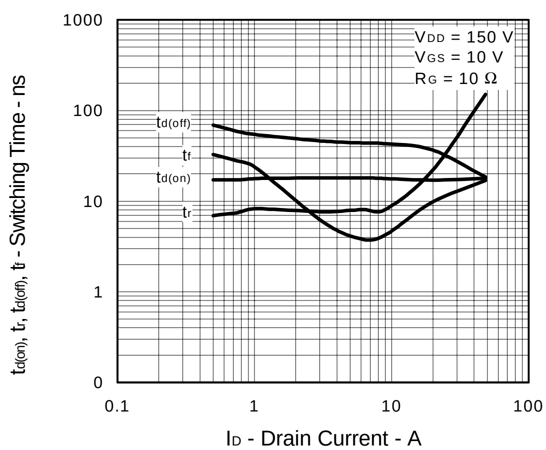
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



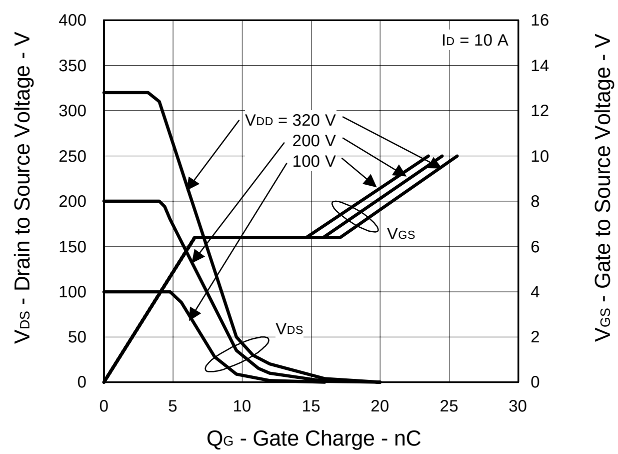
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



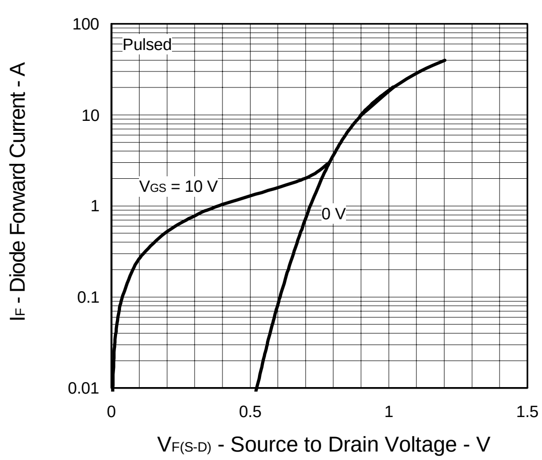
SWITCHING CHARACTERISTICS



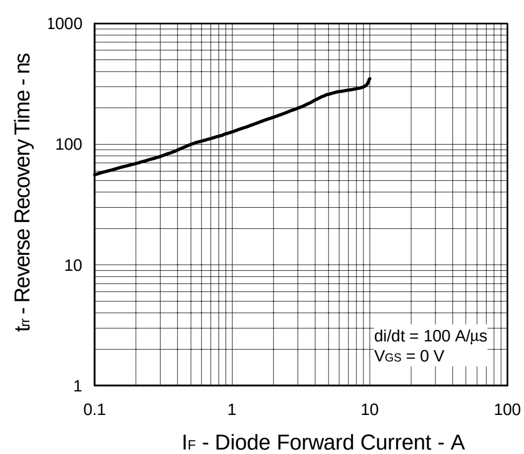
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



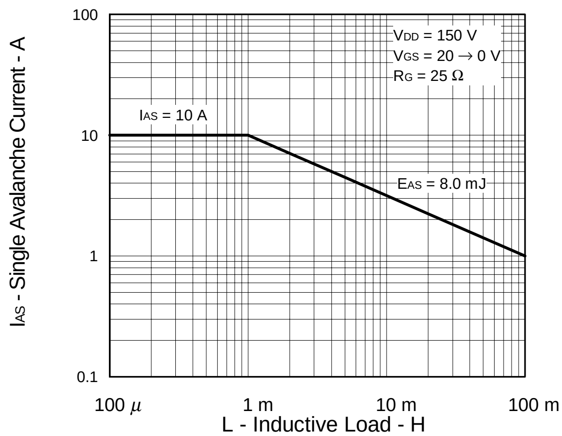
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



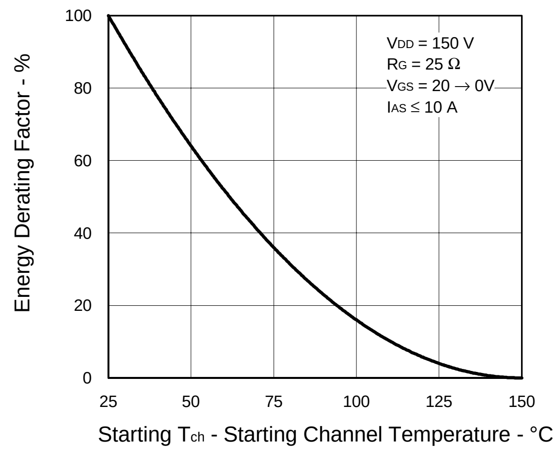
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



★ SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

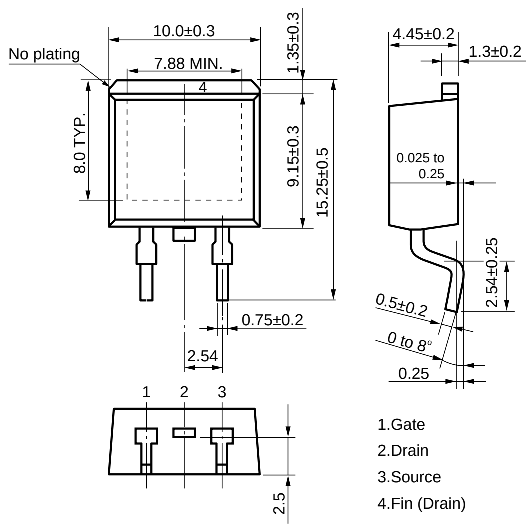


SINGLE AVALANCHE ENERGY DERATING FACTOR

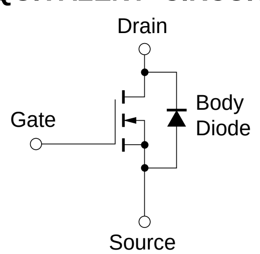


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.