

3875081 G E SOLID STATE
Triacs

01E 17747 D F-25-17

2N5441-2N5446, T6420 Series

File Number **593**

40-A Silicon Triacs

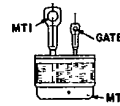
Features:

- *di/dt* capability = 100 A/ μ s
- Low switching losses
- Low on-state voltage at high current levels
- Low thermal resistance

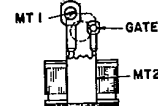
Package \ Voltage	200 V Types	400 V Types	600 V Types
Press-Fit	2N5441	2N5442	2N5443
Stud	2N5444	2N5445	2N5446
Isolated-Stud	T6420B	T6420D	T6420M

RCA triacs are gate-controlled, full-wave silicon ac switches. They are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative gate-triggering voltages.

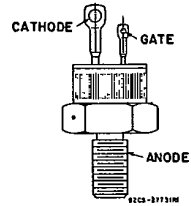
TERMINAL DESIGNATIONS



2N5441-43



T6420 Series



2N5444-46

MAXIMUM RATINGS, Absolute-Maximum Values:

For Operation with Sinusoidal Supply Voltage at Frequencies up to 50/60 Hz and with resistive or Inductive Load

	2N5441 2N5444 T6420B	2N5442 2N5445 T6420D	2N5443 2N5446 T6420M	
* REPETITIVE PEAK OFF-STATE VOLTAGE Δ , V_{DORM} Gate Open, $T_J = -65$ to 100°C	200	400	600	V
RMS ON-STATE CURRENT (Conduction angle = 360°C), $I_{T(RMS)}$ Case temperature				
$T_C = 70^\circ\text{C}$ (Press-fit types)		40		A
$T_C = 65^\circ\text{C}$ (Stud types)		40		A
$T_C = 60^\circ\text{C}$ (Isolated-stud types)		40		A
For other conditions		See Fig. 3		
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT, I_{TSM} For one cycle of applied principal voltage				
60 Hz (sinusoidal)		300		A
50 Hz (sinusoidal)		265		A
For more than one cycle of applied principal voltage		See Fig. 4		
RATE OF CHANGE OF ON-STATE CURRENT, di/dt $V_{DM} = V_{DORM}$, $I_{GT} = 200$ mA, $t_r = 0.1$ μ s (See Fig. 12)		100		A/ μ s
FUSING CURRENT (for Triac Protection), I^2t $T_J = -65$ to 110°C , $t = 1.25$ to 10 ms		450		A ² s
* PEAK GATE-TRIGGER CURRENT \blacksquare , I_{GT} For 1 μ s max.		12		A
* GATE POWER DISSIPATION Peak (For 10 μ s max., $I_{GT} \leq 4$ A, P_{GM}		40		W
Average, $P_{G(AV)}$		0.75		W
* TEMPERATURE RANGE Δ Storage, T_{stg}		-65 to 150		$^\circ\text{C}$
Operating (Case), T_C		-65 to 110		$^\circ\text{C}$
* TERMINAL TEMPERATURE (During Soldering), T_T For 10 s max. (terminals and case)		225		$^\circ\text{C}$
STUD TORQUE, τ_s Recommended		35		in-lb
Maximum (DO NOT EXCEED)		50		in-lb

* In accordance with JEDEC registration data format (JS-14, RDF2) filed for the JEDEC (2N-Series) types.

■ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

■ For either polarity of gate voltage (V_G) with reference to main terminal 1.

Δ For temperature measurement reference point, see Dimensional Outline

2N5441-2N5446, T6420 Series

ELECTRICAL CHARACTERISTICS

At Maximum Ratings Unless Otherwise Specified and at Indicated Case Temperature (T_C)

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		FOR ALL TYPES UNLESS OTHERWISE SPECIFIED			
		MIN.	TYP.	MAX.	
Peak Off-State Current: [♠] Gate open, T _J = 110°C, V _{DROM} = Max. rated value	I _{DROM}	—	0.2	4*	mA
Maximum On-State Voltage: [♠] For I _T = 100 A (peak), T _C = 25°C For I _T = 56 A (peak), T _C = 25°C	V _{TM}	—	1.7 1.5	2 1.85*	V
DC Holding Current: [♠] Gate open, Initial principal current = 500 mA (dc), v _D = 12V: T _C = 25°C T _C = -65°C For other case temperatures	I _{HO}	—	26 —	60 100*	mA
Critical Rate of Rise of Commutation Voltage: [♠] For v _D = V _{DROM} , I _T (RMS) = 40 A, commutating di/dt = 22 A/ms, gate unenergized, (See Fig. 13): T _C = 70°C (Press-fit types) = 65°C (Stud types) = 60°C (Isolated-stud types)	dv/dt	5*	30 30 5	— — —	V/μs
Critical Rate of Rise of Off-State Voltage: [♠] For v _D = V _{DROM} , exponential voltage rise, gate open, T _C = 110°C: 2N5441, 2N5444, T6420B. 2N5442, 2N5445, T6420D. 2N5443, 2N5446, T6420M	dv/dt	50* 30* 20*	200 150 100	— — —	V/μs
DC Gate-Trigger Current: ^{♠♠} Mode V _{MT2} V _G For v _D = 12 V (dc) I ⁺ positive positive R _L = 30 Ω III ⁻ negative negative T _C = 25°C I ⁻ positive negative III ⁺ negative positive	I _{GT}	—	15 20 30 40	50 50 80 80	mA
For v _D = 12 V (dc) Mode V _{MT2} V _G R _L = 30 Ω I ⁺ positive positive T _C = -65°C III ⁻ negative negative I ⁻ positive negative III ⁺ negative positive For other case temperatures		—	— — — —	125* 125* 240* 240*	
DC Gate-Trigger Voltage: ^{♠♠} For v _D = 12 V (dc), R _L = 30 Ω, T _C = 25°C = -65°C For other case temperatures For v _D = V _{DROM} , R _L = 125 Ω, T _C = 110°C	V _{GT}	— — 0.2	1.35 1.8 —	2.5 3.4* —	V
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For v _D = V _{DROM} , I _{GT} = 200 mA, t _r = 0.1 μs, I _T = 60 A (peak), T _C = 25°C (See Figs. 10 & 14)	t _{gt}	—	1.7	3	μs
Thermal Resistance, Junction-to-Case: Steady-State Press-fit types Stud types Isolated-stud types Transient (Press-fit & stud types)	R _{θJC}	— — — —	— — — —	0.8* 0.9* 1	°C/W

* In accordance with JEDEC registration data format (JS-14, RDF 2) filed for the JEDEC (2N-Series) types.
 ♠ For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.
 ♠♠ For either polarity of gate voltage (V_G) with reference to main terminal 1.

2N5441-2N5446, T6420 Series

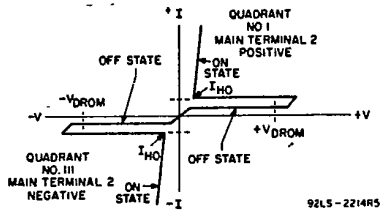


Fig. 1 - Principal voltage-current characteristic.

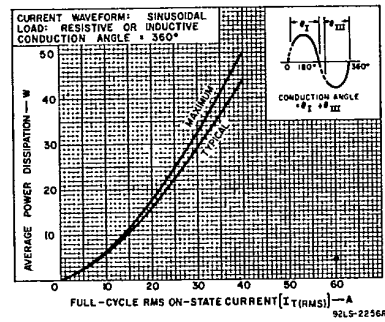


Fig. 2 - Power dissipation vs. on-state current.

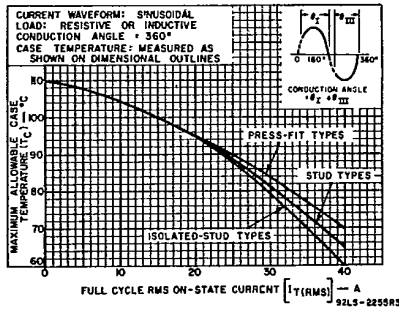


Fig. 3 - Maximum allowable case temperature vs. on-state current.

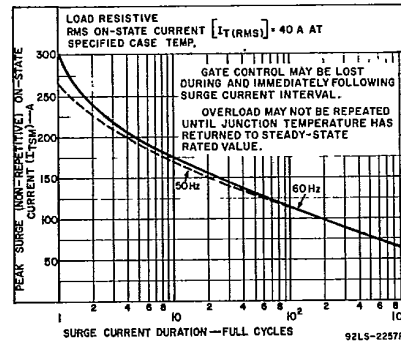


Fig. 4 - Peak surge on-state current vs. surge current duration.

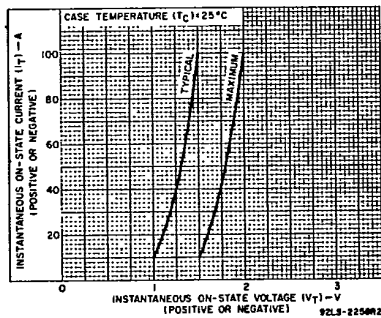


Fig. 5 - On-state current vs. on-stage voltage.

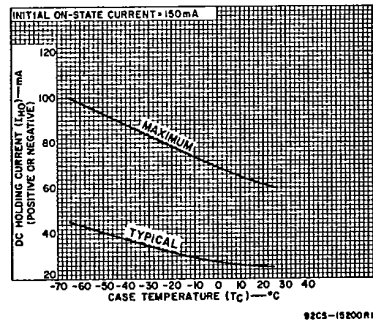


Fig. 6 - DC holding current vs. case temperature.

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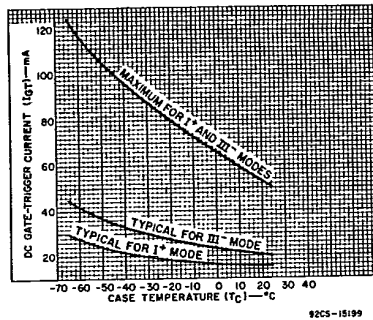


Fig. 7 - DC gate-trigger current vs. case temperature (I+ & III- modes).

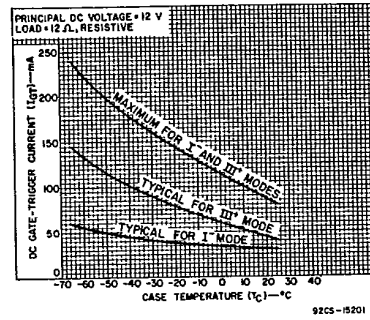


Fig. 8 - DC gate-trigger current vs. case temperature (I- & III+ modes).

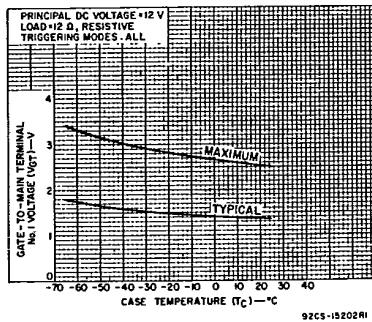


Fig. 9 - DC gate trigger voltage vs. case temperature.

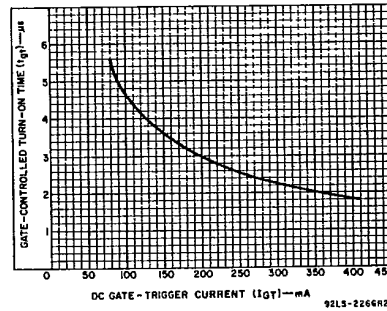


Fig. 10 - Turn-on time vs. gate-trigger current.

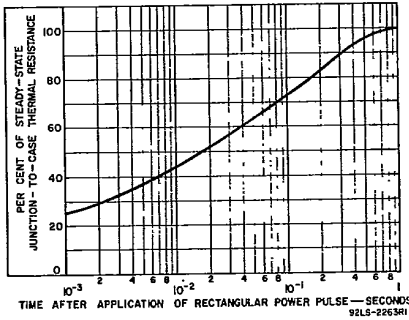


Fig. 11 - Transient junction-to-case thermal resistance vs. time for press-fit and stud types.

Tracs

2N5441-2N5446, T6420 Series

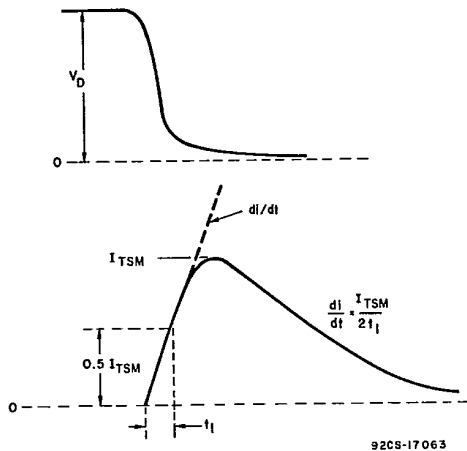


Fig. 12 - Rate of change of on-state current with time (defining di/dt).

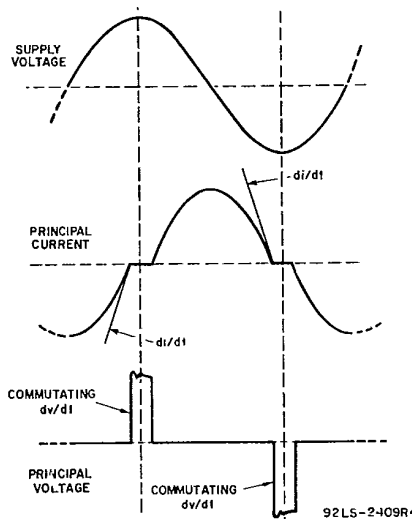


Fig. 13 - Relationship between supply voltage and principal current (Inductive load) showing reference points for definition of commutating voltage (dv/dt).

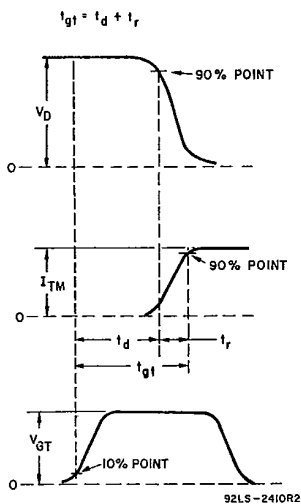


Fig. 14 - Relationship between off-state voltage, on-state current, and gate-trigger voltage showing reference points for definition of turn-on time (t_{gt}).