

# Silicon PNP Power Transistors

... for use in power amplifier and switching circuits, — excellent safe area limits. Complement to NPN 2N5191, 2N5192

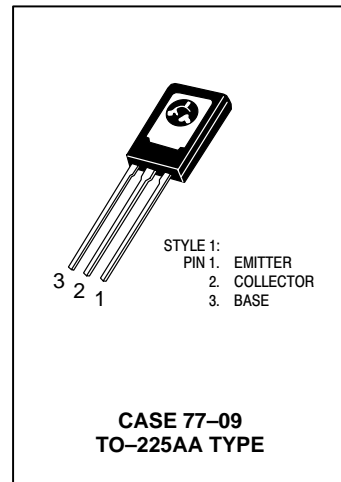
**2N5194\***  
**2N5195\***

\*ON Semiconductor Preferred Device

**4 AMPERE  
POWER TRANSISTORS  
SILICON PNP  
60–80 VOLTS**

**\*MAXIMUM RATINGS**

Rating	Symbol	2N5194	2N5195	Unit
Collector–Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector–Base Voltage	$V_{CB}$	60	80	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current	$I_C$	4.0		Adc
Base Current	$I_B$	1.0		Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40	320	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150		$^\circ\text{C/W}$



**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	3.12	$^\circ\text{C/W}$

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (1) ( $I_C = 0.1 \text{ Adc}, I_B = 0$ )	2N5194 2N5195	$V_{CEO(sus)}$	60 80	— — Vdc
Collector Cutoff Current ( $V_{CE} = 60 \text{ Vdc}, I_B = 0$ ) ( $V_{CE} = 80 \text{ Vdc}, I_B = 0$ )	2N5194 2N5195	$I_{CEO}$	— —	1.0 1.0 mAdc
Collector Cutoff Current ( $V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 60 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 80 \text{ Vdc}, V_{BE(off)} = 1.5 \text{ Vdc}, T_C = 125^\circ\text{C}$ )	2N5194 2N5195 2N5194 2N5195	$I_{CEX}$	— — — —	0.1 0.1 2.0 2.0 mAdc
Collector Cutoff Current ( $V_{CB} = 60 \text{ Vdc}, I_E = 0$ ) ( $V_{CB} = 80 \text{ Vdc}, I_E = 0$ )	2N5194 2N5195	$I_{CBO}$	— —	0.1 0.1 mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}, I_C = 0$ )		$I_{EBO}$	—	1.0 mAdc

\*Indicates JEDEC Registered Data.

(1) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

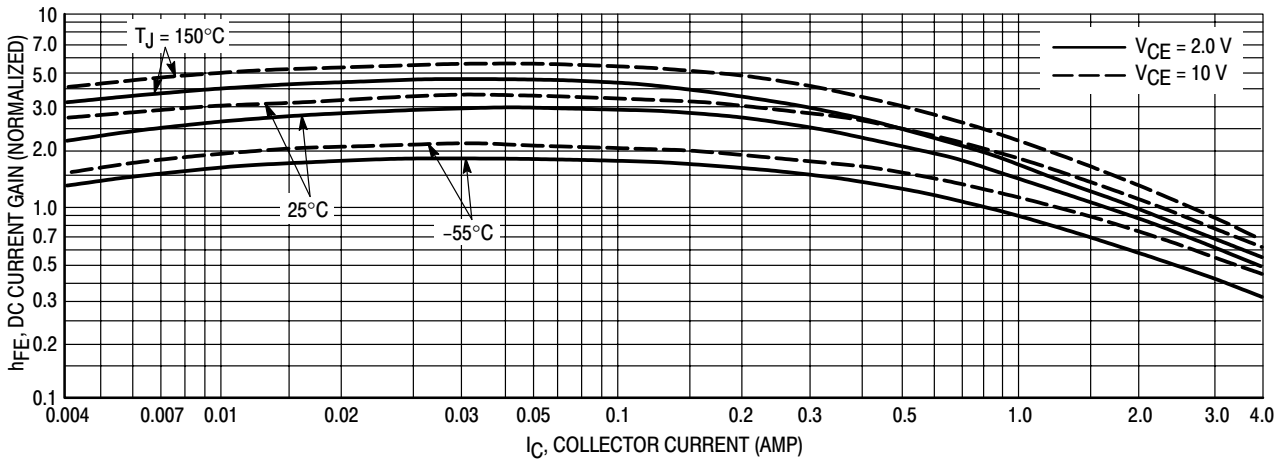
# 2N5194 2N5195

**\*ELECTRICAL CHARACTERISTICS — continued** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

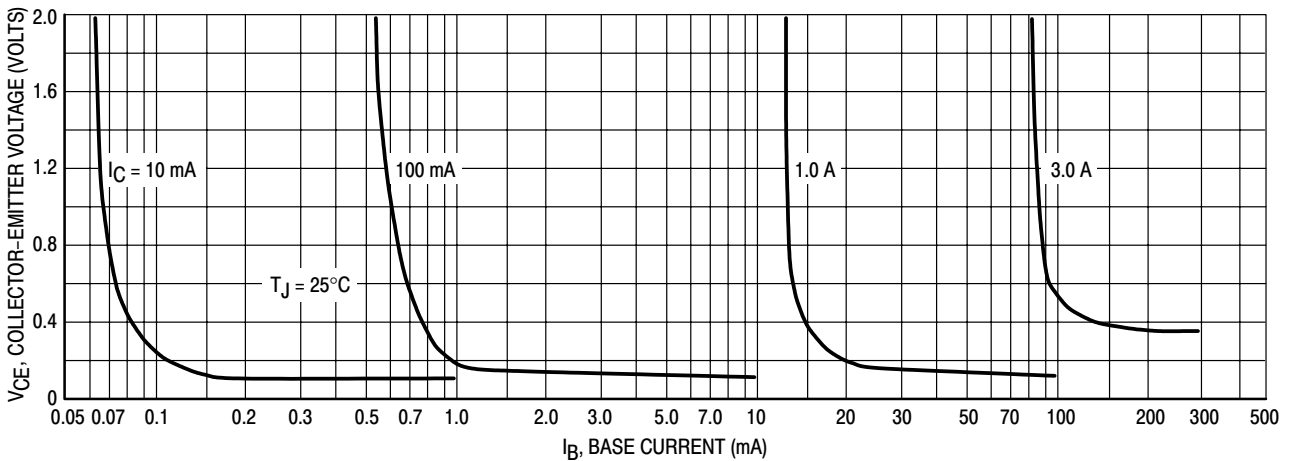
Characteristic	Symbol	Min	Max	Unit	
<b>ON CHARACTERISTICS</b>					
DC Current Gain (2) ( $I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	2N5194	25	100	—	
	2N5195	20	80	—	
	( $I_C = 4.0 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	2N5194	10	—	—
	2N5195	7.0	—	—	
Collector–Emitter Saturation Voltage (2) ( $I_C = 1.5 \text{ Adc}, I_B = 0.15 \text{ Adc}$ ) ( $I_C = 4.0 \text{ Adc}, I_B = 1.0 \text{ Adc}$ )	$V_{CE(sat)}$	—	0.6 1.4	Vdc	
Base–Emitter On Voltage (2) ( $I_C = 1.5 \text{ Adc}, V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}$	—	1.2	Vdc	
<b>DYNAMIC CHARACTERISTICS</b>					
Current–Gain — Bandwidth Product ( $I_C = 1.0 \text{ Adc}, V_{CE} = 10 \text{ Vdc}, f = 1.0 \text{ MHz}$ )	$f_T$	2.0	—	MHz	

\*Indicates JEDEC Registered Data.

(2) Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



**Figure 1. DC Current Gain**



**Figure 2. Collector Saturation Region**

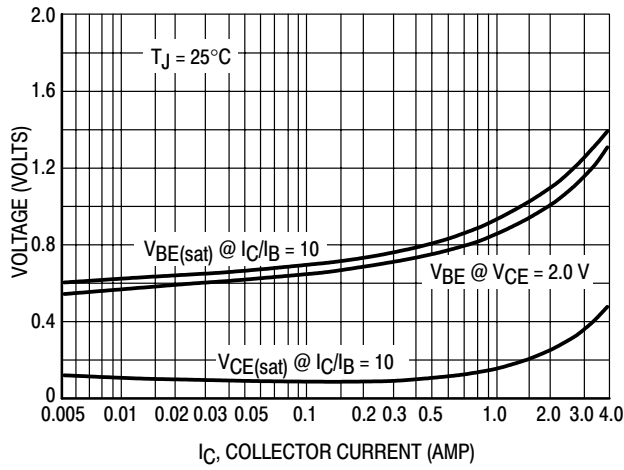


Figure 3. "On" Voltage

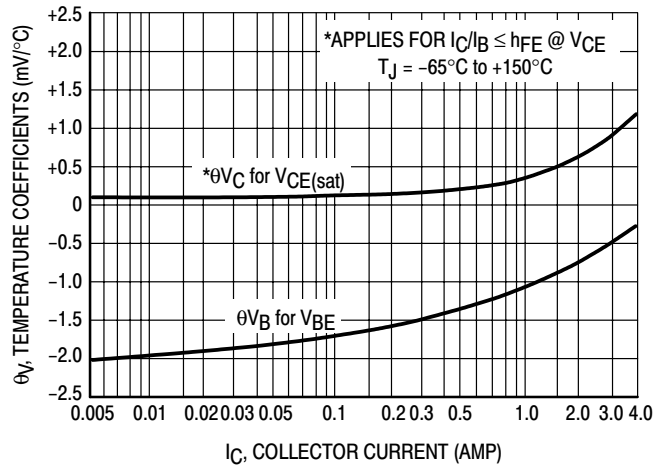


Figure 4. Temperature Coefficients

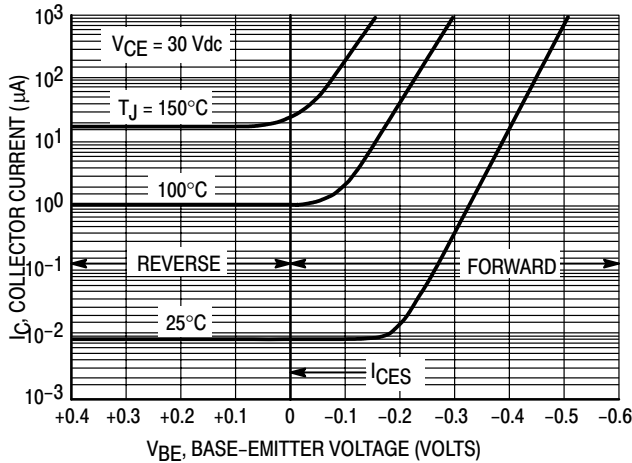


Figure 5. Collector Cut-Off Region

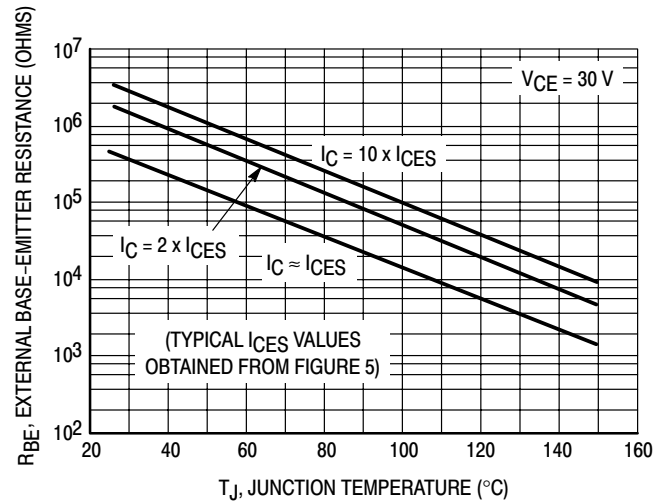


Figure 6. Effects of Base-Emitter Resistance

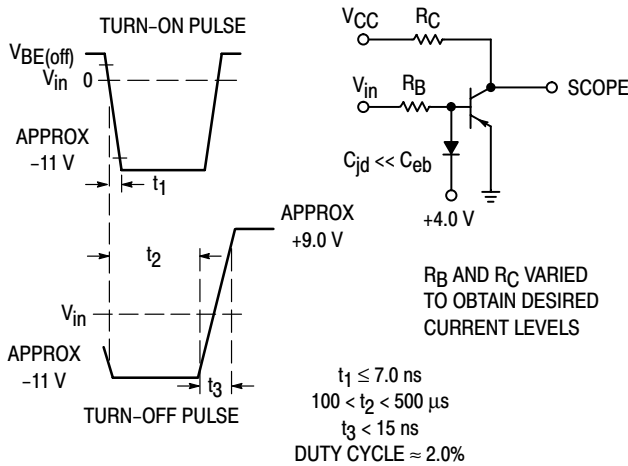


Figure 7. Switching Time Equivalent Test Circuit

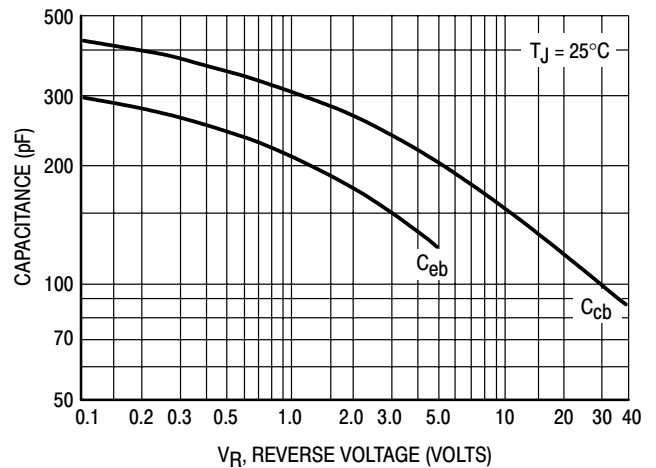


Figure 8. Capacitance

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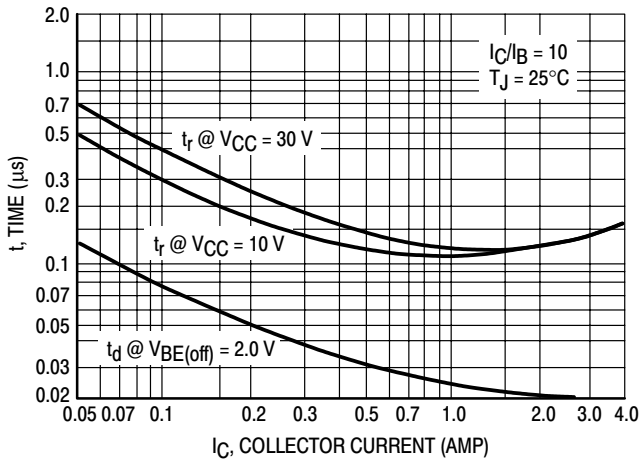


Figure 9. Turn-On Time

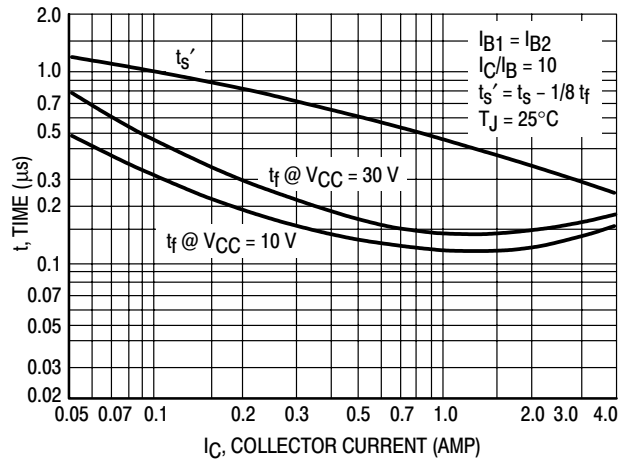


Figure 10. Turn-Off Time

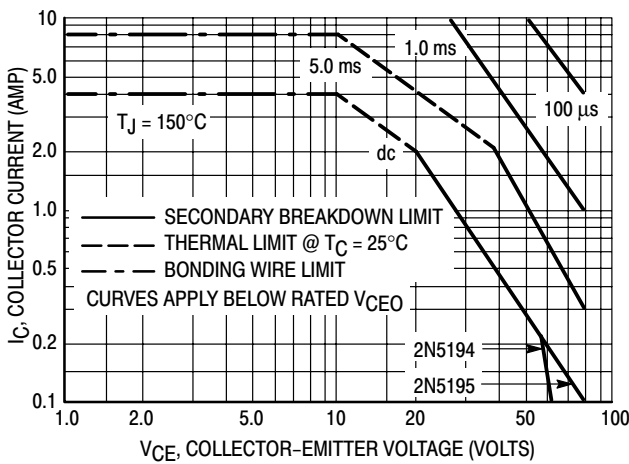


Figure 11. Rating and Thermal Data  
Active-Region Safe Operating Area

**Note 1:**

There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_{J(pk)} = 150^\circ\text{C}$ .  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high-case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

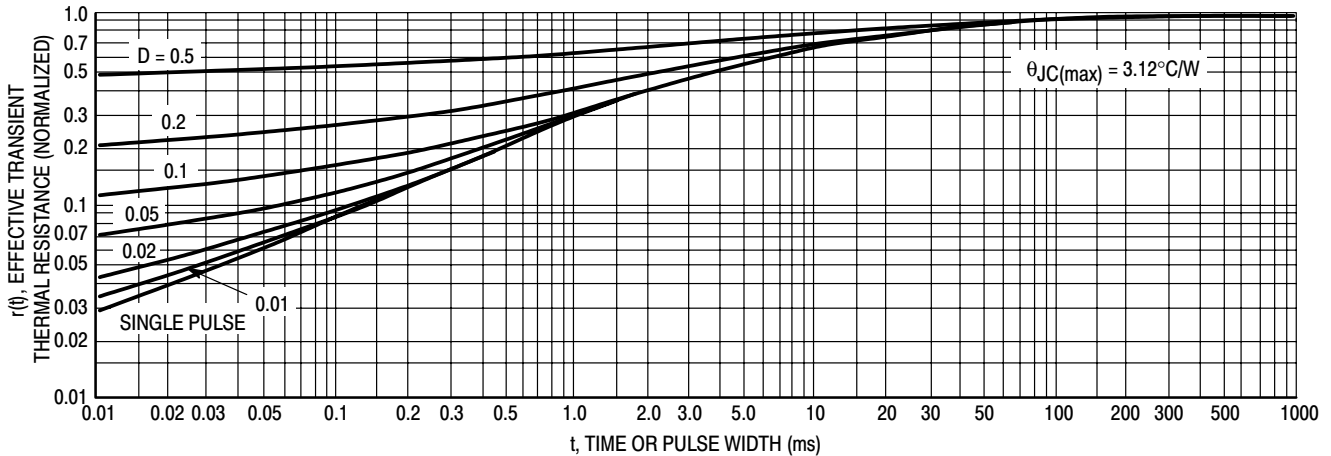


Figure 12. Thermal Response

DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA

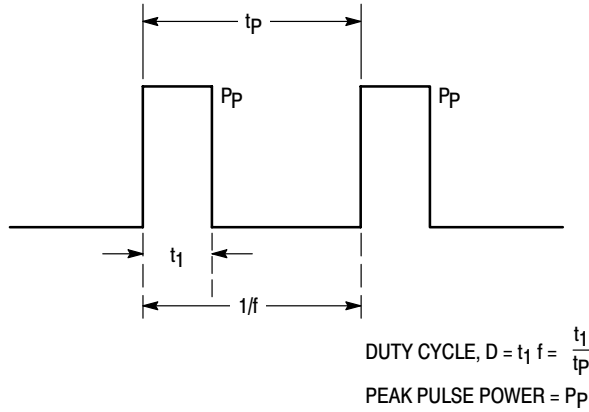


Figure 13.

A train of periodical power pulses can be represented by the model shown in Figure 13. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find  $\theta_{JC}(t)$ , multiply the value obtained from Figure 12 by the steady state value  $\theta_{JC}$ .

Example:

The 2N5193 is dissipating 50 watts under the following conditions:  $t_1 = 0.1$  ms,  $t_p = 0.5$  ms. ( $D = 0.2$ ).

Using Figure 12, at a pulse width of 0.1 ms and  $D = 0.2$ , the reading of  $r(t_1, D)$  is 0.27.

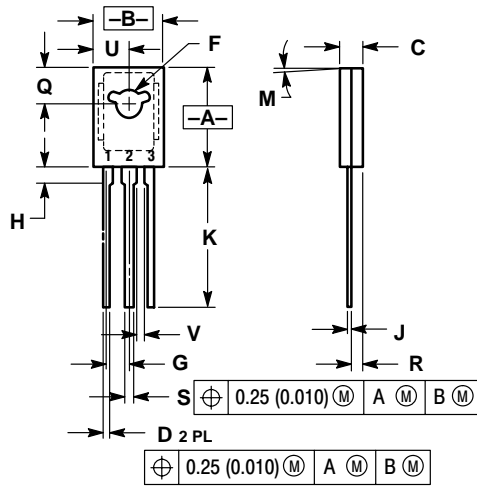
The peak rise in junction temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$

# 2N5194 2N5195

## PACKAGE DIMENSIONS

### TO-225AA CASE 77-09 ISSUE W



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

- STYLE 1:  
 PIN 1. EMITTER  
 2. COLLECTOR  
 3. BASE

## Notes

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