

Silicon Controlled Rectifiers Reverse Blocking Triode Thyristor

... designed for industrial and consumer applications such as power supplies, battery chargers, temperature, motor, light and welder controls.

- Supplied in Either Pressfit or Stud Package
- High Surge Current Rating — $I_{TSM} = 240$ Amps
- Low On-State Voltage — 1.2 V (Typ) @ $I_{TM} = 20$ Amps
- Practical Level Triggering and Holding Characteristics — 40 mA (Max) and 50 mA (Max) @ $T_C = 25^\circ\text{C}$

**2N5164
thru
2N5171**

**SCRs
20 AMPERES RMS
50 thru 600 VOLTS**



MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|------------------------------|-------------------------|----------------------|
| *Peak Forward and *Repetitive Reverse Blocking Voltage, Notes 1 and 2 2N5164, 2N5168 2N5165, 2N5169 2N5166, 2N5170 2N5167, 2N5171 | V_{DRM} or V_{RRM} | 50 200 400 600 | Volts |
| *Non-Repetitive Peak Reverse Blocking Voltage 2N5164, 2N5168 2N5165, 2N5169 2N5166, 2N5170 2N5167, 2N5171 | V_{RSM} | 75 300 500 700 | Volts |
| On-State Current RMS | $I_T(\text{RMS})$ | 20 | Amps |
| Average On-State Current ($T_C = 67^\circ\text{C}$) | $I_T(\text{AV})$ | 13 | Amps |
| Circuit Fusing ($T_J = -40$ to $+100^\circ\text{C}$, $t \leq 8.3$ ms) | I^2t | 235 | A^2s |
| *Peak Non-Repetitive Surge Current (One cycle, 60 Hz, $T_J = -40$ to $+100^\circ\text{C}$) Preceded and followed by rated current and voltage | I_{TSM} | 240 | Amps |
| *Peak Gate Power (Maximum Pulse Width = 10 μs) | P_{GM} | 5 | Watts |
| *Average Gate Power | $P_{G(\text{AV})}$ | 0.5 | Watt |
| *Peak Forward Gate Current (Maximum Pulse Width = 10 μs) | I_{GM} | 2 | Amps |
| Peak Gate Voltage | V_{GM} | 10 | Volts |
| *Operating Junction Temperature Range | T_J | -40 to +100 | $^\circ\text{C}$ |
| *Storage Temperature Range | T_{stg} | -40 to +150 | $^\circ\text{C}$ |
| Stud Torque 2N5168-2N5171 | | 30 | in. lb. |

*Indicates JEDEC registered data.

Notes: 1. V_{DRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.

2. Devices should not be operated with a positive bias applied to the gate concurrent with a negative potential applied to the anode.



**CASE 263-04
STYLE 1
2N5168 thru 2N5171**



**CASE 310-02
STYLE 1
2N5164 thru 2N5167**

2N5164 thru 2N5171

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|-----------------|----------|------------|---------------|
| *Thermal Resistance, Junction to Case 2N5164, 65, 66, 67 2N5168, 69, 70, 71 | $R_{\theta JC}$ | 1 1.1 | 1.5 1.6 | $^{\circ}C/W$ |

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted.)

| Characteristic | Symbol | Min | Max | Unit |
|--|--------------------|---------------|-----------------|---------------|
| *Peak Forward or Reverse Blocking Current (Rated V_{DRM} or V_{RRM} , gate open) $T_J = 25^{\circ}C$ $T_J = 100^{\circ}C$ | I_{DRM}, I_{RRM} | — — | 10 5 | μA mA |
| Gate Trigger Current (Continuous dc), Note 1 ($V_D = 7 V_{dc}, R_L = 100 \Omega$) *($V_D = 7 V_{dc}, R_L = 100 \Omega, T_C = -40^{\circ}C$) | I_{GT} | — — | 40 75 | mA |
| Gate Trigger Voltage (Continuous dc) ($V_D = 7 V_{dc}$, gate open) *($V_D = 7 V_{dc}, R_L = 100 \Omega, T_C = -40^{\circ}C$) *($V_D = \text{Rated } V_{DRM}, R_L = 100 \Omega, T_J = 100^{\circ}C$) | V_{GT} | — — 0.2 | 1.5 2.5 — | Volts |
| Peak On-State Voltage (Pulse Width = 1 ms max, duty cycle $\leq 1\%$) ($I_{TM} = 20 A$) *($I_{TM} = 41 A$) | V_{TM} | — 8 | 1.5 1.7 | Volts |
| Holding Current ($V_D = 7 V_{dc}$, gate open) *($V_D = 7 V_{dc}$, gate open, $T_C = -40^{\circ}C$) | I_H | — — | 50 90 | mA |
| Gate Controlled Turn-On Time ($t_d + t_r$) ($I_{TM} = 20 A, I_{GT} = 40 \text{ mAdc}, V_D = \text{Rated } V_{DRM}$) | t_{gt} | Typical | | μs |
| | | 1 | | |
| Circuit Commutated Turn-Off Time ($I_{TM} = 10 A, I_R = 10 A$) ($I_{TM} = 10 A, I_R = 10 A, T_J = 100^{\circ}C$) ($V_D = V_{DRM} = \text{rated voltage}$) ($dv/dt = 30 V/\mu s$) | t_q | 20 30 | | μs |
| Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}$, Exponential Wave Form, Gate open, $T_J = 100^{\circ}C$) | dv/dt | 50 | | $V/\mu s$ |

*Indicates JEDEC registered data.

Note 1. Devices should not be operated with a positive bias applied to the gate concurrent with a negative potential applied to the anode.

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EFFECT OF TEMPERATURE UPON TYPICAL TRIGGER CHARACTERISTICS

FIGURE 1 - GATE TRIGGER CURRENT

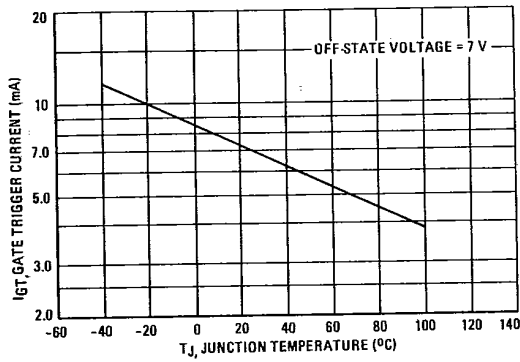
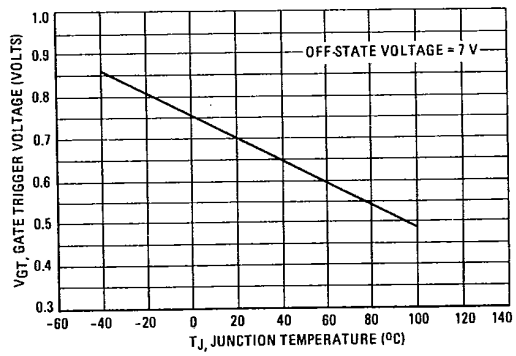


FIGURE 2 - GATE TRIGGER VOLTAGE



MAXIMUM ALLOWABLE NON-REPETITIVE SURGE CURRENT

FIGURE 3 - 60 Hz SURGES

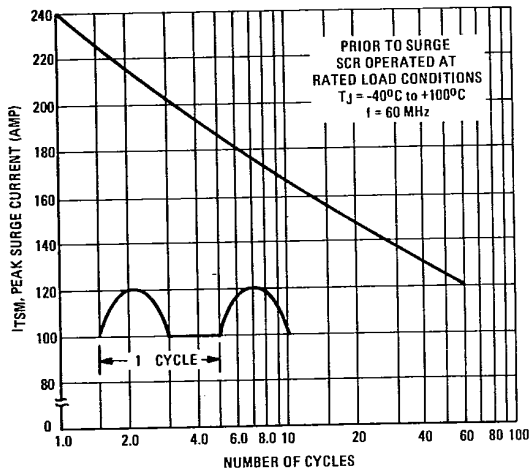
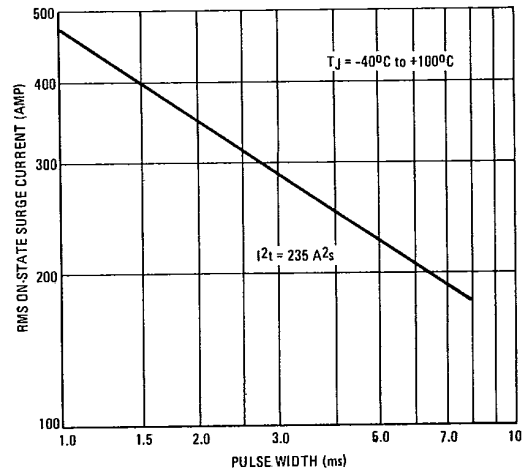


FIGURE 4 - SUB-CYCLE SURGES



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2N5164 thru 2N5171

FIGURE 5 - GATE TRIGGER CHARACTERISTICS

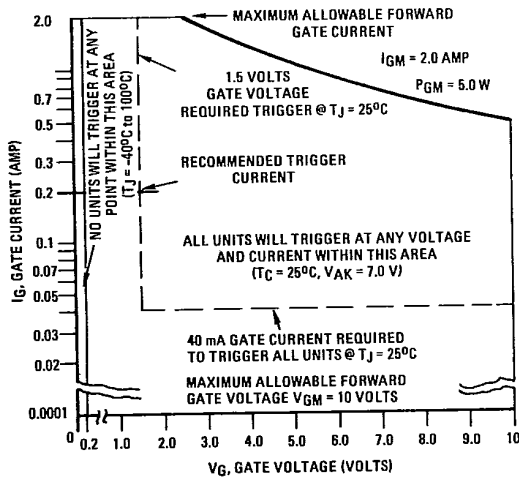
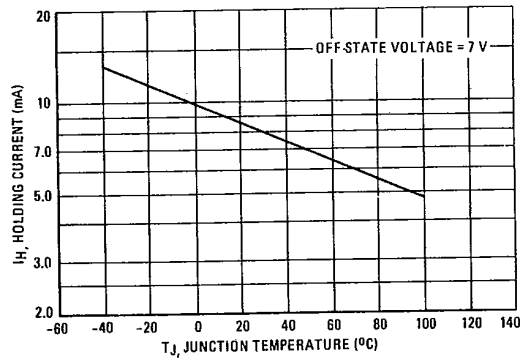


FIGURE 6 - EFFECT OF TEMPERATURE ON TYPICAL HOLDING CURRENT



DERATING AND DISSIPATION FOR RESISTIVE AND INDUCTIVE LOADS (f = 60 to 400 Hz, SINE WAVE)

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FIGURE 7 - AVERAGE CURRENT DERATING

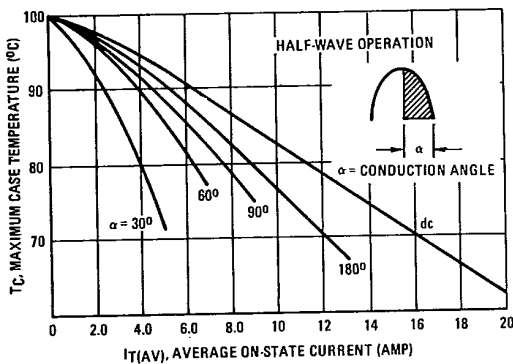


FIGURE 8 - ON-STATE POWER DISSIPATION

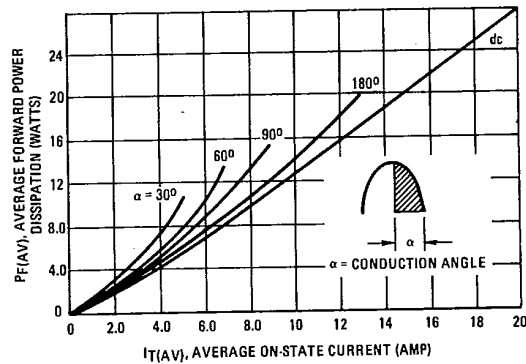


FIGURE 9 - ON-STATE CHARACTERISTICS

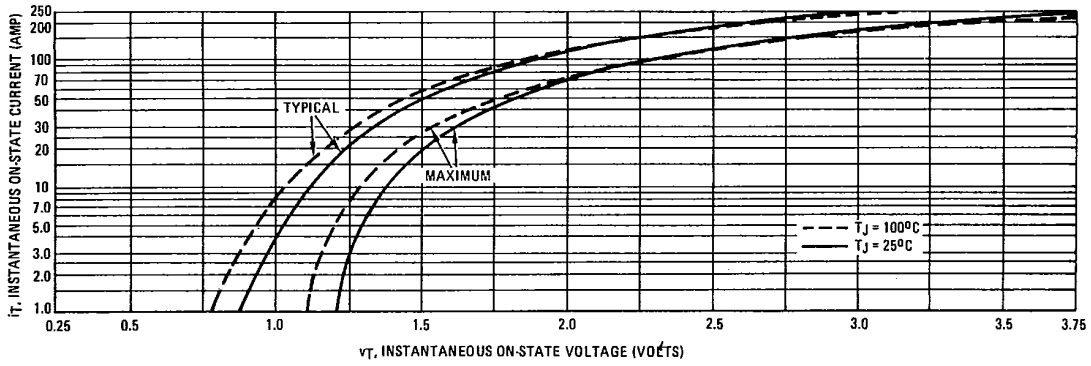


FIGURE 10 - TYPICAL THERMAL RESISTANCE OF PLATES

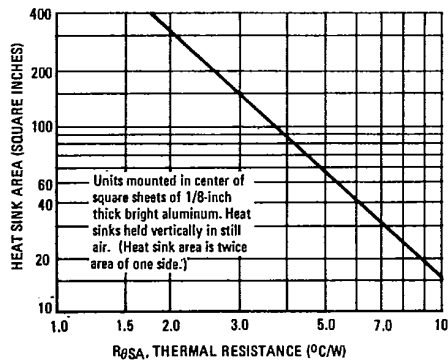
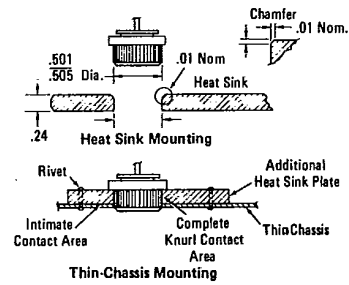


FIGURE 11 - MOUNTING DETAILS FOR PRESSFIT THYRISTORS



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