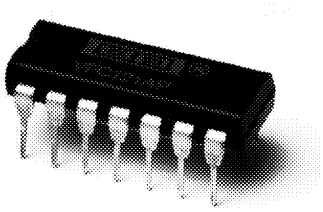
BURR-BROWN®



VFC121

Precision Single Power Supply VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- SINGLE SUPPLY OPERATION: +4.5V to +36V
- f_o = 1.5MHz max
- LOW NONLINEARITY: 0.03% max at 100kHz, 0.1% max at 1MHz
- HIGH INPUT IMPEDANCE
- VOLTAGE REFERENCE OUTPUT
- THERMOMETER OUTPUT: 1mV/°K

APPLICATIONS

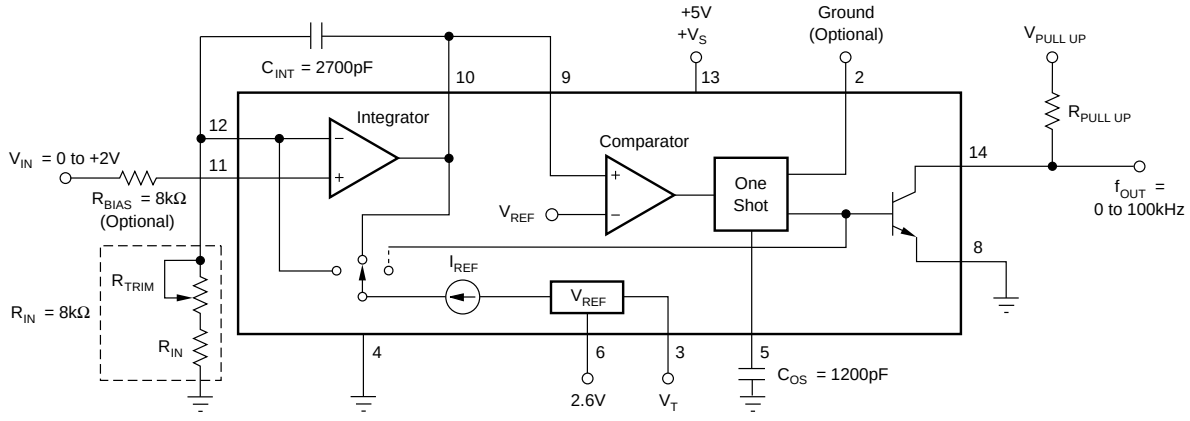
- INTEGRATING A/D CONVERSION
- ANALOG SIGNAL TRANSMISSION
- PHASE-LOCKED LOOP VCO
- GALVANICALLY ISOLATED SYSTEMS

DESCRIPTION

The VFC121 is a monolithic voltage-to-frequency converter consisting of an integrating amplifier, voltage reference, and one-shot charge pump circuitry. High-frequency complementary NPN/PNP circuitry is used to implement the charge-balance technique, achieving speed and accuracy far superior to previous single power supply VFCs.

The high-impedance input accepts signals from ground potential to V_S – 2.5V. Power supplies from 4.5V to 36V may be used. A 2.6V reference voltage output may be used to excite sensors or bias external circuitry. A thermometer output voltage proportional to absolute temperature (°K) may be used as a temperature sensor or for temperature compensation of applications circuits.

Frequency output is an open-collector transistor. A disable pin forces the output to the high impedance state, allowing multiple VFCs to share a common transmission path.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ, unless otherwise noted.

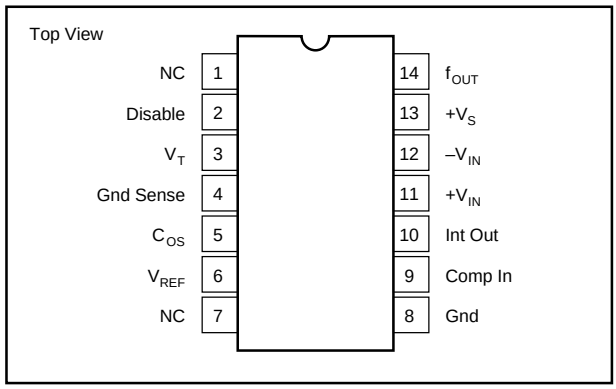
PARAMETER	CONDITIONS	VFC121AP			VFC121BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Nonlinearity: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			0.05			0.03	%FS
f_{FS} = 1MHz	C_{OS} 68pF, C_{INT} = 270pF		0.1				0.1	%FS
Gain Error: f_{FS} = 100kHz	C_{OS} 1200pF, C_{INT} = 2700pF			10			*	%FS
Gain Drift: f_{FS} = 100kHz	T_{MIN} to T_{MAX}			80			40	ppm/°C
Relative to V_{REF}	$+V_S$ = +5V to +36V			100			40	ppm/°C
PSRR				0.025			*	%/V
INPUT								
Minimum Input Voltage				0			*	V
Maximum Input Voltage		V_S – 2.5	V_S – 2		*	*		V
Impedance		10	100		*	*		MΩ
I_{BIAS}			150	300		*	*	nA
V_{OS}			300	800		100	400	µV
V_{OS} Drift	T_{MIN} to T_{MAX}		10			*		µV/°C
OPEN COLLECTOR OUTPUT								
V_{SAT}	$I_{PULL\ UP}$ = 10mA			0.4			*	V
$I_{LEAKAGE}$	$V_{PULL\ UP}$ = 5V			1			*	µA
	$V_{PULL\ UP}$ = 36V			10			*	µA
Fall Time				100			*	ns
Delay to Rise	$R_{PULL\ UP}$ = 470Ω			100			*	ns
Settling Time	To Specified Linearity for Full Scale Input Step	(1)						
REFERENCE VOLTAGE								
Voltage		2.59	2.6	2.61	*	*	*	V
Voltage Drift				100			50	ppm/°C
Load Regulation	I_O = 0 to 10mA			10			*	mV
PSRR	V_S = +5V to +36V			10			*	mV
Current Limit		Short Circuit Protected						
INTEGRATOR AMPLIFIER OUTPUT								
Output Voltage Range	R_L = 100kΩ	0.8		2.9	*		*	V
COMPARATOR INPUT								
I_{BIAS}			+1			*		µA
Trigger Voltage			2.6			*		V
Input Voltage Range		0		2.9	*		*	V
THERMOMETER								
V_T	T_A = +25°C		298			*		mV
V_T Slope	T_{MIN} to T_{MAX}		1			*		mV/°K
DISABLE INPUT								
V_{HIGH} (Disabled)		2			*			V
V_{LOW}				0.8			*	V
I_{HIGH} (Disabled)	V_{HIGH} = 2V		10			*		µA
I_{LOW}	V_{LOW} = 0.8V		10			*		µA
POWER SUPPLY								
Voltage		4.5	5	36	*	*	*	V
Current			7.5	10		*	*	mA
TEMPERATURE RANGE								
Specified		–25		+85	*		*	°C
Storage		–40		+125	*		*	°C

* Same specification as VFC121AP.
NOTE: (1) One pulse of new frequency plus 1µs.

ORDERING INFORMATION

MODEL	PACKAGE	LINEARITY ERROR, MAX (f_S = 100kHz)	TEMPERATURE RANGE
VFC121AP	Plastic DIP	0.05%	–25°C to +85°C
VFC121BP	Plastic DIP	0.03%	–25°C to +85°C

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_S$) 40V
f_{OUT} Sink Current 20mA
Comparator In Voltage ..... –0.5V to +3V
Enable Input ..... –0.3V to $+V_S$
Integrator Common-Mode Voltage ..... 0V to $+V_S$ – 2V
Integrator Differential Input Voltage ..... –0.3V to +0.3V
V_{REF} Out (short-circuit) ..... Indefinite
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature ..... –40°C to +125°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses above these ratings may permanently damage the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION

PIN #	NAME	DESCRIPTION
1	NC	Not Connected
2	Disable	Input logic Low for normal operation. Input logic High to disable the VFC121. Has internal pull-down, for normal operation if not connected.
3	V_T	Temperature compensation voltage proportional to absolute temperature. Typically 298mV at room temperature (298°K), with a change of 1mV per °C (°K).
4	Gnd Sense	Defines ground for the internal voltage reference.
5	C_{OS}	One-shot capacitor is connected between here and ground to set full scale output frequency.
6	V_{REF}	Output from the internal band-gap voltage reference, typically 2.6V. Can be used externally to set levels or excite sensors.
7	NC	Not Connected
8	Gnd	Ground
9	Comp In	Comparator In
10	Int Out	Integrator Out
11	$+V_{IN}$	Non-inverting input of the integrating op amp. The input signal is applied here.
12	$-V_{IN}$	Inverting input of the integrating op amp. C_{INT} is connected between here and the integrator output (pin 10), and R_{IN} is connected between here and ground.
13	$+V_S$	Supply voltage connected here. Range is +4.5V to +36V.
14	f_{OUT}	Frequency output pin. This is the output of an open-collector transistor, and an external pull-up circuit should be used to generate the appropriate logic levels.

PACKAGE INFORMATION

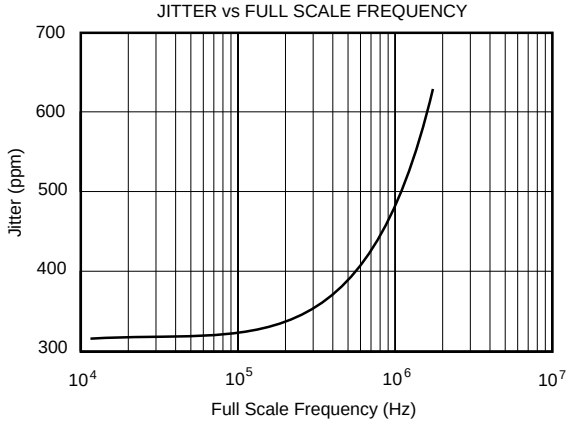
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
VFC121AP	14-Pin Plastic DIP	010
VFC121BP	14-Pin Plastic DIP	010

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

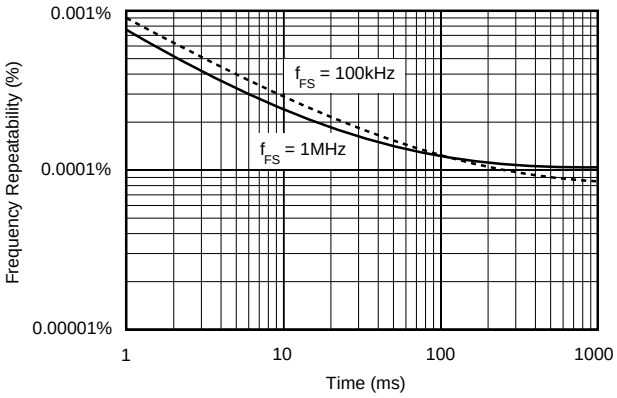
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ, unless otherwise noted.

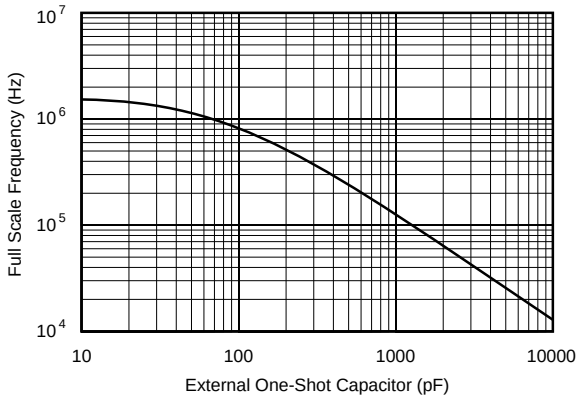
JITTER vs FULL SCALE FREQUENCY



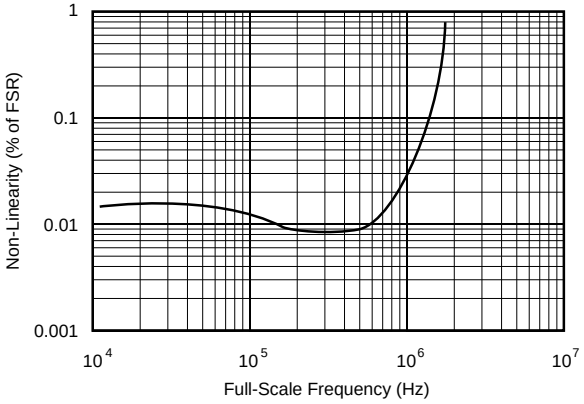
FREQUENCY COUNT REPEATABILITY
vs COUNTER GATE TIME



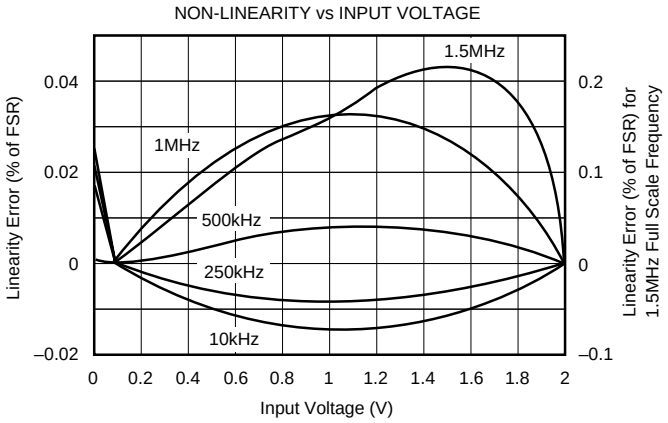
FULL SCALE FREQUENCY
vs EXTERNAL ONE-SHOT CAPACITOR



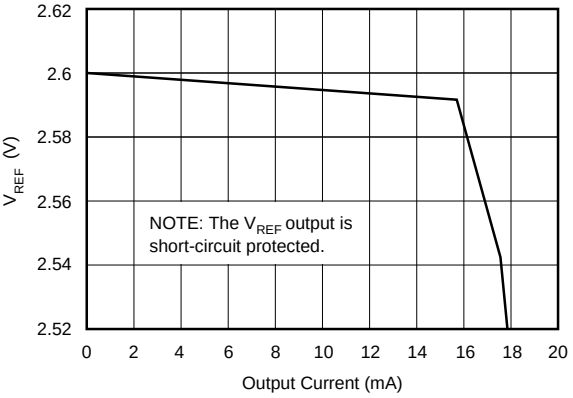
NON-LINEARITY
vs FULL-SCALE FREQUENCY



NON-LINEARITY vs INPUT VOLTAGE

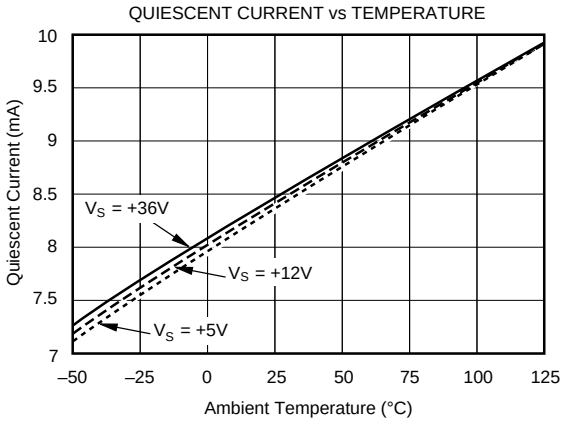


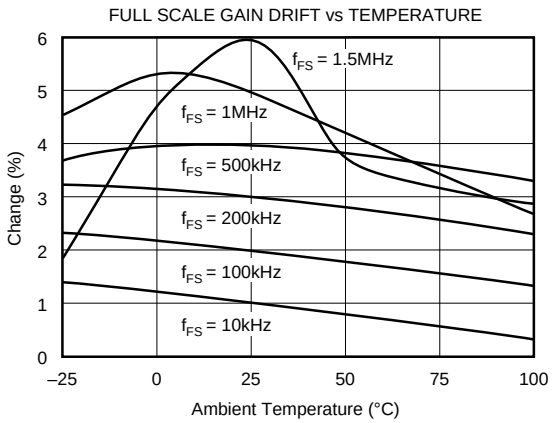
REFERENCE VOLTAGE
vs REFERENCE LOAD CURRENT



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = +5V, and R_{IN} = 8kΩ, unless otherwise noted.





THEORY OF OPERATION

The VFC121 uses a charge-balance technique to achieve high accuracy. The basic architecture is shown in Figure 1. An analog integrator at the front end, consisting of a precision op amp and a feedback capacitor, C_{INT}, provides a true integrating approach for improved noise immunity. Use of the non-inverting input of the op amp for the analog input provides a high input impedance to the user.

The integrator's output is proportional to the charge stored on C_{INT} plus the analog input voltage. An input voltage, V_{IN}, forces a current through R_{IN} of V_{IN}/R_{IN}, which also flows through C_{INT}. This current through C_{INT} causes the integrator output to ramp positive. (Refer to the timing diagram in Figure 2.)

When the output of the integrator ramps to V_{REF}, the comparator trips, driving the output of the VFC121 Low, and triggering the one-shot. The tripping of the comparator also connects the reference current, I_{REF}, to the integrator input for the duration of the one-shot period, T_{OS}. This switched current causes the output of the integrator to ramp negative.

When the one-shot times out, the output of the VFC121 is reset High, the one-shot is reset, and I_{REF} is switched to the output of the integrating op amp. (This causes the output of

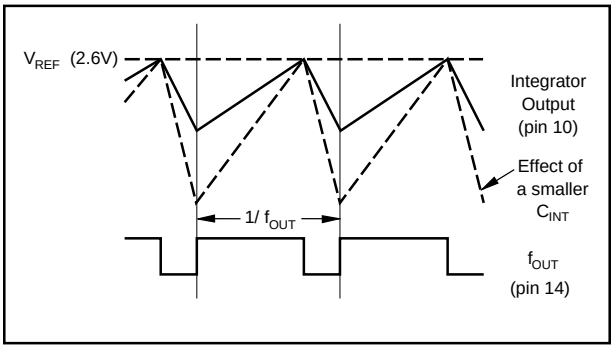


FIGURE 2. Timing Diagram.

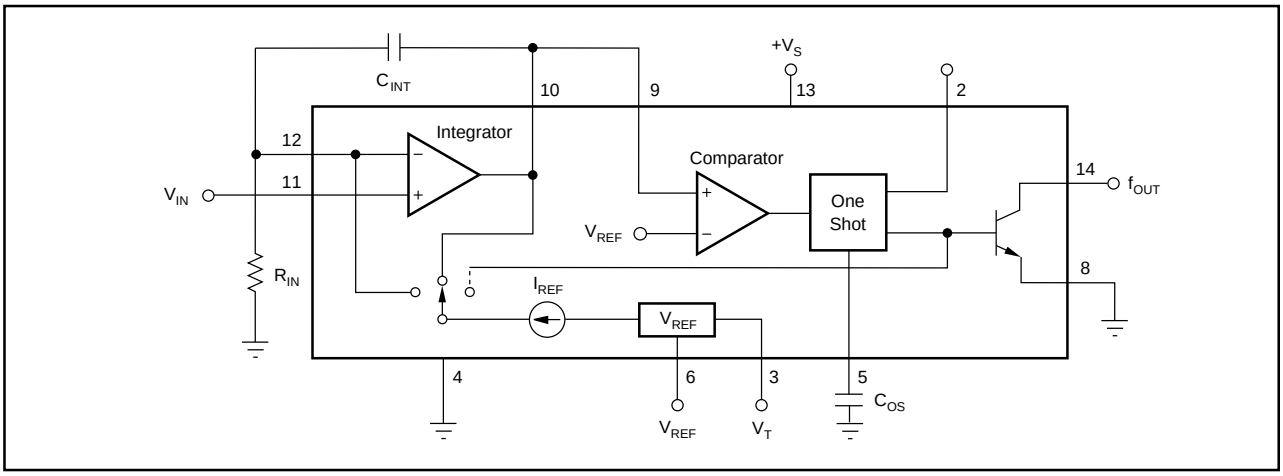


FIGURE 1. VFC121 Architecture.

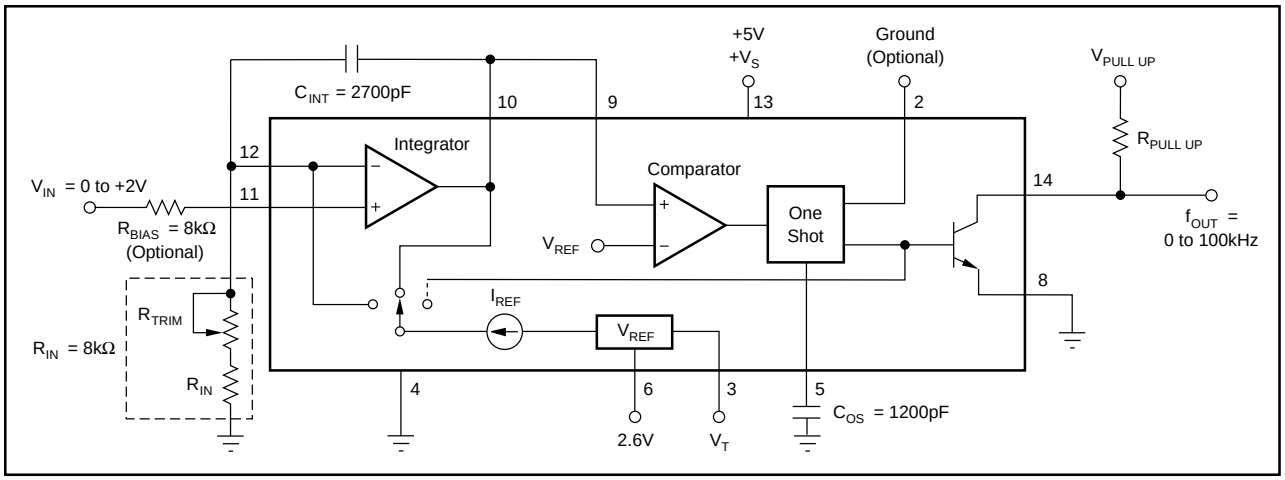


FIGURE 3. 2V Full Scale Input, 100kHz Full Scale Output.

the integrating op amp to see a constant current, reducing errors that might occur if the load were unbalanced.) In this state, the output of the integrator resumes a positive ramp, restarting the cycle.

The output frequency is regulated by the balance of current (or charge) between the current V_{IN}/R_{IN} and the time-averaged reset current. The size of the integrating capacitor, C_{INT}, determines the slew rate of the integrator, and thus how far down the integrator ramps during the one-shot period, but has no effect on the output frequency of the VFC121.

The reference voltage used internally is generated from a bandgap reference, which is actively trimmed to achieve the low drift characteristics of the VFC121. To maximize flexibility of designs using the VFC121, both the bandgap reference voltage and a thermometer voltage are available externally.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC OPERATION

The VFC121 allows users a wide range of input voltages and supply voltages, and easy control of the full scale output frequency. The basic connections are shown in Figure 3, with components that generate a 100kHz output with a 2V full scale input.

For other input and output ranges, the full scale input voltages and full scale output frequencies can be calculated as follows:

$$f_{FS} = \frac{V_{FS}}{2(R_{IN})(C_{OS} + 60)}$$

The full scale input current of 250µA was chosen to provide a 25% duty cycle in the output frequency. The VFC121 is designed to give optimum linearity under these conditions, but other current levels can be used without significantly degrading linearity. By reducing R_{IN}, the integrating current is increased, increasing the positive ramp rate of the integrator output. Since the one-shot period is unchanged, the duty cycle of the output increases.

Stray capacitance at the C_{OS} pin typically adds about 60pF to the capacitance of the external C_{OS}, which accounts for the adjustment in the above equation. This usually becomes negligible as the required output frequency is reduced, and C_{OS} is increased.

R_{BIAS} is included in the circuit in Figure 3 to compensate for the effects of bias currents at the input of the integrating op amp. It is optional in most applications, but when needed, R_{BIAS} should equal R_{IN}.

Table 1 indicates standard external component values for common input voltage ranges and output frequency ranges.

COMPONENT SELECTION

Selection of the external resistor and capacitor type is important. Temperature drift of the external input resistor and one-shot capacitor will affect temperature stability of the output frequency. NPO ceramic capacitors will normally produce the best results. Silver-mica types will result in slightly higher drift, but may be adequate in many applications. A low temperature coefficient film resistor should be used for R_{IN}.

The integrator capacitor, C_{INT}, serves as a "charge bucket," where charge accumulation is induced by the input, V_{IN}, and

FULL SCALE INPUT RANGE (V)	$R_{IN} + R_{TRIM}$ (kΩ)	
2	8	
5	20	
10	40	
FULL SCALE OUTPUT FREQUENCY (kHz)	**C_{OS} (pF)**	**C_{INT} (pF)**
1500	22	150
1000	68	270
500	180	470
250	470	1000
125	1000	2200
25	4700	10,000
NOTE: Higher output frequencies can be achieved by reducing R_{IN}.		

TABLE 1. Standard External Component Values

repeatedly reduced during the one-shot period. The size of the bucket (the capacitor value) is not critical, since it primarily determines how far below V_{REF} the output of the integrator ramps during the one-shot period. At the same time, the capacitor used must not leak since capacitor leakage or dielectric absorption can affect the linearity and offset of the transfer function. High-quality ceramic capacitors can be used for values less than 0.01µF, but caution should be used with higher value ceramic capacitors. High-k ceramic capacitors may have voltage non-linearities which can degrade overall linearity. Polystyrene, polycarbonate, or mylar film capacitors are superior for higher capacitance values.

During the one-shot period, the output of the integrator is ramping down. To prevent the integrating op amp from being saturated at its minimum output of 0.8V, C_{INT} should be kept at least 1.7 x C_{OS}.

OUTPUT FREQUENCY ADJUSTMENT

The full scale output frequency of the VFC121 can be adjusted using a trim-pot, R_{TRIM} in Figure 3, in series with R_{IN}. For optimum drift vs temperature, a low temperature coefficient fixed resistor of approximately 90% of the calculated R_{IN} requirement should be used in series with a trim-pot approximately 20% of the size of the calculated R_{IN}. The low-drift fixed resistor contributes most of the final R_{IN} resistance, so that the effect of higher drift from the trim-pot is attenuated in the total R_{IN}.

PULL-UP RESISTOR

The VFC121's frequency output is an open-collector transistor. A pull-up resistor should be connected from f_{OUT} to the logic supply, $+V_L$. The output transistor is On during the one-shot period, causing the output to be logic Low. The current flowing in this resistor should be limited to 10mA to assure a 0.4V maximum logic Low. The value chosen for the pull-up resistor may depend on the full-scale frequency and capacitance on the output line. Excessive capacitance on f_{OUT} will cause a slow, rounded rising edge at the end of an output pulse. This effect can be minimized by using a pull-up resistor which sets the output current to its maximum of 10mA. The logic power supply can be any positive voltage up to +36V.

ENABLE PIN

If left unconnected, the Enable input will assume a logic Low level, enabling the output stage, Alternatively, the Enable input may be connected directly to ground. This pin can also be driven by standard TTL or CMOS logic.

A logic High at the Enable input causes output pulses to cease. This is accomplished by interrupting the signal path through the one-shot circuitry. While disabled, all circuitry remains active and quiescent current is unchanged. Since no reset current pulses can occur while disabled, any positive input voltage will cause the integrator op amp to ramp positive and saturate at its most positive output swing of approximately V_{REF} + 0.7V.

When the Enable input receives a logic Low (less than 0.8V), a reset current cycle is initiated, (causing f_{OUT} to go Low). The integrator ramps negatively and normal operation is established. The time required for the output frequency to stabilize is equal to approximately one cycle of the final output frequency plus 1µs.

Using the Enable input, the outputs from several VFCs can be connected to a single line. All disabled VFCs will have a high output impedance; one active VFC can then transmit on the line. Since disabled VFCs are not oscillating, they cannot interfere or "lock" with the operating VFC. Locking can occur when one VFC operates at nearly the same frequency, or a multiple, as a nearby VFC. Coupling between the two may cause them to lock to the same frequency or an exact multiple. It then takes a small incremental input voltage change on one of the VFCs to unlock them. Locking cannot occur when unneeded VFCs are disabled.

APPLICATION INFORMATION

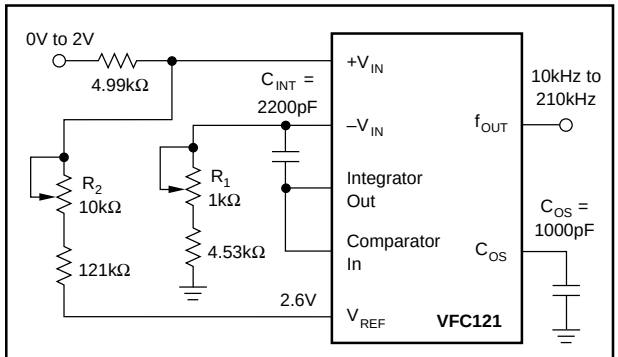
OPERATION FROM 10kHz TO 210kHz

The VFC121 is designed to provide an output frequency starting at 0Hz for a 0V input and increasing linearly to the full scale output frequency, f_{FS}, at the full scale input voltage, V_{FS}. For applications where low level inputs, near 0V, are critical, it may be inconvenient to have an output frequency approaching 0Hz. Figure 4 shows a circuit which transforms a 0V to 2V input level into output frequencies from 10kHz to 210kHz, by placing a resistor divider network between the input source and the V_{REF} output of the VFC121. This produces a positive voltage at $+V_{IN}$ when the input to the circuit is grounded. This circuit makes use of the high input impedance at $+V_{IN}$.

The transfer function of this circuit is:

$$V_{IN} = \frac{f_{OUT} - 10kHz}{100kHz} \text{ V}$$

To trim the circuit, first apply 2V to the analog input, and adjust R_1 to give a full scale output frequency of 210kHz. Then apply 0V to the analog input, and adjust R_2 until the output frequency is 10kHz. For absolute precision, it may be necessary to make several iterations trimming R_1 and R_2. In most cases, one iteration will be enough, since the effect of R_2 on



NOTE: Use 1% metal film fixed resistors, Cermet® trim pots, and NPO ceramic capacitors.

FIGURE 4. Offsetting the Output Frequency.

full scale output frequency is attenuated by the divider network, which sees only a 0.6V total delta at full scale (2.6V at V_{REF} minus 2V full scale input) as compared with a 2.6V delta at a 0V input level.

USING THE VFC121 THERMOMETER VOLTAGE

Because of the high input impedance of the VFC121 (which results from using the non-inverting input to the integrating op amp), it is relatively simple to use a standard multiplexer in front of the VFC121. One of the possible reason to multiplex the input to the VFC121 is to use it to track temperature changes in the operating environment of the electronics in a system, in addition to using the VFC121 in its normal mode to measure an analog signal.

Figure 5 shows a way to do this. In this circuit, the normal analog input signals to be multiplexed through the VFC121 have a full scale voltage of 2V, and generate a full scale output frequency of 100kHz. To measure the electronics system temperature, the user selects the multiplexer channel connected to the thermometer voltage on pin 3. A measured output frequency from the VFC121, with the multiplexer on channel 8, now corresponds to the temperature of the electronics as follows:

$$\text{Temp (°C)} = \frac{\text{Output Frequency} - 13{,}650}{50}$$

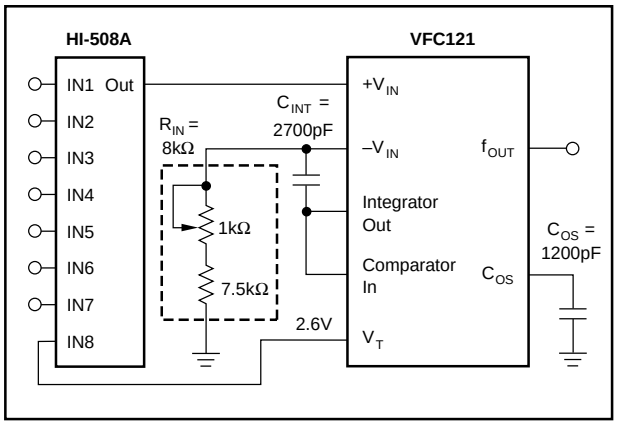
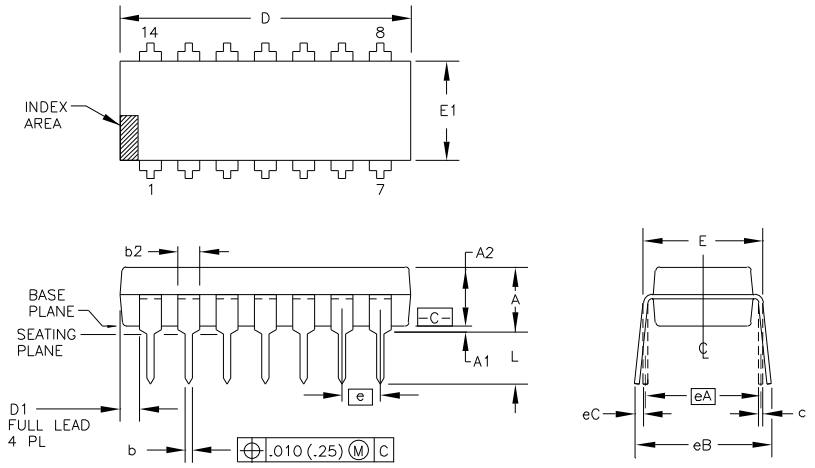


FIGURE 5. Measuring System Temperature.

PACKAGE DRAWING

Package Number 010 - 14-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
c	.008	.014	0.20	0.36	
D	.735	.775	18.67	19.69	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
L	.115	.150	2.92	3.81	3
N	14		14		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ010	REV.: G
JEDEC NUMBER: MS-001-AA	