



REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original	May 3 ,2001
Rev. 1.0	Delete STSOP package	Jul 27,2001
Rev. 1.1	Add STSOP package	Sep 27,2001
Rev. 1.2	Revised STSOP package	Feb 1,2002
Rev. 1.3	Add under/overshoot range of V_{IL} & V_{IH}	Nov 27,2002
Rev. 1.4	Add package 28-pin 300 mil skinny PDIP & Package outline dimension	Jan 10,2003



FEATURES

- Fast access time : 8/10/12/15 ns (max.)
- Low power operating : 80 mA (typical)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 28-pin 300 mil SOJ
28-pin 8mmx13.4mm STSOP
28-pin 300 mil skinny PDIP

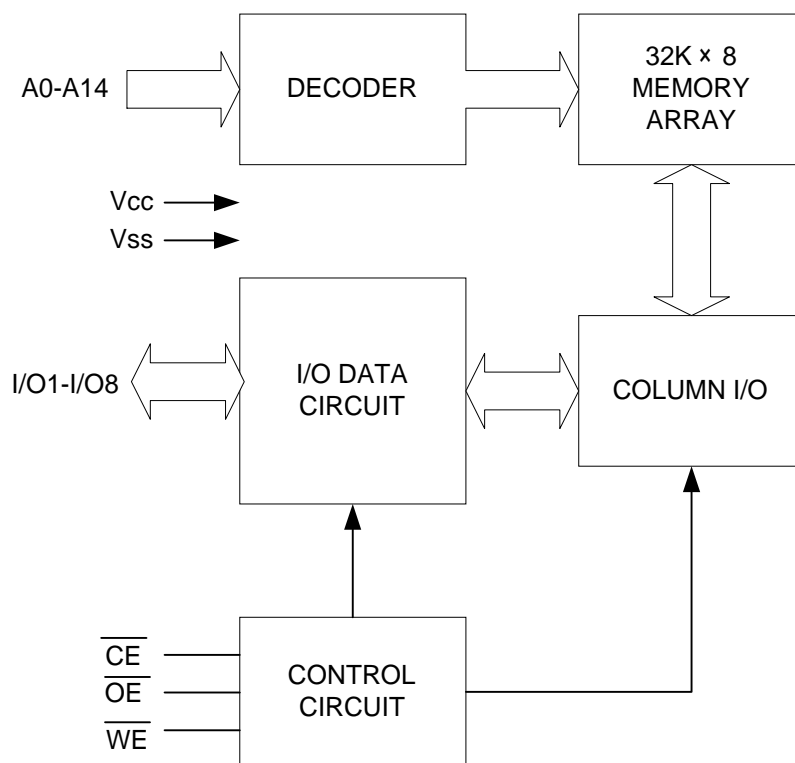
GENERAL DESCRIPTION

The UT61256C is a 262,144-bit high-speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT61256C is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

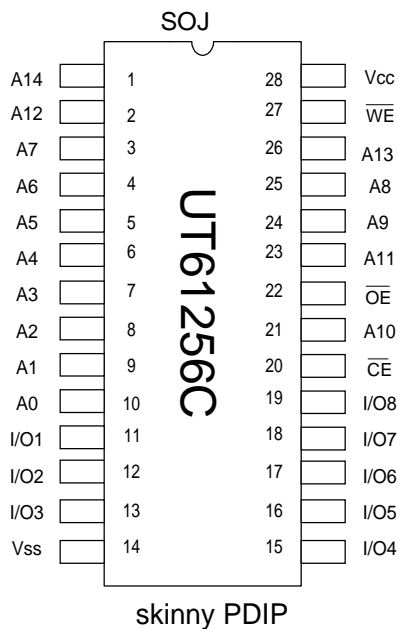
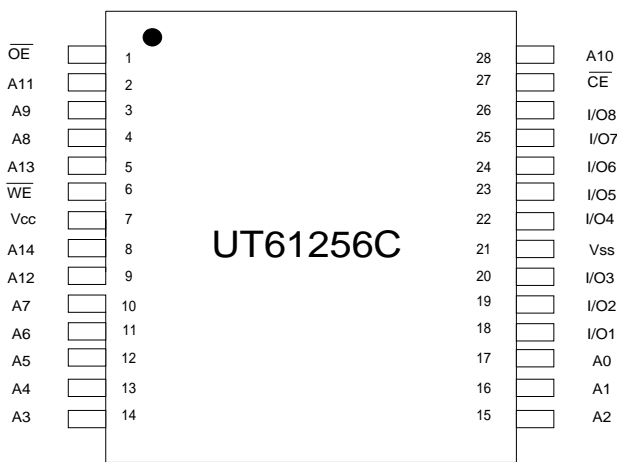
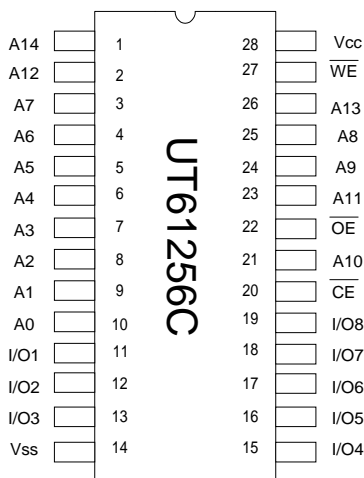
The UT61256C operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground

**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V _{SS}	V _{TERM}	-0.5 to +6.5	V
Operating Temperature	T _A	0 to +70	
Storage Temperature	T _{STG}	-65 to +150	
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA
Soldering Temperature (under 10 sec)	T _{solder}	260	

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High - Z	I _{CC}
Read	L	L	H	D _{OUT}	I _{CC}
Write	L	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to 70 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Input High Voltage	V _{IH}		2.2	V _{CC} +0.5	V
Input Low Voltage	V _{IL}		- 0.5	0.8	V
Input Leakage Current	I _{LI}	V _{SS} V _{IN} V _{CC}	- 1	1	μA
Output Leakage Current	I _{LO}	V _{SS} V _{I/O} V _{CC} $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	- 1	1	μA
Output High Voltage	V _{OH}	I _{OH} = - 4mA	2.4	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	0.4	V
Operating Power Supply Current	I _{CC}	Cycle time=Min. $\overline{CE} = V_{IL}$, I _{I/O} = 0mA	- 8	190	mA
			- 10	180	mA
			- 12	160	mA
			- 15	140	mA
Standby Current (TTL)	I _{SB}	$\overline{CE} = V_{IH}$	-	30	mA
Standby Current (CMOS)	I _{SB1}	$\overline{CE} = V_{CC}-0.2V$	-	5	mA

Notes:

1. Overshoot : V_{CC}+2.0v for pulse width less than 6ns.
2. Undershoot : V_{SS}-2.0v for pulse width less than 6ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

**CAPACITANCE** ($T_A=25$, $f=1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=30\text{pF}$, $I_{OH}/I_{OL}=-4\text{mA}/8\text{mA}$

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_A = 0$ to 70)**(1) READ CYCLE**

PARAMETER	SYMBOL	UT61256C -8		UT61256C -10		UT61256C -12		UT61256C -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ}^*	2	-	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	t_{OLZ}^*	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ}^*	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ}^*	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns

(2) WRITE CYCLE

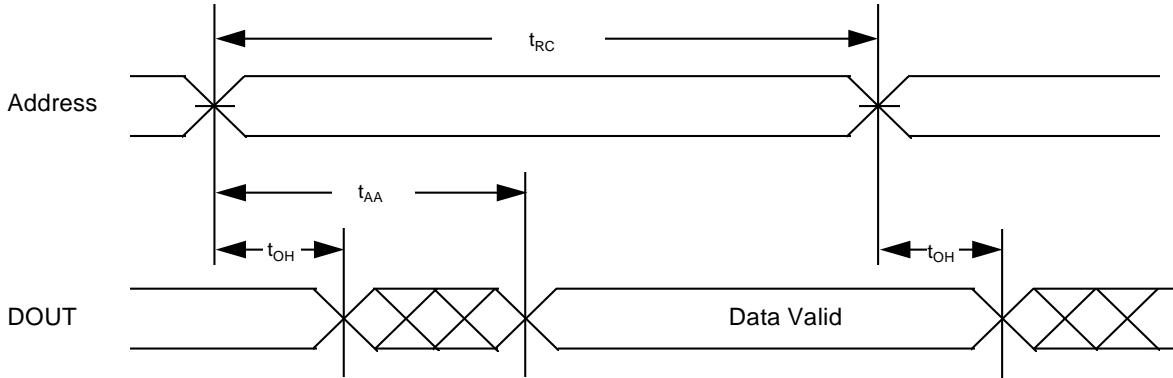
PARAMETER	SYMBOL	UT61256C -8		UT61256C -10		UT61256C -12		UT61256C -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	6.5	-	8	-	10	-	12	-	ns
Chip Enable to End of Write	t_{CW}	6.5	-	8	-	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	6.5	-	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	1.5	-	2	-	3	-	4	-	ns
Write to Output in High Z	t_{WHZ}^*	5	-	6	-	7	-	8	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

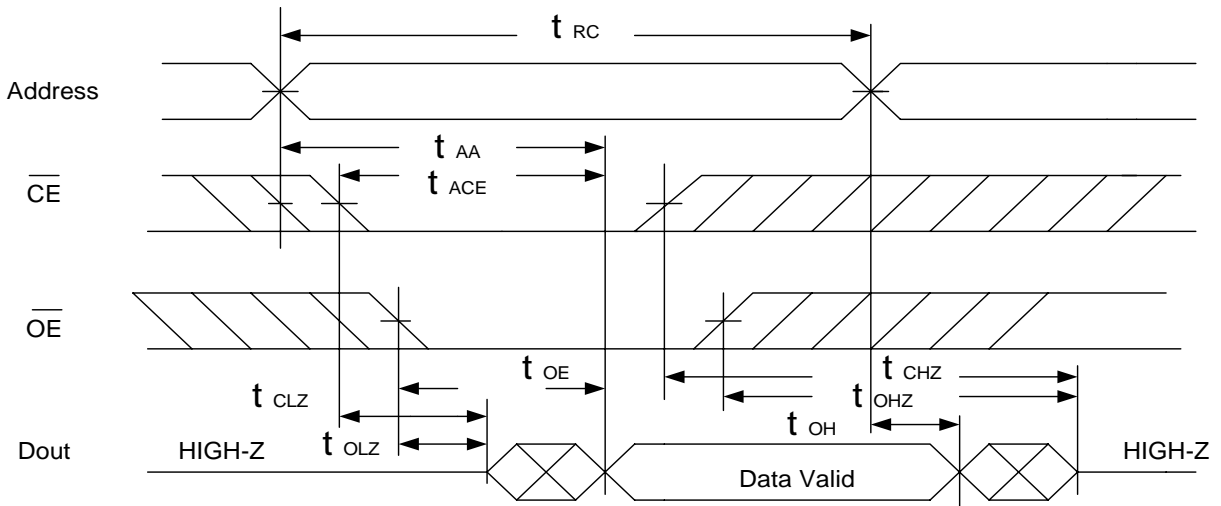


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 (\overline{CE} and \overline{OE} Controlled) (1,3,5,6)

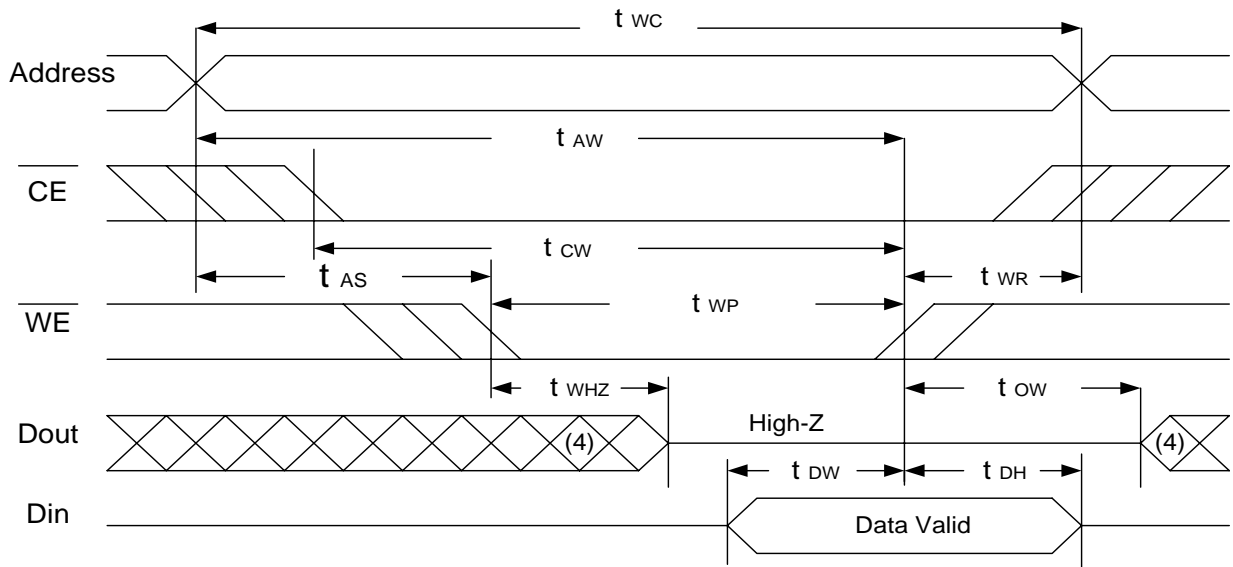


Notes :

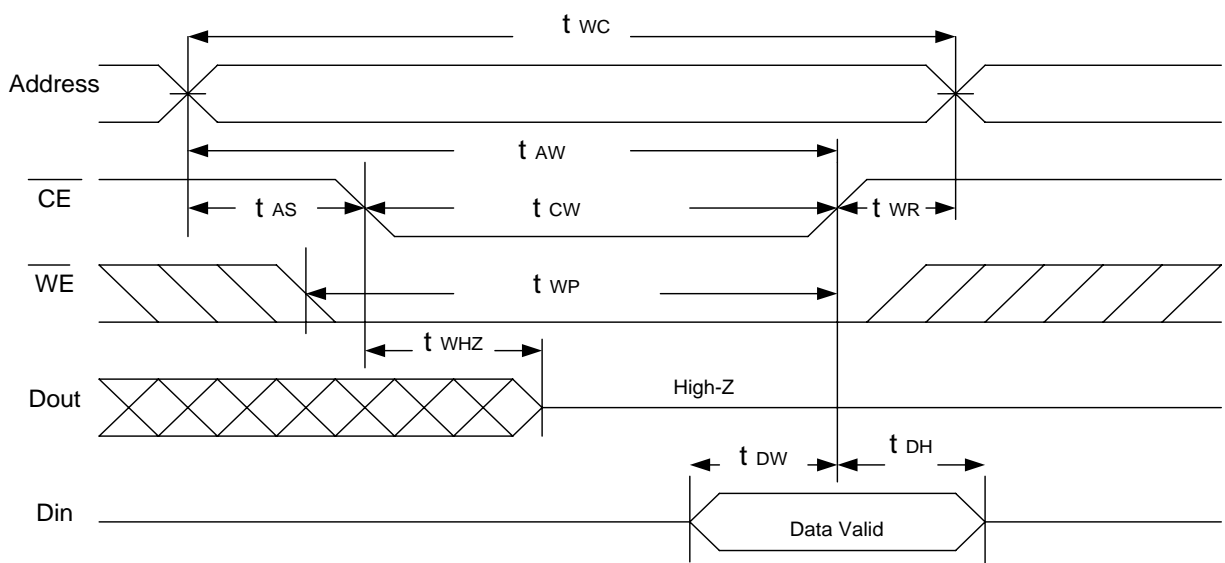
1. \overline{WE} is HIGH for read cycle.
2. Device is continuously selected $\overline{CE} = V_{IL}$.
3. Address must be valid prior to or coincident with \overline{CE} transition; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is LOW.
5. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (\overline{CE} Controlled) (1,2,5)



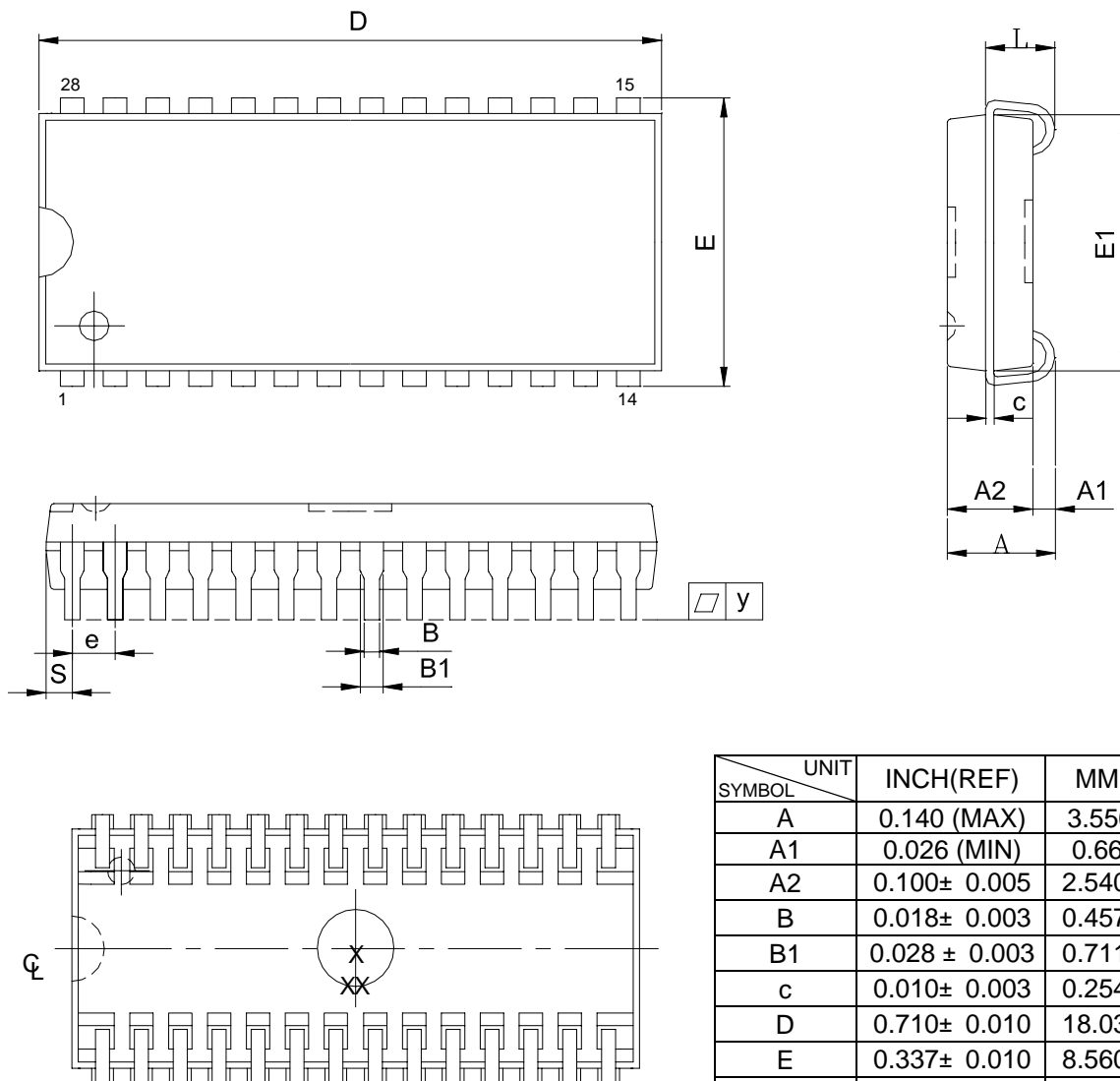
Notes :

1. \overline{WE} and \overline{CE} must be HIGH during all address transitions.
2. A write occurs during the overlap of a low \overline{CE} and a low \overline{WE} .
3. During a \overline{WE} controlled with write cycle with \overline{OE} LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} low transition occurs simultaneously with or after \overline{WE} low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



PACKAGE OUTLINE DIMENSION

28 pin 300 mil SOJ Package Outline Dimension



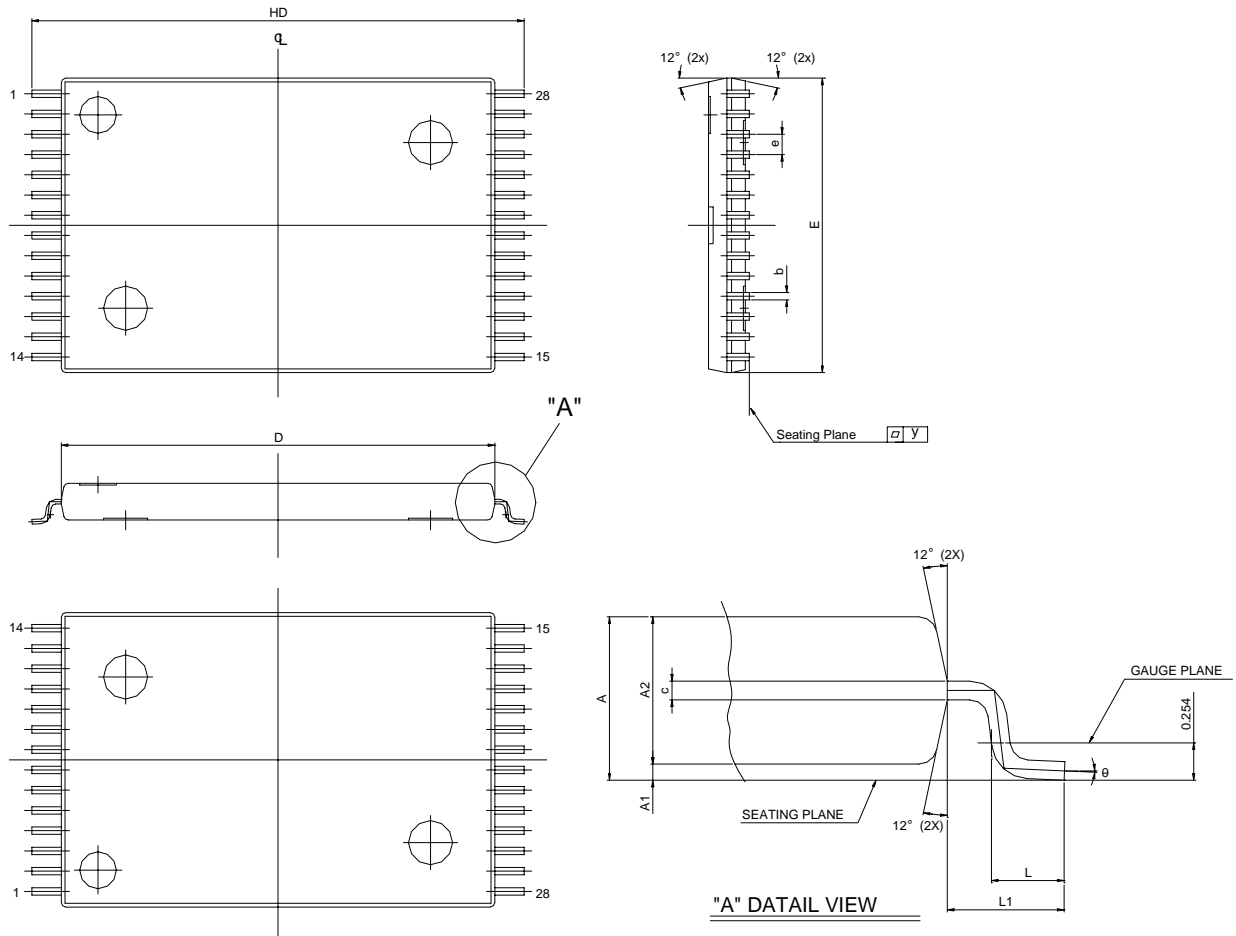
SYMBOL \ UNIT	INCH(REF)	MM(BASE)
A	0.140 (MAX)	3.556 (MAX)
A1	0.026 (MIN)	0.660 (MIN)
A2	0.100± 0.005	2.540± 0.127
B	0.018± 0.003	0.457± 0.076
B1	0.028 ± 0.003	0.711± 0.076
c	0.010± 0.003	0.254± 0.076
D	0.710± 0.010	18.03± 0.254
E	0.337± 0.010	8.560± 0.254
E1	0.300± 0.005	7.620± 0.127
e	0.050± 0.003	1.270± 0.076
L	0.087± 0.010	2.210± 0.254
S	0.030± 0.004	0.762± 0.102
Y	0.003 (MAX)	0.076 (MAX)

Note:

1. S/E/D DIM NOT INCLUDEING MOLD FLASH.
2. THE END FLASH IN PACKAGE LENGTHWISE IS NOT MORE THAN 10 MILS EACH SIDE



28 pin 8x13.4mm STSOP Package Outline Dimension

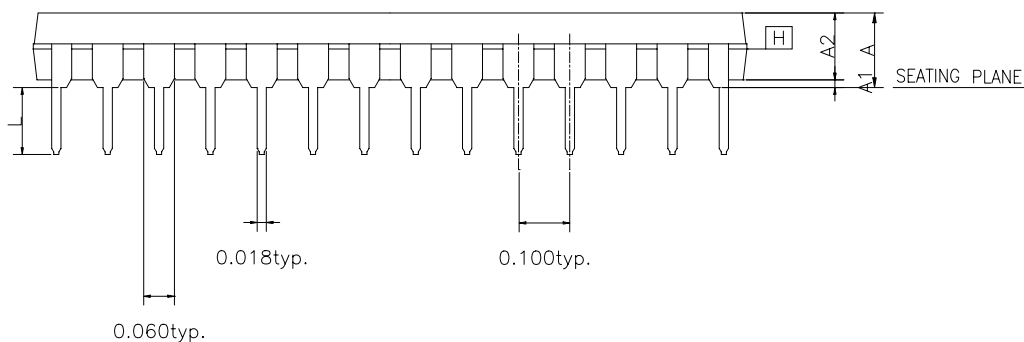
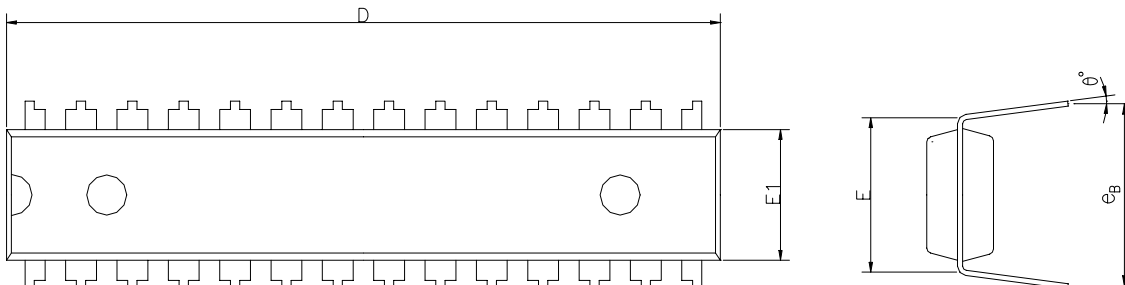


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	0.15	0.20	0.004	0.006	0.008
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
	0°	3°	5°	0°	3°	5°



PACKAGE OUTLINE DIMENSION

28 pin 300 mil skinny PDIP Package Outline Dimension



SYMBOL	UNIT	MIN	NOR.	MAX
A		-	-	0.210
A1		0.015	-	-
A2		0.125	0.130	0.135
D		1.385	1.390	1.400
E		0.310 BSC		
E1		0.283	0.288	0.293
L		0.115	0.130	0.150
eB		0.330	0.350	0.370
°		0	7	15

Note :
1. JEDEC OUTLINE : N / A



ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61256CJC-8	8	28 PIN SOJ
UT61256CJC-10	10	28 PIN SOJ
UT61256CJC-12	12	28 PIN SOJ
UT61256CJC-15	15	28 PIN SOJ
UT61256CLS-8	8	28 PIN STSOP
UT61256CLS-10	10	28 PIN STSOP
UT61256CLS-12	12	28 PIN STSOP
UT61256CLS-15	15	28 PIN STSOP
UT61256CKC-8	8	28 PIN SKINNY PDIP
UT61256CKC-10	10	28 PIN SKINNY PDIP
UT61256CKC-12	12	28 PIN SKINNY PDIP
UT61256CKC-15	15	28 PIN SKINNY PDIP



UTRON

Rev. 1.4

UT61256C
32K X 8 BIT HIGH SPEED CMOS SRAM

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