

Preliminary

TOSHIBA Photocoupler GaAlAs IRED + Photo IC

TLP351

Inverter for Air Conditioner
 IGBT/Power MOS FET Gate Drive
 Industrial Inverter

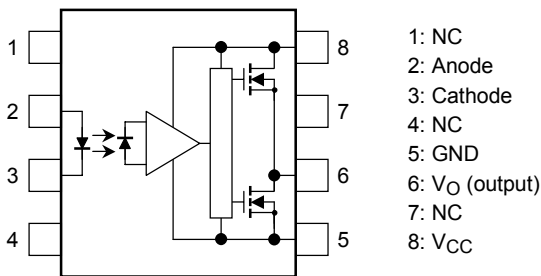
The TOSHIBA TLP351 consists of a GaAlAs light emitting diode and a integrated photodetector.
 This unit is 8-lead DIP package.
 TLP351 is suitable for gate driving circuit of IGBT or power MOS FET.
 Especially TLP351 is capable of "direct" gate drive of lower Power IGBTs.

- Peak output current: ± 0.6 A (max)
- Guaranteed performance over temperature: -40 to 100°C
- Supply current: 2 mA (max)
- Power supply voltage: 10 to 30 V
- Threshold input current : $I_F = 5$ mA (max)
- Switching time (t_{pLH}/t_{pHL}) : 700 ns (max)
- Common mode transient immunity: 10 kV/ μs
- Isolation voltage: 3750 Vrms

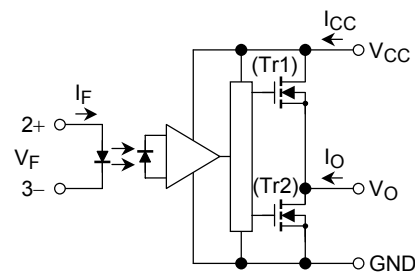
Truth Table

Input	LED	Tr1	Tr2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

Pin Configuration (top view)

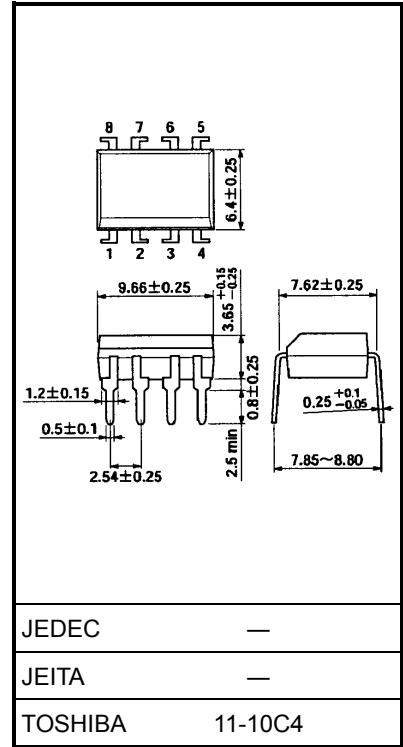


Schematic



A 0.1 μF bypass capacitor must be connected between pin 8 and 5. (See Note 6)

Unit: mm



Weight: 0.54 g (typ.)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I_F	20	mA
	Forward current derating (Ta ≥ 85°C)	$\Delta I_F / \Delta T_a$	-0.54	mA/°C
	Peak transient forward current (Note 1)	I_{FP}	1	A
	Reverse voltage	V_R	5	V
	Junction temperature	T_j	125	°C
Detector	“H” peak output current (Note 2)	I_{OPH}	-0.6	A
	“L” peak output current (Note 2)	I_{OPL}	0.6	A
	Output voltage	V_O	35	V
	Supply voltage	V_{CC}	35	V
	Junction temperature	T_j	125	°C
Operating frequency (Note 3)	f	25	kHz	
Storage temperature range	T_{stg}	-55 to 125	°C	
Operating temperature range	T_{opr}	-40 to 100	°C	
Lead soldering temperature (10 s) (Note 4)	T_{sol}	260	°C	
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 5)	BV_S	3750	Vrms	

Note 1: Pulse width $P_W \leq 1 \mu s$, 300 pps

Note 2: Exponential waveform pulse width $P_W \leq 10 \mu s$, $f \leq 15 \text{ kHz}$

Note 3: Exponential waveform $I_{OPH} \leq -0.4 \text{ A}$ ($\leq 2.0 \mu s$), $I_{OPL} \leq +0.4 \text{ A}$ ($\leq 2.0 \mu s$), $T_a = 100^\circ\text{C}$

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 6: A ceramic capacitor(0.1 μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 7)	$I_F (ON)$	7.5	—	10	mA
Input voltage, OFF	$V_F (OFF)$	0	—	0.8	V
Supply voltage	V_{CC}	10	—	30	V
Peak output current	I_{OPH}/I_{OPL}	—	—	± 0.2	A
Operating temperature	T_{opr}	-40	—	100	°C

Note 7: Input signal rise time (fall time) < 0.5 μs .

Electrical Characteristics (Ta = -40 to 100°C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Forward voltage		V_F	—	$I_F = 5 \text{ mA}$, $T_a = 25^\circ\text{C}$	—	1.55	1.70	V	
Temperature coefficient of forward voltage		$\Delta V_F / \Delta T_a$	—	$I_F = 5 \text{ mA}$	—	-2.0	—	mV/°C	
Input reverse current		I_R	—	$V_R = 5 \text{ V}$, $T_a = 25^\circ\text{C}$	—	—	10	μA	
Input capacitance		C_T	—	$V = 0$, $f = 1 \text{ MHz}$, $T_a = 25^\circ\text{C}$	—	45	—	pF	
Output current (Note 8)	"H" Level	I_{OPH1}	1	$V_{CC} = 15 \text{ V}$ $I_F = 5 \text{ mA}$	$V_{8-6} = 4 \text{ V}$	-0.2	-0.4	—	A
		I_{OPH2}			$V_{8-6} = 10 \text{ V}$	-0.4	-0.67		
	"L" Level	I_{OPL1}	2	$V_{CC} = 15 \text{ V}$ $I_F = 0 \text{ mA}$	$V_{6-5} = 2 \text{ V}$	0.2	0.35	—	
		I_{OPL2}			$V_{6-5} = 10 \text{ V}$	0.4	0.63	—	
Output voltage	"H" Level	V_{OH}	3	$V_{CC} = 10 \text{ V}$	$I_O = -100 \text{ mA}$, $I_F = 5 \text{ mA}$	6.0	8.5	—	V
	"L" Level	V_{OL}				4	$I_O = 100 \text{ mA}$, $V_F = 0.8 \text{ V}$	—	
Supply current	"H" Level	I_{CCH}	5	$V_{CC} = 10 \text{ to } 30 \text{ V}$ V_O open	$I_F = 10 \text{ mA}$			—	1.4
	"L" Level	I_{CCL}				6	$I_F = 0 \text{ mA}$	—	1.3
Threshold input current	L → H	I_{FLH}	—	$V_{CC} = 15 \text{ V}$, $V_O > 1 \text{ V}$	—			2.5	5
Threshold input voltage	H → L	V_{FHL}	—	$V_{CC} = 15 \text{ V}$, $V_O < 1 \text{ V}$	0.8	—	—	V	
Supply voltage		V_{CC}	—	—	10	—	30	V	
Capacitance (Input-Output)		C_S	—	$V = 0$, $f = 1 \text{ MHz}$, $T_a = 25^\circ\text{C}$	—	1.0	—	pF	
Resistance (Input-Output)		R_S	—	$V_S = 500 \text{ V}$, $T_a = 25^\circ\text{C}$, R.H. ≤ 60%	1×10^{12}	10^{14}	—	Ω	

*: All typical values are at $T_a = 25^\circ\text{C}$

Note 8: Duration of I_O time ≤ 50 μs

Note 9: This product is more sensitive than the conventional product to static electricity (ESD) because of a lowest power consumption design.

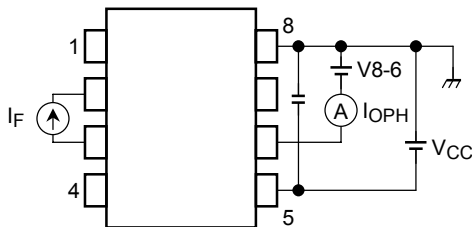
General precaution to static electricity (ESD) is necessary for handling this component.

Switching Characteristics (Ta = -40 to 100°C, unless otherwise specified)

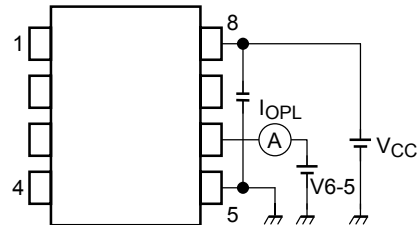
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Propagation delay time	L → H	7	V _{CC} = 30 V R _g = 47 Ω C _g = 3 nF	I _F = 0 → 5 mA	100	—	700	ns
	H → L			I _F = 5 → 0 mA	100	—	700	
Propagation delay difference between any two parts or channels	PDD t _{pHL} - t _{pLH}	7	V _{CC} = 30 V, R _g = 47 Ω, C _g = 3 nF	-500	—	500	ns	
Output rise time (10-90%)	t _r	7	V _{CC} = 30 V R _g = 47 Ω C _g = 3 nF	I _F = 0 → 5 mA	—	50	—	ns
Output fall time (90-10%)	t _f			I _F = 5 → 0 mA	—	50	—	
Common mode transient immunity at high level output	CM _H	8	V _{CM} = 1000 V _{p-p} Ta = 25°C V _{CC} = 30 V	I _F = 5 mA V _O (min) = 26 V	-10000	—	—	V/μs
Common mode transient immunity at low level output	CM _L			I _F = 0 mA V _O (max) = 1 V	10000	—	—	

*: All typical values are at Ta = 25°C

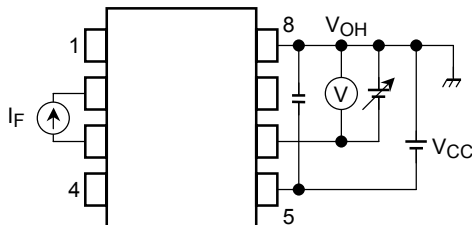
Test Circuit 1: I_{OPH}



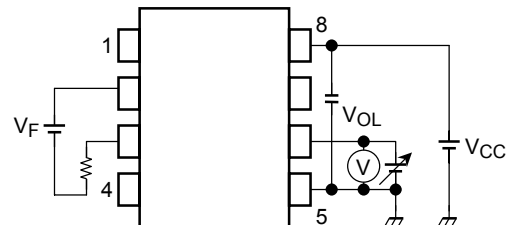
Test Circuit 2: I_{OPL}



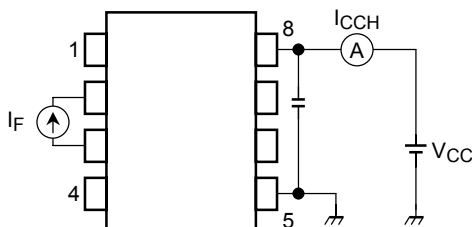
Test Circuit 3: V_{OH}



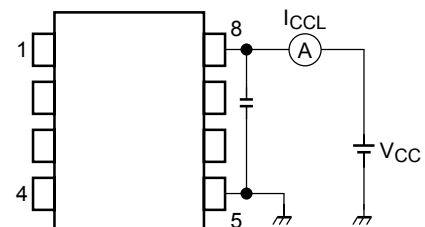
Test Circuit 4: V_{OL}



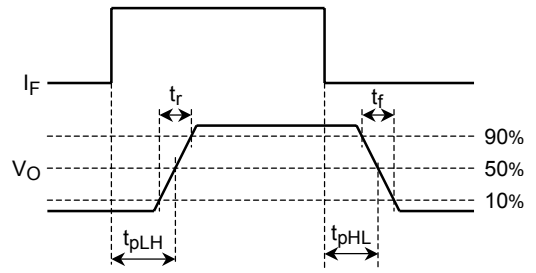
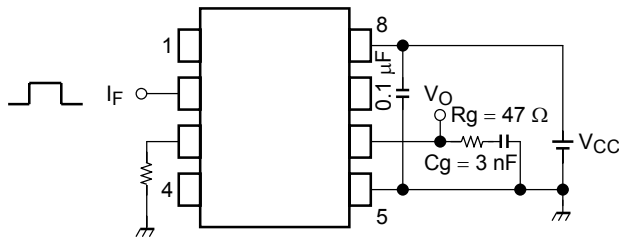
Test Circuit 5: I_{CCH}



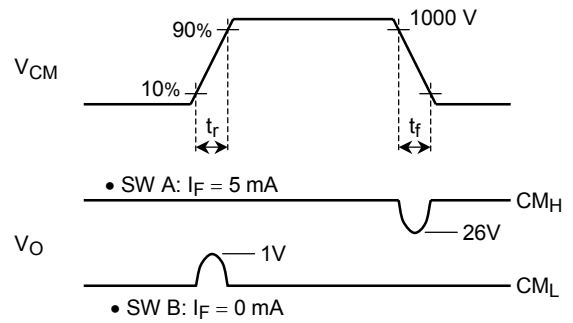
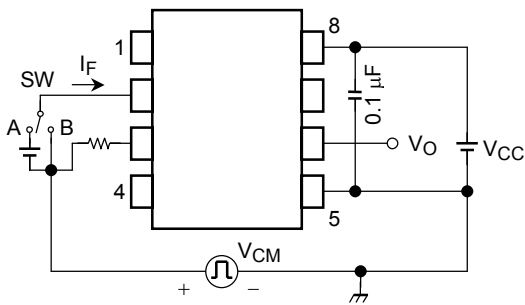
Test Circuit 6: I_{CCL}



Test Circuit 7: t_{pLH} , t_{pHL} , t_r , t_f , PDD



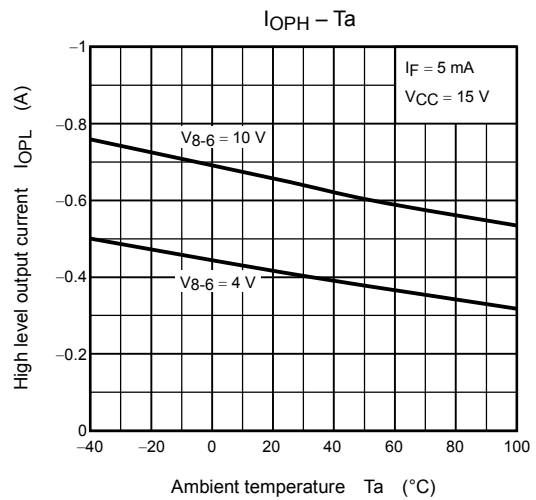
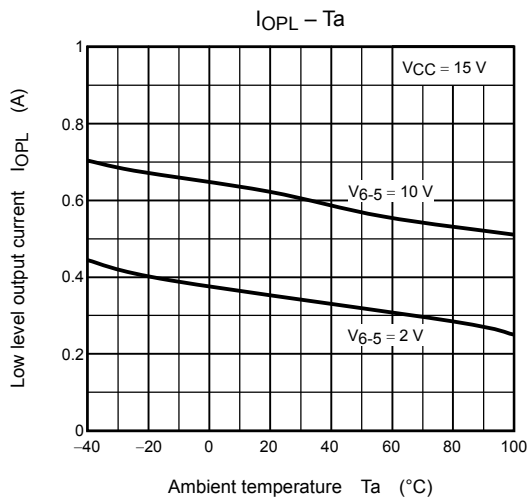
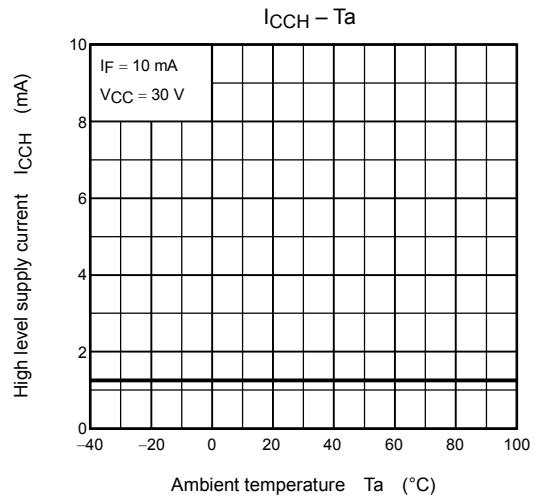
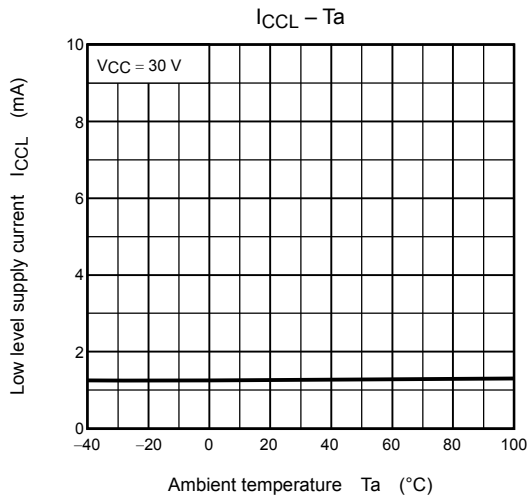
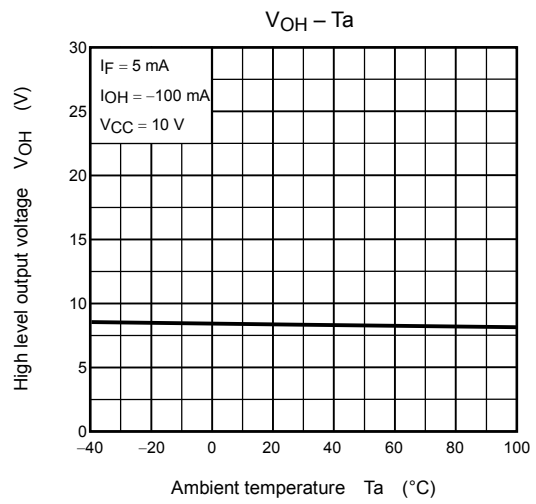
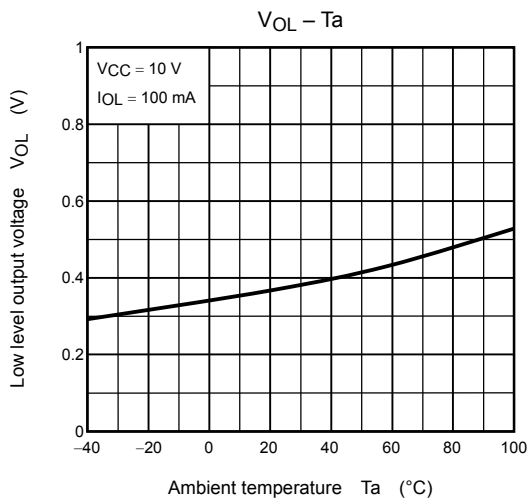
Test Circuit 8: CM_H , CM_L



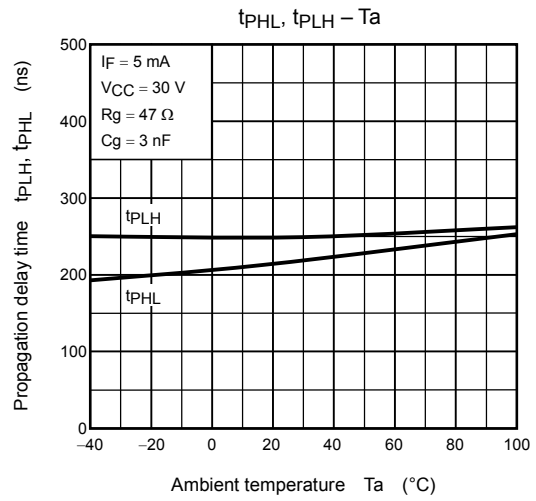
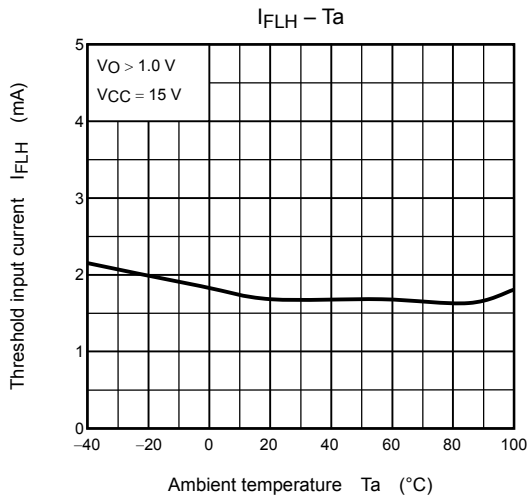
$$CM_L = \frac{800 \text{ V}}{t_f (\mu\text{s})}$$

$$CM_H = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.



*: The above graphs show typical characteristics.



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