

DATA SHEET

TDA8787

**10-bit, 3.0 V analog-to-digital
interface for CCD cameras**

Preliminary specification
Supersedes data of 1998 Mar 27
File under Integrated Circuits, IC02

1998 Oct 15

10-bit, 3.0 V analog-to-digital interface for CCD cameras

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FEATURES

- Correlated Double Sampling (CDS), Automatic Gain Control (AGC), 10-bit Analog-to-Digital Converter (ADC) and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- AGC gain range of 36 dB (in steps of 0.1 dB)
- Low power consumption of only 190 mW (typ.)
- Power consumption in standby mode of 4.5 mW (typ.)
- 3.0 V operation and 2.5 to 3.6 V operation for the digital outputs
- Active control pulses polarity selectable via serial interface
- 8-bit DAC included for analog settings
- TTL compatible inputs, CMOS compatible outputs.

APPLICATIONS

- Low-power, low-voltage CCD camera systems.

GENERAL DESCRIPTION

The TDA8787 is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC and a low-power 10-bit ADC together with its reference voltage regulator.

AGC gain is controlled via the serial interface.

The ADC input clamp level is controlled via the serial interface.

An additional DAC is provided for additional system controls; its output voltage range is 1.0 V (p-p) which is available at pin OFDOUT.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	3.6	V
I_{CCA}	analog supply current	all clamps active	–	55	70	mA
I_{CCD}	digital supply current		–	8	11	mA
I_{CCO}	digital outputs supply current	$f_{pix} = 18$ MHz; $C_L = 20$ pF; input ramp response time is 800 μ s	–	1	2	mA
ADC_{res}	ADC resolution		–	10	–	bits
$V_{i(CDS)(p-p)}$	maximum CDS input voltage (peak-to-peak value)	$V_{CC} = 2.85$ V	650	–	–	mV
		$V_{CC} \geq 3.0$ V	800	–	–	mV
$f_{pix(max)}$	maximum pixel rate		18	–	–	MHz
$f_{pix(min)}$	minimum pixel rate		5	–	–	MHz
DR_{AGC}	AGC dynamic range		–	36	–	dB
$N_{tot(rms)}$	total noise from CDS input to ADC output	AGC gain = 0 dB; see Fig.8	–	0.25	–	LSB
P_{tot}	total power consumption	$V_{CCA} = V_{CCD} = V_{CCO} = 3$ V	–	190	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8787HL	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

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BLOCK DIAGRAM

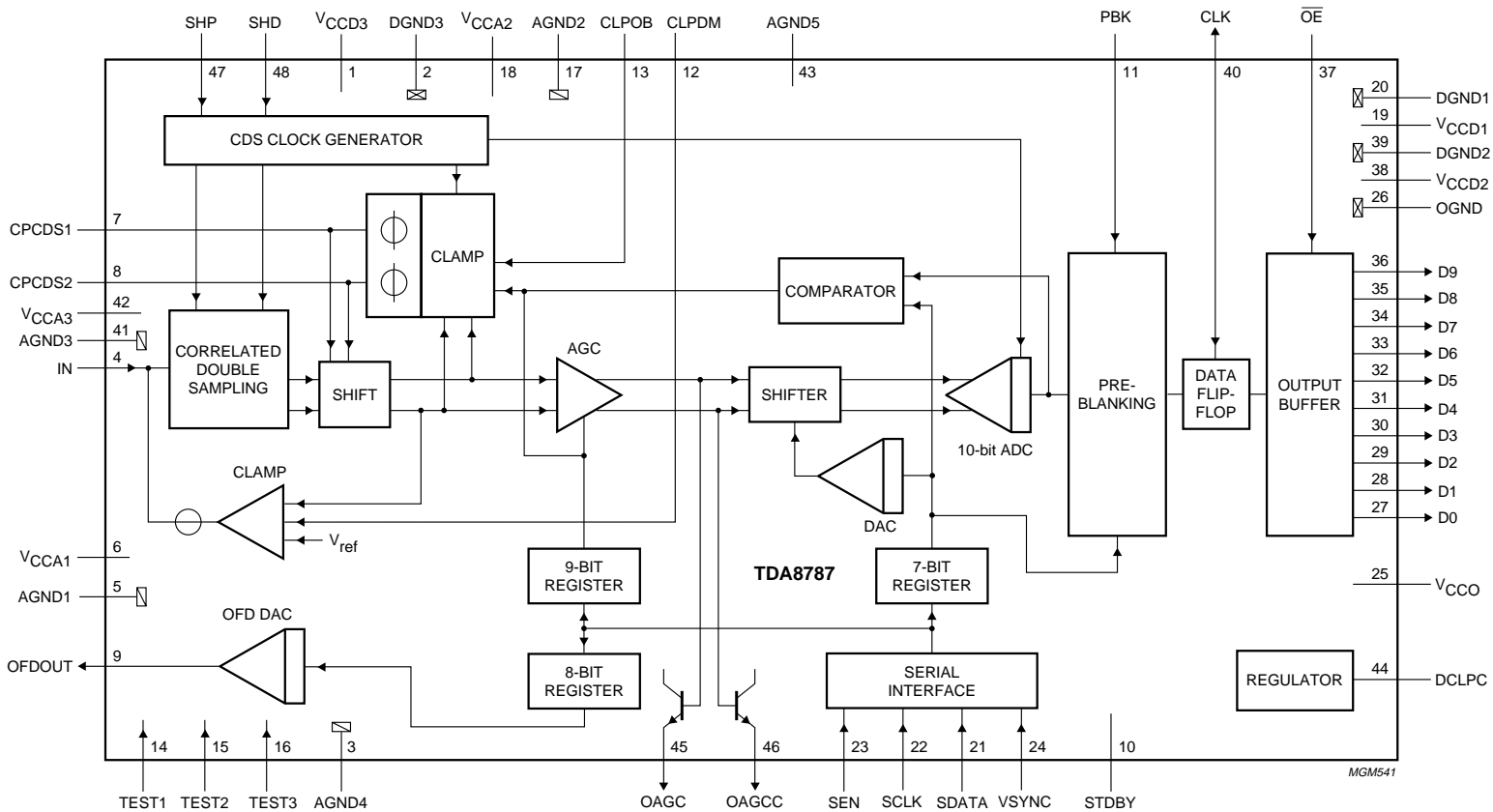


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
V _{CCD3}	1	digital supply voltage 3
DGND3	2	digital ground 3
AGND4	3	analog ground 4
IN	4	input signal from CCD
AGND1	5	analog ground 1
V _{CCA1}	6	analog supply voltage 1
CPCDS1	7	clamp storage capacitor pin 1
CPCDS2	8	clamp storage capacitor pin 2
OFDOUT	9	analog output of the additional 8-bit control DAC
STDBY	10	standby mode control input (LOW: TDA8787 active; HIGH: TDA8787 standby)
PBK	11	pre-blanking control input
CLPDM	12	clamp pulse input at dummy pixel
CLPOB	13	clamp pulse input at optical black
TEST1	14	test pin input 1 (should be connected to AGND2)
TEST2	15	test pin input 2 (should be connected to AGND1)
TEST3	16	test pin input 3 (should be connected to AGND2)
AGND2	17	analog ground 2
V _{CCA2}	18	analog supply voltage 2
V _{CCD1}	19	digital supply voltage 1
DGND1	20	digital ground 1
SDATA	21	serial data input for serial interface control
SCLK	22	serial clock input for serial interface
SEN	23	strobe pin for serial interface
VSYNC	24	vertical sync pulse input
V _{CCO}	25	output supply voltage
OGND	26	digital output ground
D0	27	ADC digital output 0 (LSB)
D1	28	ADC digital output 1
D2	29	ADC digital output 2
D3	30	ADC digital output 3
D4	31	ADC digital output 4
D5	32	ADC digital output 5
D6	33	ADC digital output 6
D7	34	ADC digital output 7
D8	35	ADC digital output 8
D9	36	ADC digital output 9 (MSB)
OE	37	output enable control input (LOW: outputs active; HIGH: outputs in high impedance)
V _{CCD2}	38	digital supply 2
DGND2	39	digital ground 2
CLK	40	data clock input

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SYMBOL	PIN	DESCRIPTION
AGND3	41	analog ground 3
VCCA3	42	analog supply 3
AGND5	43	analog ground 5
DCLPC	44	regulator decoupling pin
OAGC	45	AGC output (test pin)
OAGCC	46	AGC complementary output (test pin)
SHP	47	preset sample-and-hold pulse input
SHD	48	data sample-and-hold pulse input

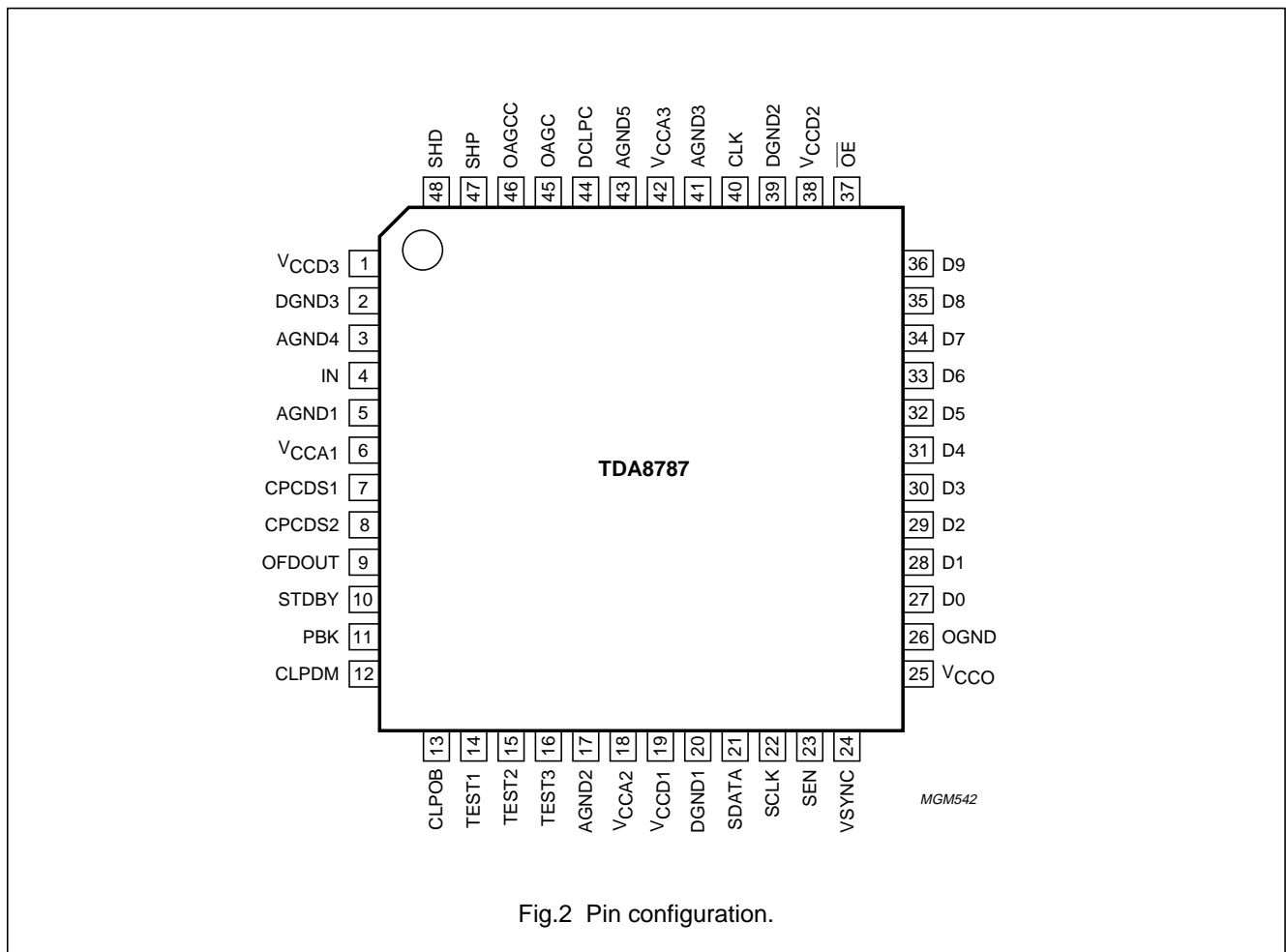


Fig.2 Pin configuration.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	-0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	-0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	-0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}		-1.0	+1.0	V
	between V_{CCA} and V_{CCO}		-1.0	+1.0	V
	between V_{CCD} and V_{CCO}		-1.0	+1.0	V
V_i	input voltage	referenced to AGND	-0.3	+7.0	V
I_o	data output current		-	± 10	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		-20	+75	°C
T_j	junction temperature		-	150	°C

Note

- The supply voltages V_{CCA} , V_{CCD} and V_{CCO} may have any value between -0.3 and +7.0 V provided that the supply voltage difference ΔV_{CC} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	76	K/W

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CHARACTERISTICS
 $V_{CCA} = V_{CCD} = 3.0\text{ V}$; $V_{CCO} = 2.6\text{ V}$; $f_{\text{pix}} = 18\text{ MHz}$; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	3.6	V
I_{CCA}	analog supply current	all clamps active	–	55	70	mA
I_{CCD}	digital supply current		–	8	11	mA
I_{CCO}	digital outputs supply current	$C_L = 20\text{ pF}$ on all data outputs; input ramp frequency	–	1	2	mA
Digital inputs						
INPUTS: SHP, SHD, STDBY, CLPDM, CLPOB, SCLK, SDATA, SEN, $\overline{VS\text{ync}}$, \overline{OE} AND PBK						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.2	–	V_{CCD}	V
I_i	input current	$0 \leq V_i \leq V_{CCD}$	–2	–	+2	μA
Clamps						
GLOBAL CHARACTERISTICS OF THE CLAMP LOOPS						
$t_{W(\text{clamp})}$	clamp active pulse width in number of pixels	AGC code = 383 for maximum 4 LSB error	18	–	–	pixels
INPUT CLAMP (DRIVEN BY CLPDM)						
$g_{m(\text{CDS})}$	CDS input clamp transconductance		1.5	2.7	3.5	mS
OPTICAL BLACK CLAMP (DRIVEN BY CLPOB)						
G_{shift}	gain from CPCDS1 and 2 to AGC inputs		–	0.27	–	–
$I_{\text{LSB}(\text{cp})}$	charge pump current for ± 1 LSB error at ADC output	AGC code = 0	–	± 350	–	μA
		AGC code = 383	–	± 10	–	μA
$I_{\text{push}(\text{cp})}$	available push current of the charge pump		–	650	–	μA
$I_{\text{pull}(\text{cp})}$	available pull current of the charge pump		–	–650	–	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Correlated Double Sampling (CDS)						
$V_{i(\text{CDS})(\text{p-p})}$	maximum peak-to-peak CDS input amplitude (video signal)	$V_{\text{CC}} = 2.85 \text{ V}$	650	–	–	mV
		$V_{\text{CC}} \geq 3.0 \text{ V}$	800	–	–	mV
$V_{\text{reset}(\text{max})}$	maximum CDS input reset pulse amplitude		500	–	–	mV
$I_{i(\text{IN})}$	input current into pin IN (pin 4)	at floating gate level	–1	–	+1	μA
$t_{\text{CDS}(\text{min})}$	CDS control pulses minimum active time	video input = $V_{i(\text{CDS})(\text{p-p})}$; 2 LSB error at ADC output	11	15	–	ns
$t_{\text{h}(\text{IN-SHP})}$	CDS input hold time (pin IN) compared to control pulse SHP	$V_{\text{CCA}} = V_{\text{CCD}} = 30 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; see Fig.9	3	5	7	ns
$t_{\text{h}(\text{IN-SHD})}$	CDS input hold time (pin IN) compared to control pulse SHD	$V_{\text{CCA}} = V_{\text{CCD}} = 30 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; see Fig.9	3	5	7	ns
Amplifier						
DR_{AGC}	AGC dynamic range		–	36	–	dB
$\Delta\text{G}_{\text{AGC}}$	maximum AGC gain step		–0.3	–	+0.3	dB
Analog-to-Digital Converter (ADC)						
LE_i	integral linearity error	$f_{\text{pix}} = 18 \text{ MHz}$; ramp input	–	± 1.3	± 2.5	LSB
LE_d	differential linearity error	$f_{\text{pix}} = 18 \text{ MHz}$; ramp input	–	± 0.5	± 0.9	LSB
Total chain characteristics (CDS + AGC + ADC)						
$f_{\text{pix}(\text{max})}$	maximum pixel frequency		18	–	–	MHz
t_{CLKH}	CLK pulse width HIGH		15	–	–	ns
t_{CLKL}	CLK pulse width LOW		15	–	–	ns
$t_{\text{d}(\text{SHD-CLK})}$	time delay between SHD and CLK	see Fig.9	10	–	–	ns
$t_{\text{su}(\text{PBK-CLK})}$	set-up time of PBK compared to CLK		10	–	–	ns
$V_{i(\text{IN})}$	video input dynamic signal for ADC full-scale output	AGC code = 00	800	–	–	mV
		AGC code = 383	12.7	–	–	mV
$N_{\text{tot}(\text{rms})}$	total output noise (RMS value)	see Fig.8				
		AGC gain = 0 dB	–	0.25	–	LSB
		AGC gain = 9 dB	–	0.8	–	LSB
$O_{\text{CCD}(\text{max})}$	maximum offset between CCD floating level and CCD dark pixel level		–70	–	+70	mV
$V_{n(i)(\text{eq})}(\text{rms})$	equivalent input noise voltage (RMS value)		–	110	–	μV

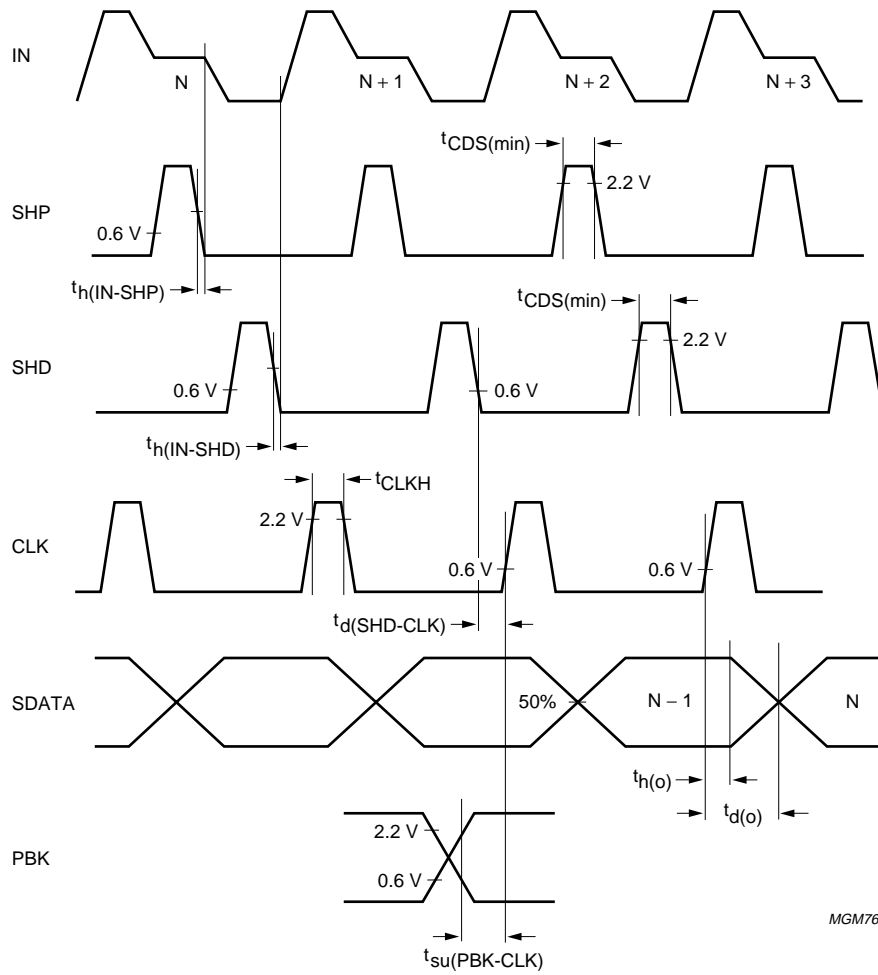
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-analog converter (OFDOUT DAC)						
$V_{\text{OFDOUT}(p-p)}$	additional 8-bit control DAC (OFD) output voltage (peak-to-peak value)	$R_i = 1 \text{ M}\Omega$	–	1.0	–	V
$V_{\text{OFDOUT}(0)}$	DC output voltage for code 0		–	AGND	–	V
$V_{\text{OFDOUT}(255)}$	DC output voltage for code 255		–	AGND + 1.0	–	V
T_{CDAC}	DAC output range temperature coefficient		–	250	–	ppm/°C
Z_{OFDOUT}	DAC output impedance		–	2000	–	Ω
I_{OFDOUT}	OFD output current drive	static	–	–	100	μA
Digital outputs ($f_{\text{pix}} = 18 \text{ MHz}$; $C_L = 22 \text{ pF}$)						
V_{OH}	HIGH-level output voltage	$I_{\text{OH}} = -1 \text{ mA}$	$V_{\text{CCO}} - 0.5$	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	$I_{\text{OL}} = 1 \text{ mA}$	0	–	0.5	V
I_{OZ}	output current in 3-state mode	$0.5 \text{ V} < V_o < V_{\text{CCO}}$	–20	–	+20	μA
$t_{\text{h}(o)}$	output hold time	see Fig.9	11	–	–	ns
$t_{\text{d}(o)}$	output delay time	$C_L = 22 \text{ pF}$; $V_{\text{CCO}} = 3.0 \text{ V}$	–	28	tbf	ns
		$C_L = 22 \text{ pF}$; $V_{\text{CCO}} = 2.7 \text{ V}$	–	27	tbf	ns
C_L	output load capacitance		–	–	22	pF
Serial interface						
$f_{\text{SCLK}(\text{max})}$	maximum frequency of serial interface		5	–	–	MHz

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Fig.3 Pixel frequency timing diagram; all polarities active HIGH.

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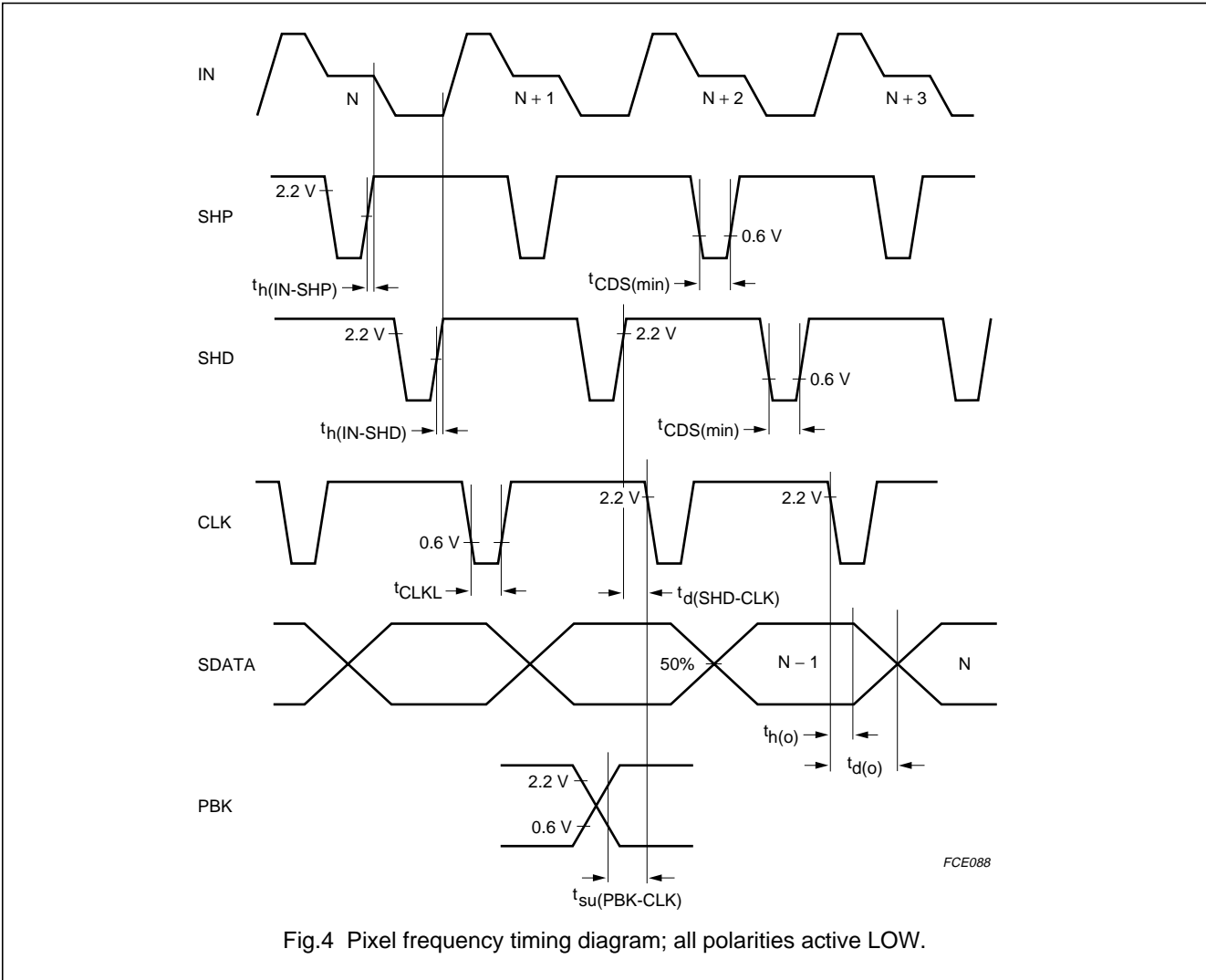


Fig.4 Pixel frequency timing diagram; all polarities active LOW.

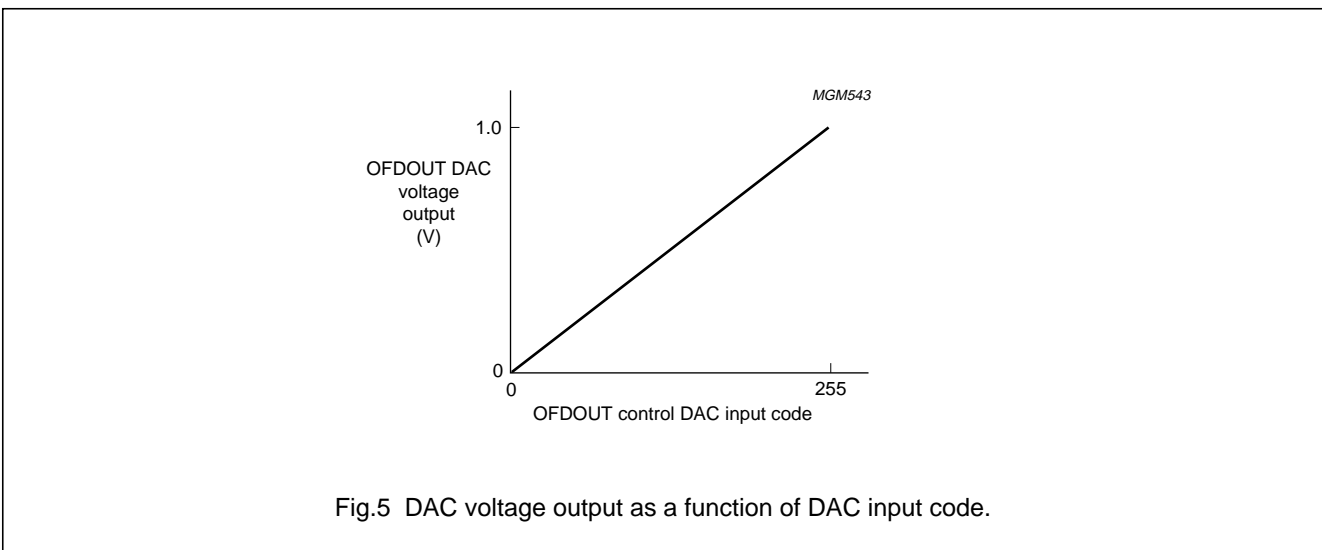
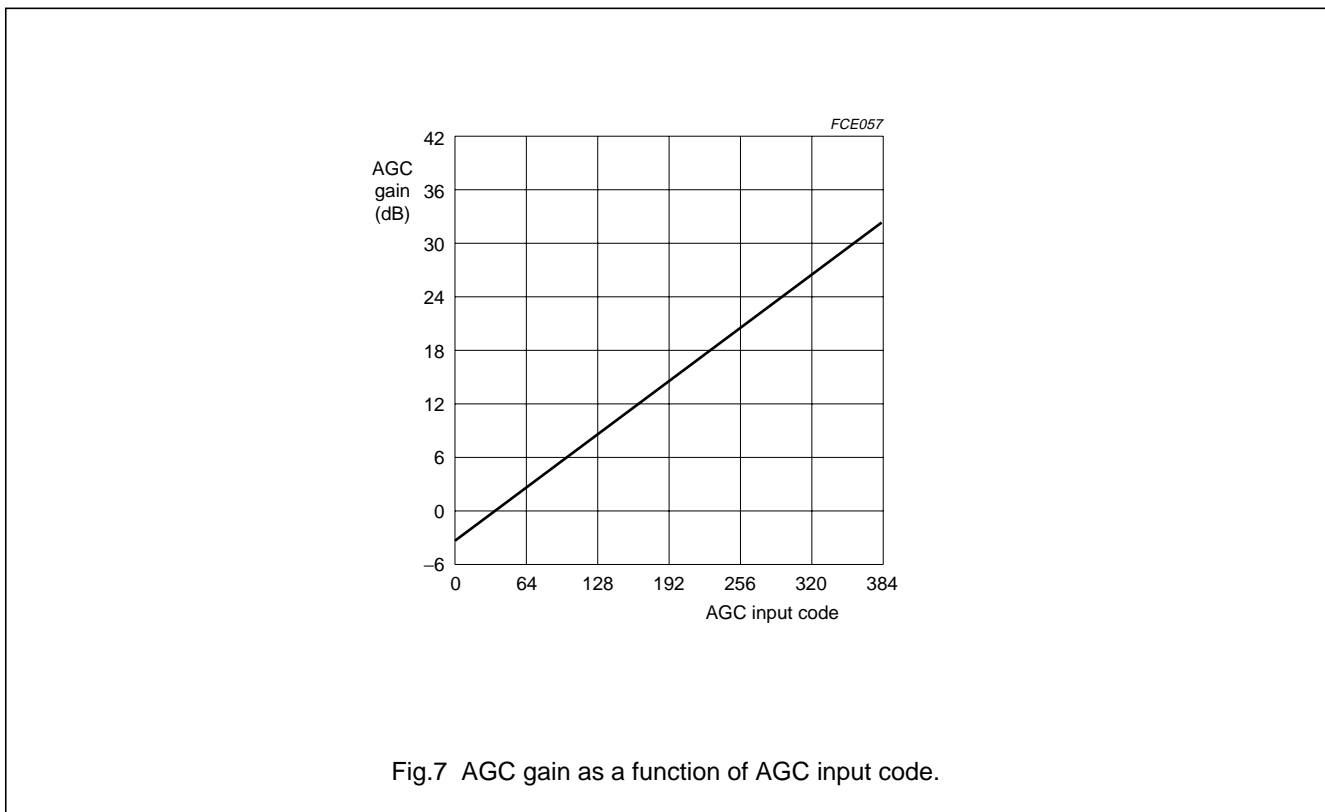
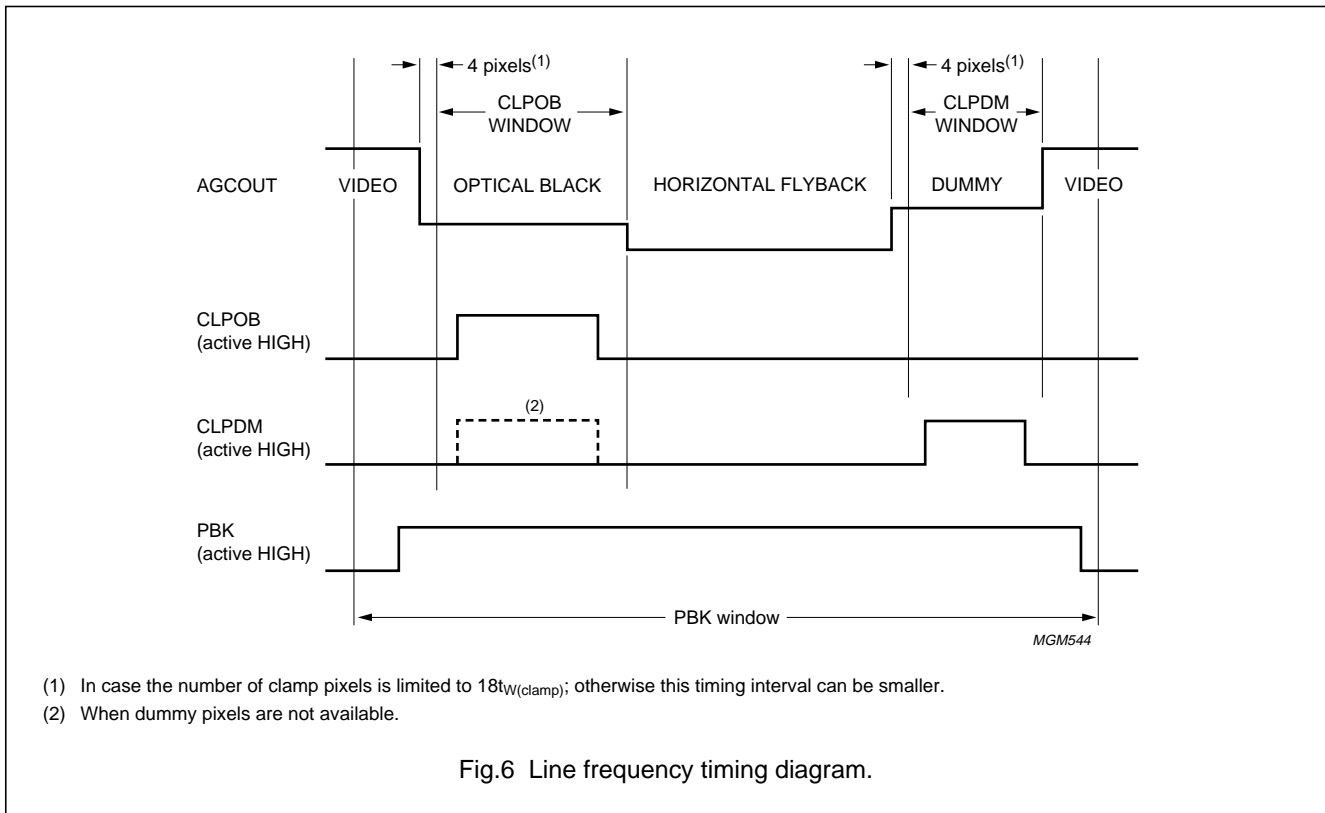


Fig.5 DAC voltage output as a function of DAC input code.

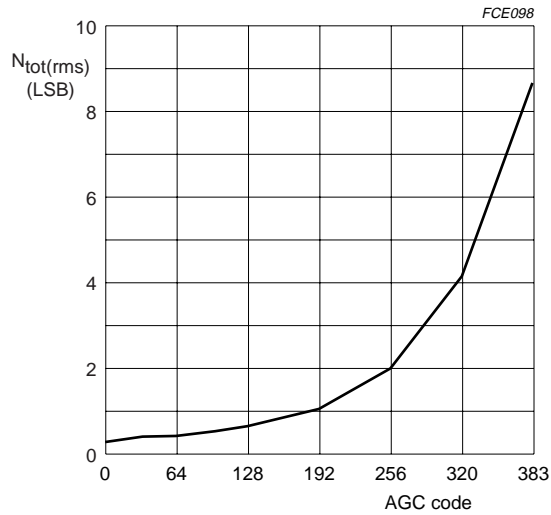
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Noise measurement at ADC outputs:

Coupling capacitor at input is grounded, so only noise contribution of the front-end is evaluated. Front-end works at 18 Mpixels with line of 1024 pixels whose first 40 are used to run CLPOB and the last 40 for CLPDM. Data at the ADC outputs are measured during the other pixels. As a result of this, the standard deviation of the codes statistic is computed, resulting in the noise. No quantization noise is taken into account as no signal is inputted.

Fig.8 Total noise performance as a function of AGC gain.

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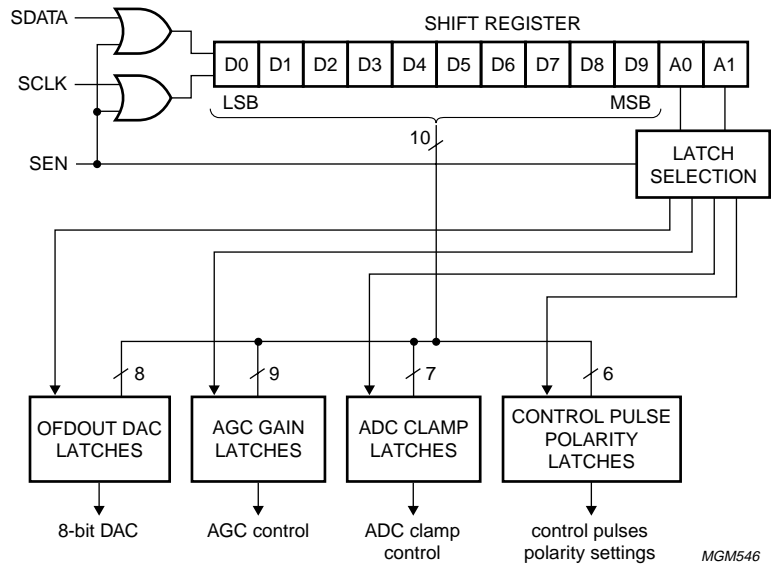
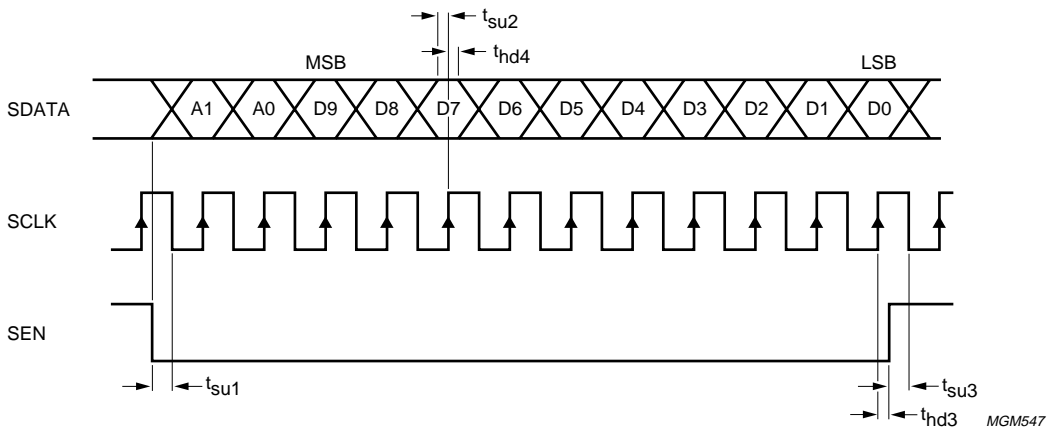


Fig.9 Serial interface block diagram.



$t_{su1} = t_{su2} = t_{su3} = 10 \text{ ns (min.)}$; $t_{hd3} = t_{hd4} = 10 \text{ ns (min.)}$.

Fig.10 Loading sequence of control input data via the serial interface.

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Table 1 Serial interface programming

ADDRESS BITS		DATA BITS D9 TO D0
A1	A0	
0	0	AGC gain control (D8 to D0); bit D9 should be set to logic 0
0	1	DAC OFDOUT output control (D7 to D0); bits D8 and D9 should be set to logic 0
1	0	ADC clamp reference control (D6 to D0); bits D7, D8 and D9 should be set to logic 0
1	1	control pulses (pins SHP, SHD, CLPDM, CLPOB, PBK and CLK) polarity settings

Table 2 Polarity settings

SYMBOL	PIN	SERIAL CONTROL BIT ⁽¹⁾	ACTIVE EDGE OR LEVEL
SHP and SHD	47 and 48	D0	1 = HIGH; 0 = LOW
CLK	40	D1	1 = rising; 0 = falling
CLPDM	12	D2	1 = HIGH; 0 = LOW
CLPOB	13	D3	1 = HIGH; 0 = LOW
PBK	11	D5	1 = HIGH; 0 = LOW
VSYNC	24	D6	0 = rising; 1 = falling

Note

1. Bit D4 is not used.

Table 3 Standby selection

STDBY	ADC DIGITAL OUTPUTS D9 TO D0	I _{CCA} + I _{CCO} + I _{CCD} (TYP.)
1	logic state LOW	1 mA
0	active	64 mA

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APPLICATION DIAGRAM

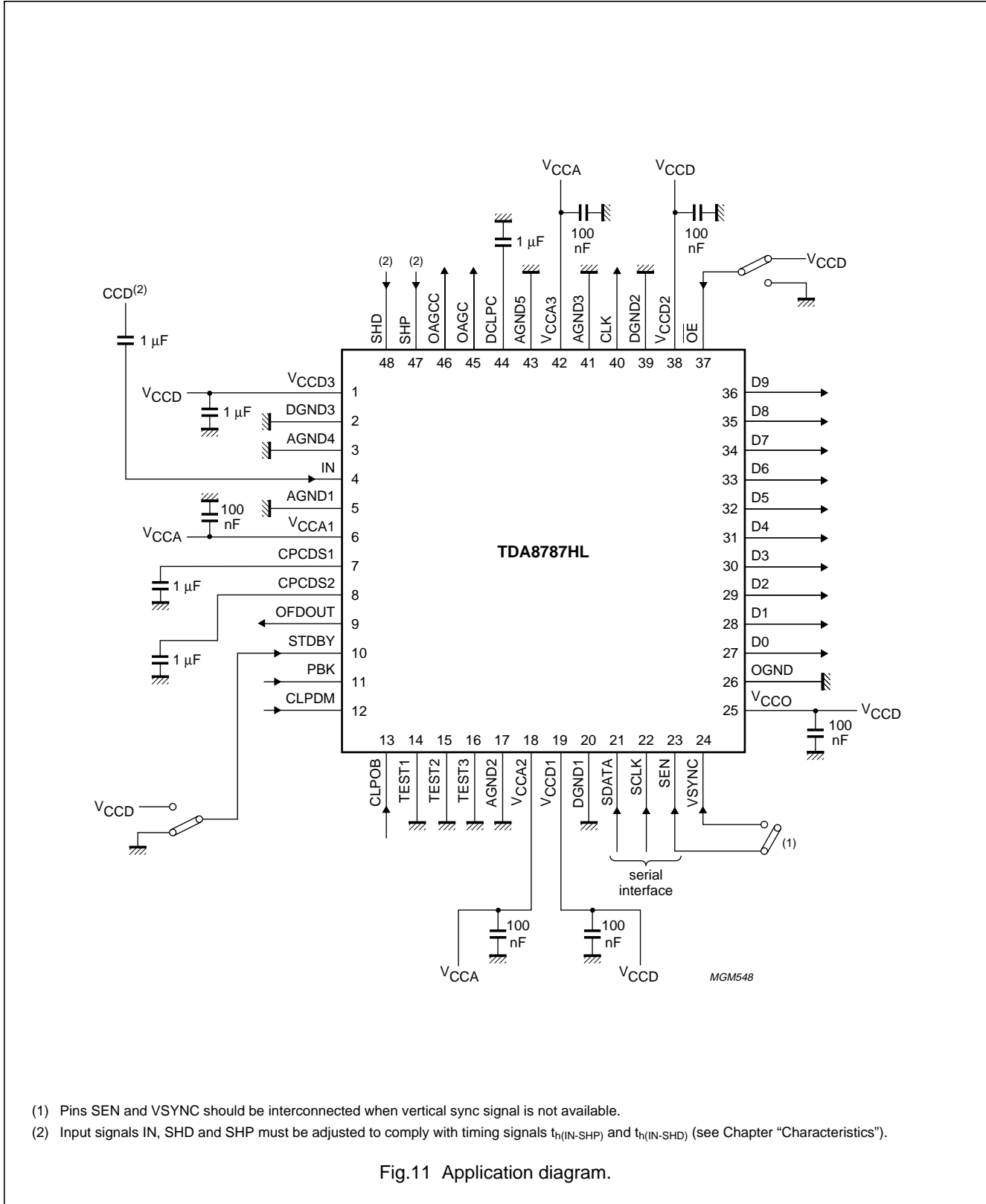


Fig.11 Application diagram.

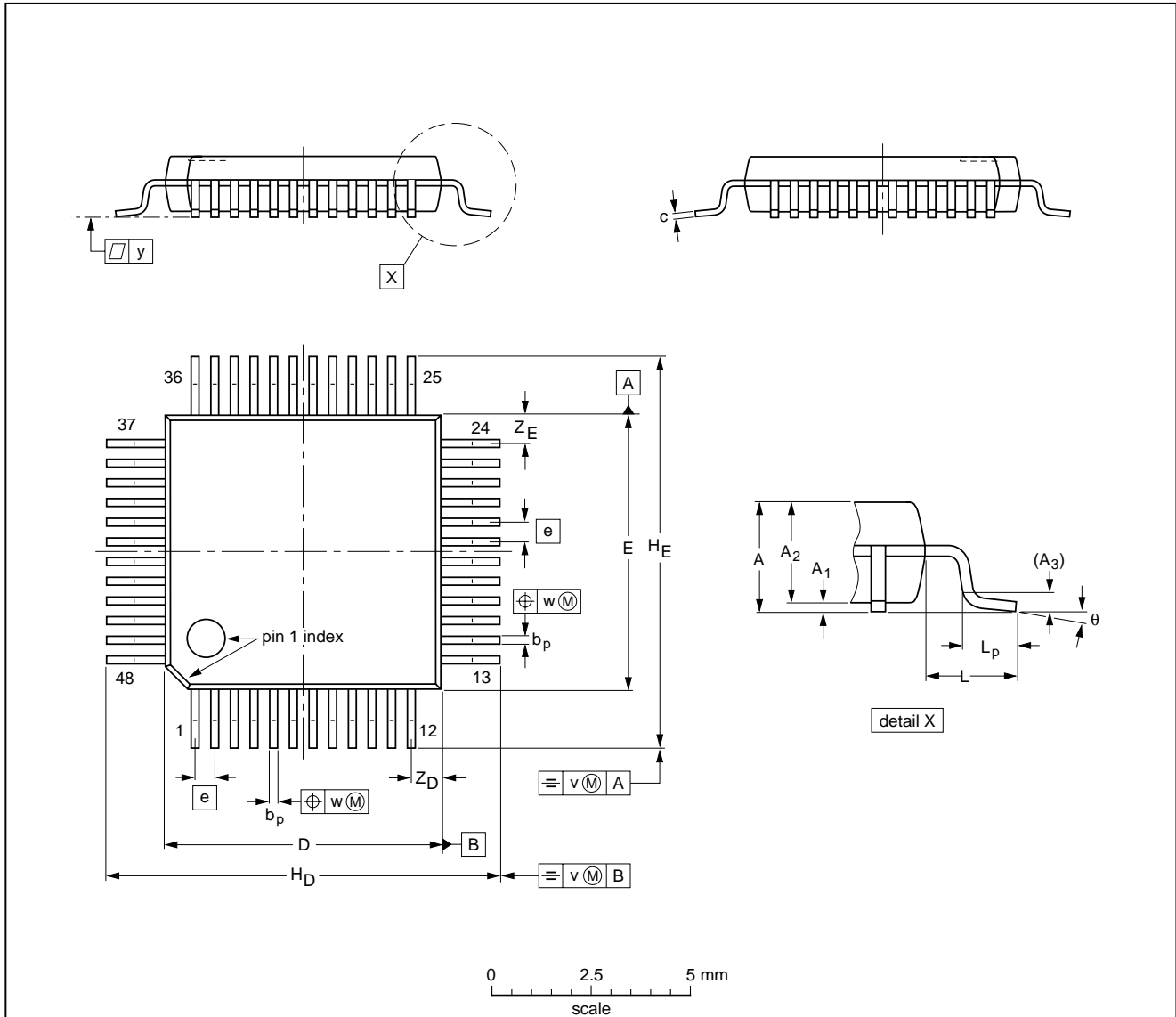
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PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm

SOT313-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						94-12-19 97-08-01

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

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TDA8787**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010, Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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