

# DATA SHEET

## **TDA8566TH**

**2 × 40 W/2 Ω stereo BTL car radio  
power amplifier with differential  
inputs and diagnostic outputs**

Objective specification  
File under Integrated Circuits, IC01

2001 Apr 24

## 2 × 40 W/2 Ω stereo BTL car radio power amplifier with differential inputs and diagnostic outputs

### TDA8566TH

#### FEATURES

- Differential inputs
- Very high Common Mode Rejection Ratio (CMRR)
- High common mode input signal handling
- Requires very few external components
- High output power
- 4 and 2 Ω load driving capability
- Low offset voltage at output
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit proof to ground, to  $V_P$  and across the load

- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Protected against electrostatic discharge
- No switch-on/switch-off plops
- Low thermal resistance.

#### GENERAL DESCRIPTION

The TDA8566TH is an integrated class-B output amplifier contained in a 20-lead small outline plastic package. The device contains 2 amplifiers in a Bridge-Tied Load (BTL) configuration. The output power is 2 × 25 W in a 4 Ω load or 2 × 40 W in a 2 Ω load. It has a differential input stage and 2 diagnostic outputs. The device is primarily developed for car radio applications.

#### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	operating supply voltage		6	14.4	18	V
$I_{ORM}$	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
$I_{stb}$	standby current		–	0.1	10	μA
$I_{sw}$	switch-on current		–	–	40	μA
$Z_i$	input impedance		100	120	–	kΩ
$P_{out}$	output power	$R_L = 4 \Omega$ ; THD = 10%	–	25	–	W
		$R_L = 2 \Omega$ ; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	$R_s = 0 \Omega$	–	60	–	dB
$\alpha_{cs}$	channel separation	$R_s = 10 \text{ k}\Omega$	–	50	–	dB
CMRR	common mode rejection ratio		–	75	–	dB
$G_v$	closed loop voltage gain		25	26	27	dB
$V_{n(o)}$	noise output voltage	$R_s = 0 \Omega$	–	–	120	μV

#### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8566TH	HSOP20	plastic, heatsink small outline package; 20 leads; low stand-off height	SOT418-2

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**BLOCK DIAGRAM**

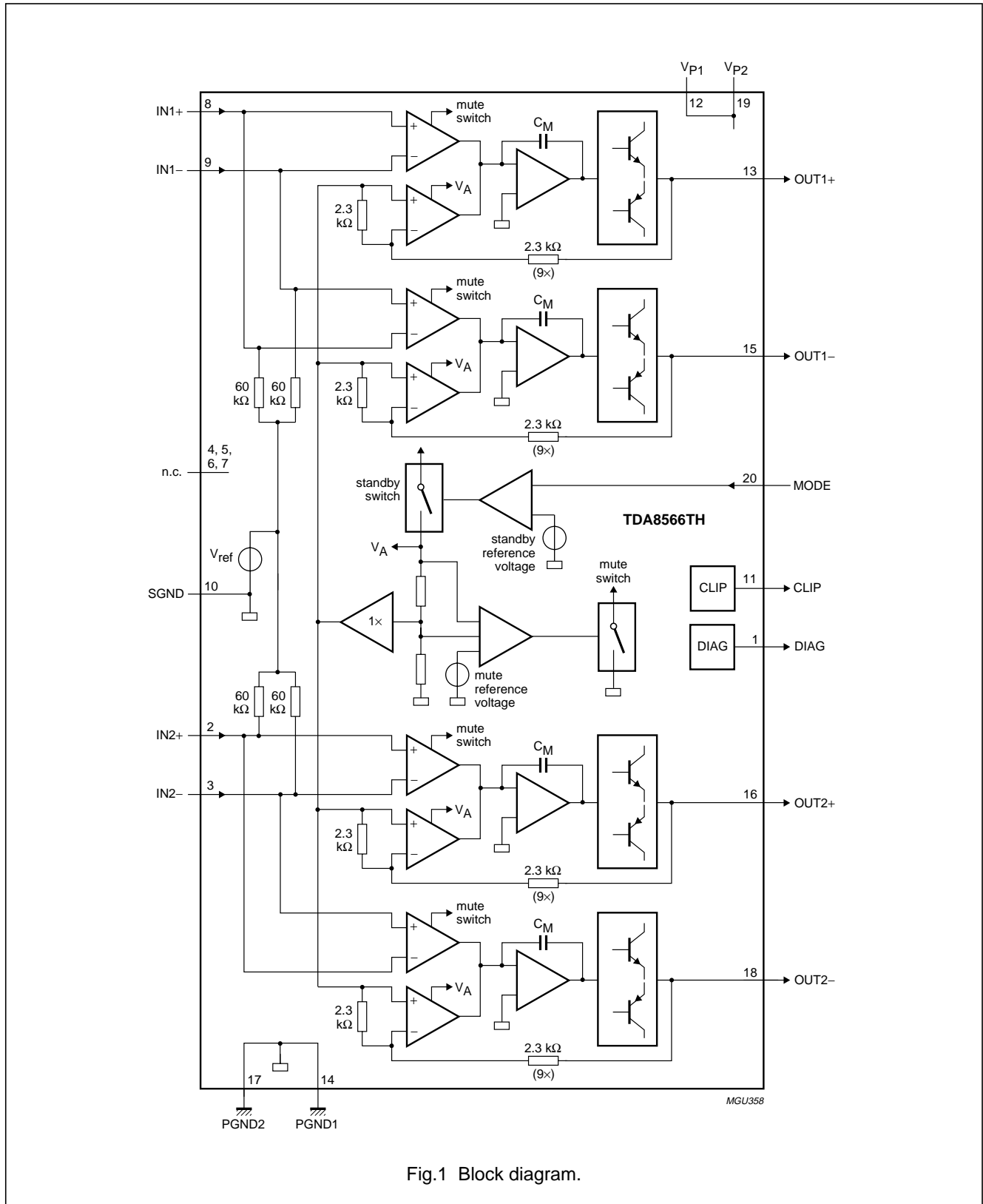


Fig.1 Block diagram.

**2 × 40 W/2 Ω stereo BTL car radio power amplifier  
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**PINNING**

SYMBOL	PIN	DESCRIPTION
DIAG	1	short-circuit and temperature pre-warning diagnostic output
IN2+	2	channel 2 input positive
IN2-	3	channel 2 input negative
n.c.	4	not connected
n.c.	5	not connected
n.c.	6	not connected
IN1+	8	channel 1 input positive
IN1-	9	channel 1 input negative
SGND	10	signal ground
CLIP	11	clip detection output
V <sub>P1</sub>	12	supply voltage 1
OUT1+	13	channel 1 output positive
PGND1	14	power ground 1
OUT1-	15	channel 1 output negative
OUT2+	16	channel 2 output positive
PGND2	17	power ground 2
OUT2-	18	channel 2 output negative
V <sub>P2</sub>	19	supply voltage 2
MODE	20	mode select switch input (standby/mute/operating)

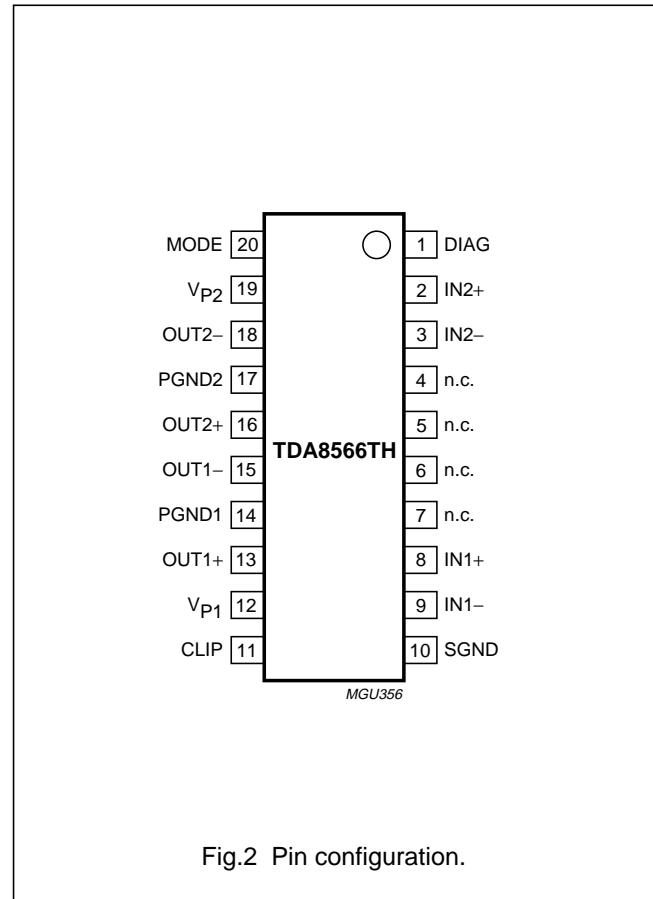


Fig.2 Pin configuration.

## 2 × 40 W/2 Ω stereo BTL car radio power amplifier with differential inputs and diagnostic outputs

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### FUNCTIONAL DESCRIPTION

The TDA8566TH contains 2 identical amplifiers and can be used for BTL applications. The gain of each amplifier is fixed at 26 dB. Special features of this device are:

1. Mode select switch
2. Clip detection
3. Short-circuit diagnostic
4. Temperature pre-warning
5. Open-collector diagnostic outputs
6. Differential inputs.

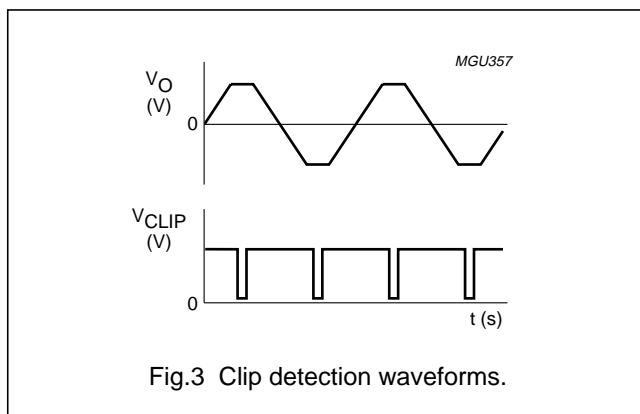
#### Mode select switch (pin MODE)

- Standby: low supply current
- Mute: input signal suppressed
- Operating: normal on condition.

Since this pin has a very low input current (<40 μA), a low cost supply switch can be applied. To avoid switch-on pops, it is advisable to keep the amplifier in the mute mode for a period of ≥150 ms (charging the input capacitors at pins IN1+, IN1-, IN2+ and IN2-). This can be realized by using a microcontroller or by using an external timing circuit as illustrated in Fig.7.

#### Clip detection (pin CLIP)

When clipping occurs at one or more output stages, the dynamic distortion detector becomes active and pin CLIP goes LOW. This information can be used to drive a sound processor or a DC volume control to attenuate the input signal and so limit the level of distortion. The output level of pin CLIP is independent of the number of channels that are being clipped. The clip detection circuit is disabled in a short-circuit condition, so if a fault condition occurs at the outputs, pin CLIP will remain at a HIGH level. The clip detection waveforms are illustrated in Fig.3.



#### Short-circuit diagnostic (pin DIAG)

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again (with a delay of approximately 20 ms after the removal of the short-circuit). During this short-circuit condition, pin DIAG is continuously LOW.

When a short-circuit occurs across the load of one or both channels, the output stages are switched off for approximately 20 ms. After that time the load condition is checked during approximately 50 μs to see whether the short-circuit is still present. Due to this duty cycle of 50 μs/20 ms the average current consumption during the short-circuit condition is very low (approximately 40 mA). During this condition, pin DIAG is LOW for 20 ms and HIGH for 50 μs; see Fig.4. The power dissipation in any short-circuit condition is very low.

#### Temperature pre-warning (pin DIAG)

When the junction temperature ( $T_{vj}$ ) reaches 145 °C, pin DIAG will become continuously LOW.

#### Open-collector diagnostic outputs

Pins DIAG and CLIP are open-collector outputs, therefore more devices can be tied together. Pins DIAG and CLIP can also be tied together. An external pull-up resistor is required.

#### Differential inputs

The input stage is a high-impedance fully differential balanced input stage that is also capable of operating in a single-ended mode with one of the inputs capacitively coupled to an audio ground. It should be noted that if a source resistance is added (input voltage dividers) the CMRR degrades to lower values.

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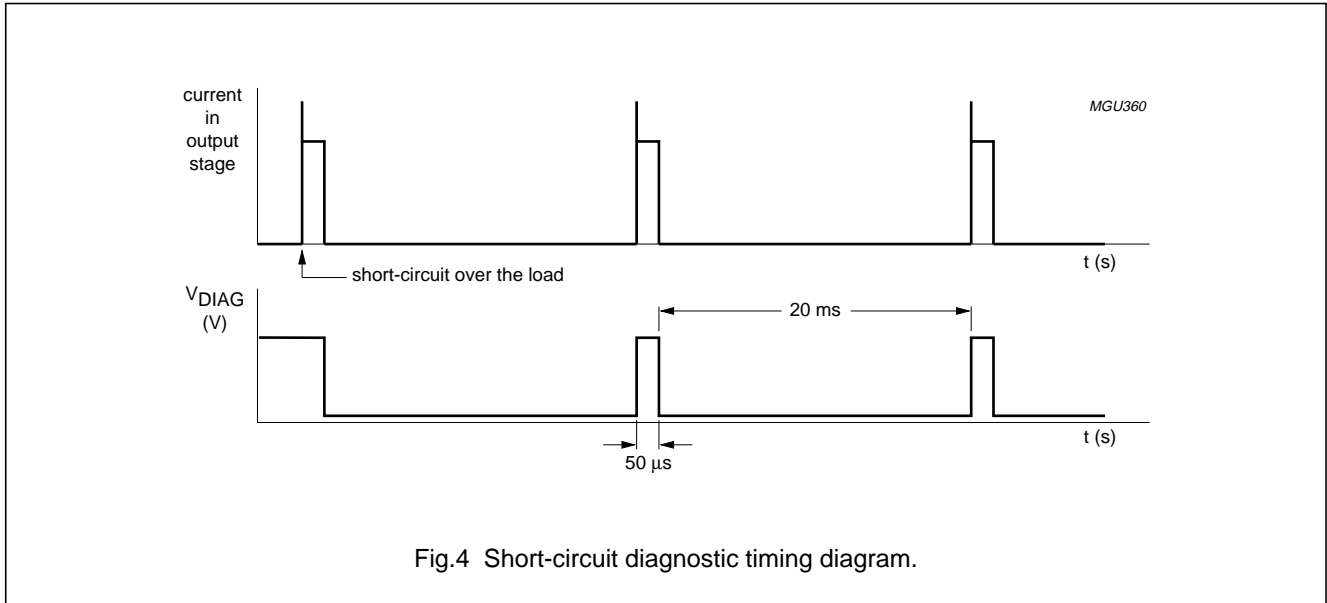


Fig.4 Short-circuit diagnostic timing diagram.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_P$	supply voltage	operating	–	18	V
		non-operating	–	30	V
		load dump protection; during 50 ms; $t_r \geq 2.5$ ms	–	45	V
$I_{OSM}$	non-repetitive peak output current		–	10	A
$I_{ORM}$	repetitive peak output current		–	7.5	A
$T_{stg}$	storage temperature		–55	+150	°C
$T_{vj}$	virtual junction temperature		–	150	°C
$T_{amb}$	ambient temperature		–40	+85	°C
$V_{psc}$	short-circuit safe voltage		–	18	V
$V_{rp}$	reverse polarity voltage		–	6.0	V
$P_{tot}$	total power dissipation		–	60	W

**QUALITY SPECIFICATION**

Quality specification in accordance with “SNW-FQ-611D”, if this type is used as an audio amplifier.

**THERMAL CHARACTERISTICS**

Thermal characteristics in accordance with IEC 60747-1.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	see Fig.5	1.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

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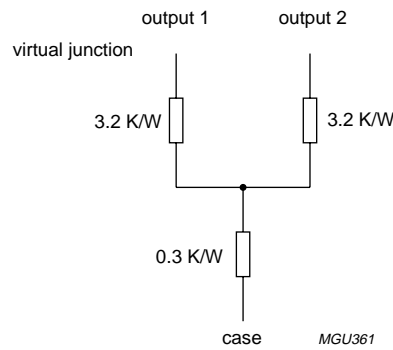


Fig.5 Equivalent thermal resistance network.

### DC CHARACTERISTICS

$V_P = 14.4\text{ V}$ ;  $T_{\text{amb}} = 25\text{ °C}$ ; measured in test circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_P$	supply voltage	note 1	6	14.4	18	V
$I_q$	quiescent current	$R_L = \infty$	–	115	180	mA
<b>Operating condition</b>						
$V_{\text{MODE}}$	mode select switch level		8.5	–	$V_P$	V
$I_{\text{MODE}}$	mode select switch current	$V_{\text{MODE}} = 14.4\text{ V}$	–	15	40	$\mu\text{A}$
$V_O$	output voltage	note 2	–	7.0	–	V
$V_{\text{OO}}$	output offset voltage		–	–	100	mV
<b>Mute condition</b>						
$V_{\text{MODE}}$	mode select switch level		3.3	–	6.4	V
$V_O$	output voltage	note 2	–	7.0	–	V
$V_{\text{OO}}$	output offset voltage		–	–	60	mV
$\Delta V_{\text{OO}}$	output offset voltage difference	with respect to operating condition	–	–	60	mV
<b>Standby condition</b>						
$V_{\text{MODE}}$	mode select switch level		0	–	2	V
$I_{\text{stb}}$	standby current		–	0.1	10	$\mu\text{A}$
<b>Diagnostic</b>						
$V_{\text{DIAG}}$	diagnostic output voltage	during any fault condition	–	–	0.6	V

### Notes

1. The circuit is DC adjusted at  $V_P = 6$  to  $18\text{ V}$  and AC operating at  $V_P = 8.5$  to  $18\text{ V}$ .
2. At  $V_P = 18$  to  $30\text{ V}$  the DC output voltage is  $\leq 0.5V_P$ .

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**AC CHARACTERISTICS**

$V_P = 14.4\text{ V}$ ;  $T_{\text{amb}} = 25\text{ °C}$ ;  $R_L = 2\ \Omega$ ;  $f_i = 1\text{ kHz}$ ; measured in test circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P <sub>o</sub>	output power	THD = 0.5%	25	30	–	W
		THD = 10%	33	40	–	W
		THD = 30%	45	55	–	W
		V <sub>P</sub> = 13.5 V; THD = 0.5%	–	25	–	W
		V <sub>P</sub> = 13.5 V; THD = 10%	–	35	–	W
		THD = 0.5%; R <sub>L</sub> = 4 Ω	16	19	–	W
		THD = 10%; R <sub>L</sub> = 4 Ω	21	25	–	W
		THD = 30%; R <sub>L</sub> = 4 Ω	28	35	–	W
		V <sub>P</sub> = 13.5 V; THD = 0.5%; R <sub>L</sub> = 4 Ω	–	14	–	W
		V <sub>P</sub> = 13.5 V; THD = 10%; R <sub>L</sub> = 4 Ω	–	22	–	W
THD	total harmonic distortion	P <sub>o</sub> = 1 W	–	0.1	–	%
		V <sub>CLIP</sub> = 0.6 V; note 1	–	8	–	%
		P <sub>o</sub> = 1 W; R <sub>L</sub> = 4 Ω	–	0.05	–	%
B	power bandwidth	THD = 0.5%; P <sub>o</sub> = –1 dB with respect to 25 W	–	20 to 20000	–	Hz
f <sub>ro(l)</sub>	low frequency roll off	–1 dB; note 2	–	25	–	Hz
f <sub>ro(h)</sub>	high frequency roll off	–1 dB	20	–	–	kHz
G <sub>v</sub>	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	operating; note 3	50	–	–	dB
		mute; note 3	50	–	–	dB
		standby; note 3	80	–	–	dB
Z <sub>i</sub>	input impedance	differential	100	120	150	kΩ
		single-ended	50	60	75	kΩ
ΔZ <sub>i</sub>	input impedance mismatch		–	2	–	%
V <sub>n(o)</sub>	noise output voltage	operating; R <sub>s</sub> = 0 Ω; note 4	–	85	120	μV
		operating; R <sub>s</sub> = 10 kΩ; note 4	–	100	–	μV
		mute; independent of R <sub>s</sub> ; note 4	–	60	–	μV
α <sub>cs</sub>	channel separation	P <sub>o</sub> = 25 W; R <sub>s</sub> = 10 kΩ	45	–	–	dB
ΔG <sub>v</sub>	channel unbalance		–	–	1	dB



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{O(\text{mute})}$	output signal voltage in mute	$V_{in} = V_{in(\text{max})} = 1 \text{ V (RMS)}$	–	–	2	mV
CMRR	common mode rejection ratio	$R_s = 0 \text{ } \Omega$ ; note 5	60	75	–	dB
		$R_s = 45 \text{ k}\Omega$ ; note 6	40	–	–	dB

**Notes**

1. Dynamic distortion detector active; pin CLIP is LOW.
2. Frequency response externally fixed.
3.  $V_{\text{ripple}} = V_{\text{ripple}(\text{max})} = 2 \text{ V (p-p)}$ ;  $R_s = 0 \text{ } \Omega$ .
4. Noise measured in a bandwidth of 20 Hz to 20 kHz.
5. Common mode rejection ratio measured at the output (over  $R_L$ ) with both inputs tied together;  $V_{\text{common}} \leq 3.5 \text{ V (RMS)}$ ;  $f_i = 100 \text{ Hz to } 10 \text{ kHz}$ ;  $R_s = 0 \text{ } \Omega$ .
6. Common mode rejection ratio measured at the output (over  $R_L$ ) with both inputs tied together;  $V_{\text{common}} \leq 3.5 \text{ V (RMS)}$ ;  $f_i = 1 \text{ kHz}$ ;  $R_s = 45 \text{ k}\Omega$ . The mismatch of the input coupling capacitors is excluded.

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**TEST AND APPLICATION INFORMATION**

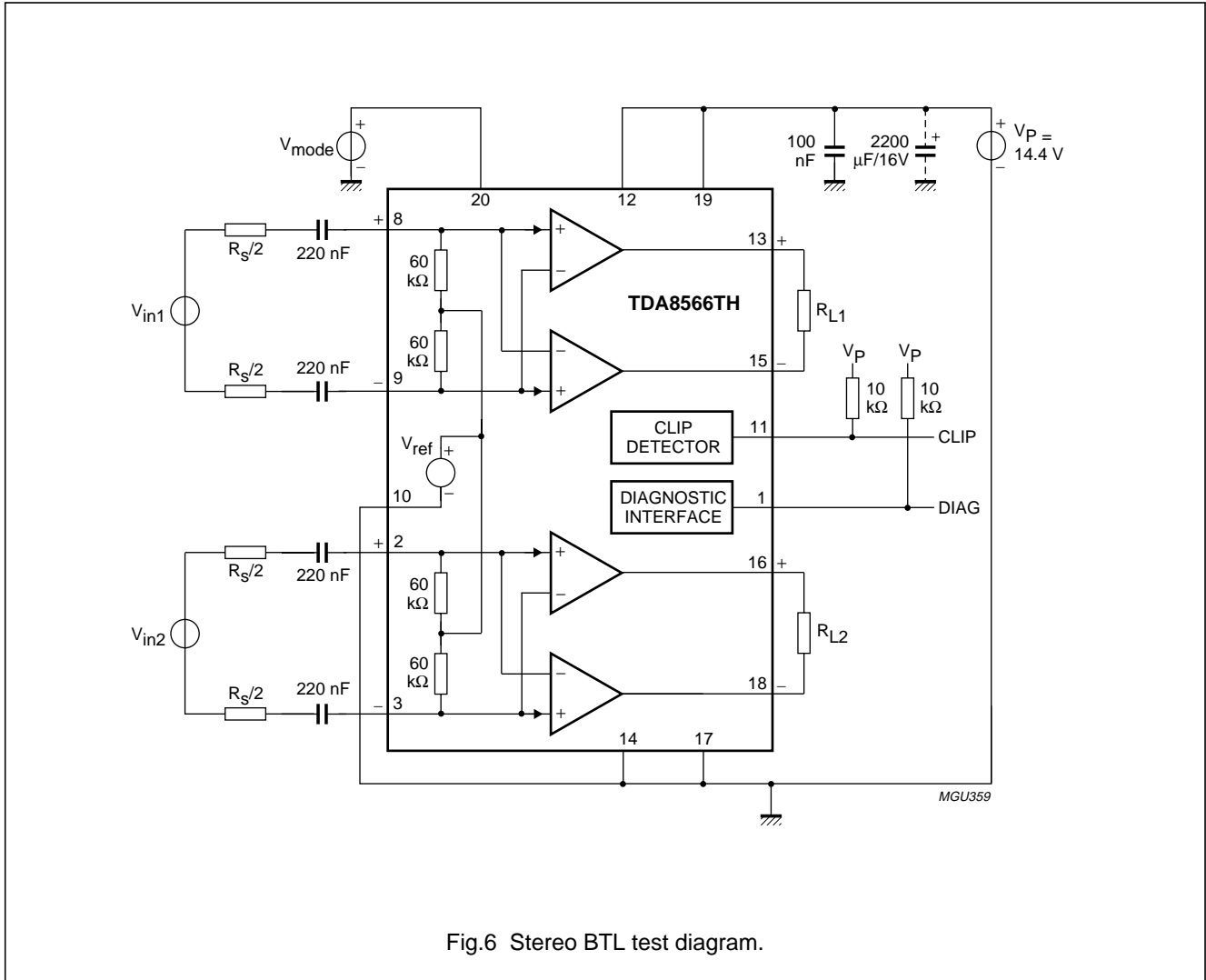


Fig.6 Stereo BTL test diagram.

**Application information**

**DIAGNOSTIC OUTPUT**

Special care must be taken in the PCB layout to separate pin CLIP from pins IN1+, IN1-, IN2+ and IN2- to minimize the crosstalk between the CLIP output and the inputs.

**MODE SELECT SWITCH**

To avoid switch-on plops, it is advisable to keep the amplifier in the mute mode during ≥150 ms (charging of the input capacitors at pins IN1+, IN1-, IN2+ and IN2-). The circuit in Fig.7 slowly ramps-up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

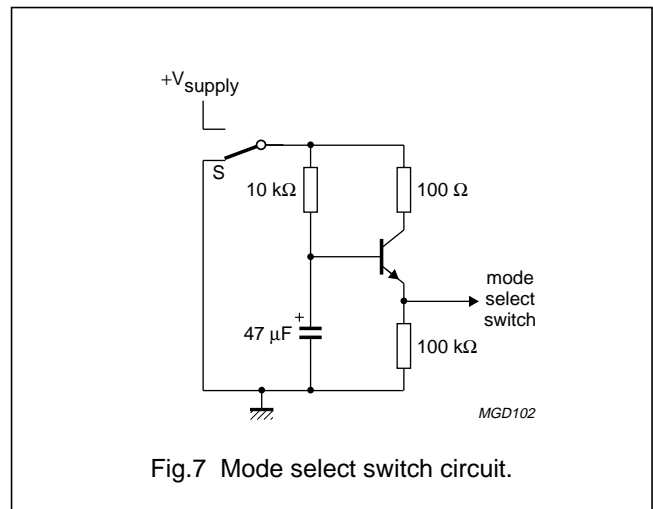


Fig.7 Mode select switch circuit.

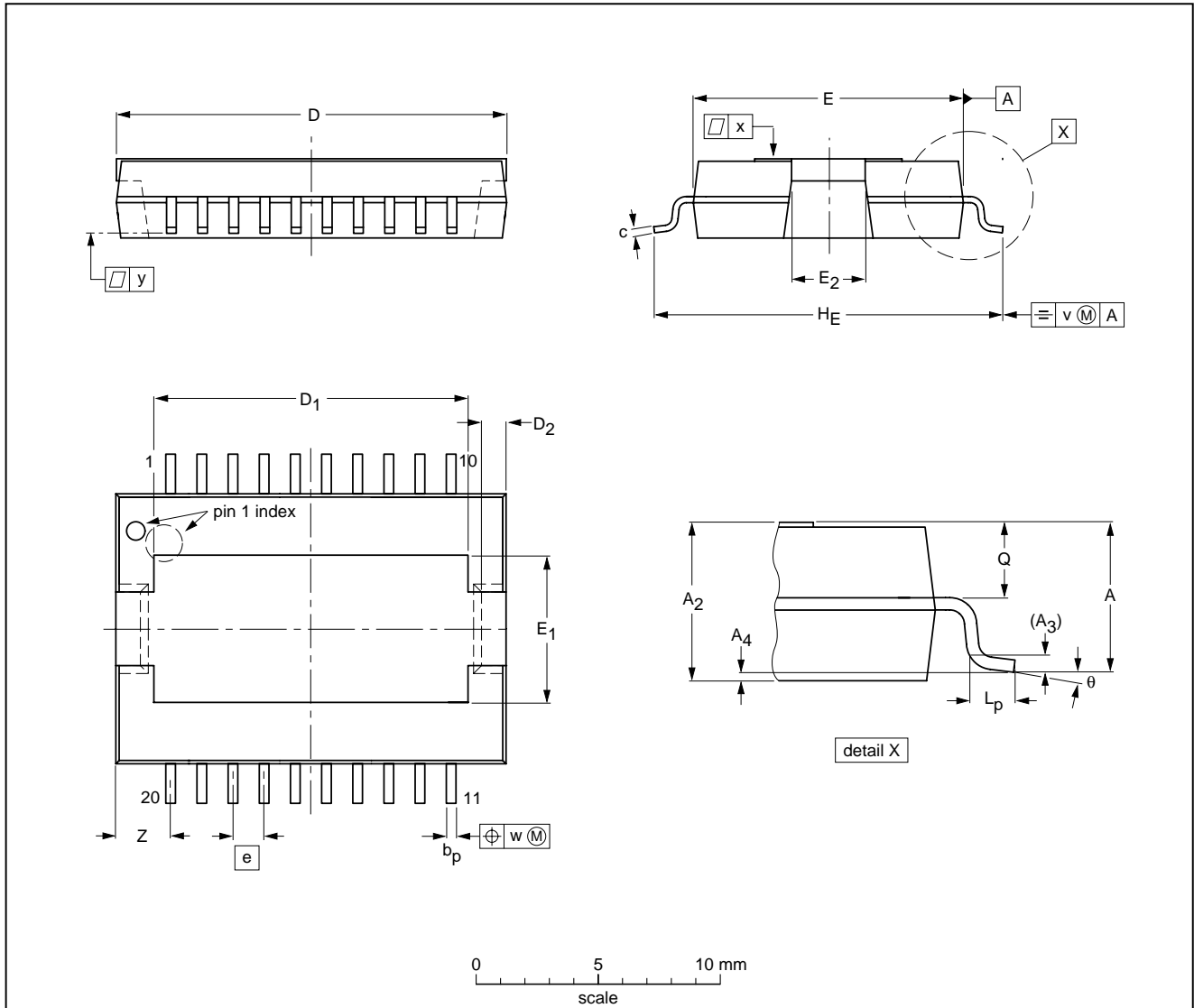
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**PACKAGE OUTLINE**

**HSOP20: plastic, heatsink small outline package; 20 leads; low stand-off height**

**SOT418-2**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sub>max.</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub> <sup>(1)</sup>	b <sub>p</sub>	c	D <sup>(2)</sup>	D <sub>1</sub>	D <sub>2</sub>	E <sup>(2)</sup>	E <sub>1</sub>	E <sub>2</sub>	e	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.12 -0.02	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1.27	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.5 2.0	8° 0°

**Notes**

- Limits per individual lead.
- Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT418-2						98-02-25 99-11-12

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**Suitability of surface mount IC packages for wave and reflow soldering methods**

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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**DATA SHEET STATUS**

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

**Notes**

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

**DEFINITIONS**

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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with differential inputs and diagnostic outputs**

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**NOTES**

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 3 Figtree Drive, HOMEBUSH, NSW 2140,  
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 7 - 9 Rue du Mont Valérien, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4728 6600, Fax. +33 1 4728 6638

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** Philips Hungary Ltd., H-1119 Budapest, Fehervari ut 84/A,  
Tel: +36 1 382 1700, Fax: +36 1 382 1800

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),  
Tel. +39 039 203 6838, Fax +39 039 203 6800

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Al.Jerozolimskie 195 B, 02-222 WARSAW,  
Tel. +48 22 5710 000, Fax. +48 22 5710 001

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 319762,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,  
Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,  
Tel. +66 2 361 7910, Fax. +66 2 398 3447

**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,  
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 3341 299, Fax.+381 11 3342 553

**For all other countries apply to:** Philips Semiconductors,  
Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,  
The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

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