DATA SHEET

TDA8044
Satellite demodulator and decoder

Product specification
Supersedes data of 1998 Nov 17
File under Integrated Circuits, IC02

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Philips
Semiconductors

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FEATURES

- General features:
  - One-chip Digital Video Broadcasting (DVB) compliant Quadrature Phase Shift Keying (QPSK) and Binary Phase Shift Keying (BPSK) demodulator and concatenated Viterbi/Reed-Solomon decoder with de-interleaver and de-randomizer (ETS 300 421)
  - 3.3 V supply voltage (input pads are 5 V tolerant)
  - Standby mode for low power dissipation
  - Internal clock PLL to allow low frequency crystal application and selectable clock frequencies
  - Power-on reset module
  - Package: QFP100
  - Boundary scan test.
- QPSK/BPSK demodulator:
  - Interpolator and anti-alias filter to handle a large range of symbol rates without additional external filtering
  - On-chip AGC of the analog input I and Q baseband signals or tuner AGC control
  - Two on-chip matched Analog-to-Digital Converters (ADCs; 7 bits)
  - Half Nyquist (square root raised-cosine) filter with selectable roll-off factor
  - Large range of symbol frequencies: 0.5 to 45 Msymbols/s for TDA8044 and 0.5 to 30 Msymbols/s for TDA8044A, including Single Carrier Per Channel (SCPC) function
  - Can be used at low channel Signal-to-Noise ratio (S/N)
  - Internal carrier recovery, clock recovery and AGC loops with programmable loop filters
  - Two loop carrier recovery enabling phase tracking of the incoming symbols
  - Software carrier sweep for low symbol rate applications
  - Signal-to-noise ratio estimation
  - External indication of demodulator lock.
- Viterbi decoder:
  - Rate $\frac{1}{2}$ convolutional code based
  - Constraint length K = 7 with $G_1 = 171_{oct}$ and $G_2 = 133_{oct}$; supported puncturing code rates: $\frac{1}{2}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{4}{5}$, $\frac{5}{6}$, $\frac{6}{7}$, $\frac{7}{8}$ and $\frac{8}{9}$
  - 4 bits input for ‘soft decision’ for both I and Q
  - Truncation length: 144
  - Automatic synchronization
  - Channel Bit Error Rate (BER) estimation
  - External indication of Viterbi sync lock
  - Differential decoding optional.
- Reed-Solomon (RS) decoder:
  - (204, 188, T = 8) Reed-Solomon code
  - Automatic (I^2C-bus configurable) synchronization of bytes, transport packets and frames
  - Internal convolutional de-interleaving (I = 12; using internal memory)
  - De-randomizer based on Pseudo Random Bit Sequence (PRBS)
  - External indication of Register Select (RS) decoder sync lock
  - External indication of uncorrectable error (transport error indicator is set)
  - External indication of corrected byte
  - Indication of the number of lost blocks
  - Indication of the number of corrected blocks.
- Interface:
  - I^2C-bus interface to initialize and monitor the demodulator and Forward Error Correction (FEC) decoder; when no I^2C-bus usage, default mode is defined
  - Programmable interrupt facility
  - 6 bits I/O expander for flexible access to and from the I^2C-bus
  - Switchable I^2C-bus loop-through to suppress I^2C-bus crosstalk in the tuner
  - DiSEqC level 1.X support for dish control applications
  - 3-state mode for transport stream outputs.

APPLICATIONS

- Digital satellite TV: demodulation and Forward Error Correction (FEC).

GENERAL DESCRIPTION

This document gives preliminary information about the TDA8044 and TDA8044A, which are the successors of the TDA8043. The TDA8044A is only specified where the product deviates from the TDA8044, all other references are the same. The TDA8044 is backwards compatible with the TDA8043, with respect to pinning and the I^2C-bus software. The TDA8044 is a DVB compliant demodulator and error correction decoder IC for reception of QPSK and BPSK modulated signals for satellite applications. It can handle variable symbol rates in the range of 0.5 to 45 Msymbols/s (0.5 to 30 Msymbols/s for TDA8044A) with a minimum number of low cost and non-critical external components. Typical applications for this device are Multi Channel Per Carrier (MCPC), Single Channel Per Carrier (SCPC) and simulcast. In these applications one satellite transponder contains respectively one broad QPSK carrier, several small QPSK carriers and one small QPSK carrier together with one or two FM carriers.

The TDA8044 has minimum interface with the tuner, it only requires the demodulated analog I and Q baseband input signals. Analog-to-digital conversion is performed internally by two matched 7-bit ADCs. Since all the loops (AGC, clock and carrier recovery) are internal, no feedback to the tuner is needed. However, for maximum tuner flexibility, there is the possibility to close the AGC and carrier recovery loop externally via the tuner.

The number of external components required for operation of the TDA8044 is very low. Moreover the external components are low cost and non-critical. This gives an easy and low cost application. The TDA8044 operates on a low frequency crystal which is upconverted to a clock frequency by means of an internal PLL. Different clock frequencies can be selected with the PLL without changing the crystal. This allows for maximum flexibility concerning symbol rate range combined with minimum power consumption.

The TDA8044 also has internal anti-alias filters, which can cover a large range of symbol frequencies (approximately one decade) without the need to switch external (SAW) filters. To cover the whole range of 0.5 to 45 Msymbols/s switching of clock frequency (internally) and filtering (externally) is necessary.

The TDA8044 has a double carrier loop configuration which has excellent capabilities of tracking phase noise. Synchronization of the FEC unit is done completely internally, thereby minimizing I^2C-bus communication. The output of the TDA8044 is highly flexible, allowing different output modes to interface to a demultiplexer/descrambler/MPEG-2 decoder including a 3-state mode. For evaluation of the TDA8044, demodulator and Viterbi outputs can be made available externally.

Interfacing to the TDA8044 has been extended compared to the TDA8043. Separate resets are available for logic only, logic plus I^2C-bus and carrier loops. A Power-on reset module has been implemented which gives a reset signal at power-up. This signal can be used to reset the TDA8044 in order to guarantee correct starting of the IC. Two extra general purpose I/O pins (I/O expanders) have been added. A switchable I^2C-bus loop-through to the tuner is implemented to switch-off the I^2C-bus connection to the tuner. This reduces phase noise in the tuner in the event of I^2C-bus crosstalk. The transport stream outputs can be put in 3-state mode. DiSEqC level 1.X support is integrated for dish control applications. The power consumption in standby mode has been decreased considerably.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		3.05	3.3	3.55	V
V_{DDD}	digital supply voltage		3.05	3.3	3.55	V
$I_{DD(tot)}$	total supply current	V_{DDD} = 3.3 V				
	TDA8044	note 1	–	320	480	mA
	TDA8044A	notes 1 and 2	–	–	350	mA
f_{clk}	internal clock frequency	CFS = 0 or CFS = 1; f_{xtal} = 4 MHz				
	TDA8044	note 1	10.7	–	96	MHz
	TDA8044A	notes 1 and 2	10.7	–	64	MHz
r_s	symbol rate	note 3				
	TDA8044		0.5	–	45	Msymbols/s
	TDA8044A		0.5	–	30	Msymbols/s
P_{tot}	total power dissipation	T_{amb} = 70 °C; note 4				
	TDA8044		–	1150	1700	mW
	TDA8044A		–	–	1250	mW
IL	implementation loss	note 5	–	0.3	–	dB
S/N	signal-to-noise ratio for locking the TDA8044	note 5	2	–	–	dB

Notes

1. Programmable internal frequencies possible:
   a) Values 10.7, 16, 32 or 64 MHz for CFS = 0.
   b) Values 16, 24, 48 or 96 MHz for CFS = 1.
2. CFS is set to logic 0.
3. Without switching internal clock frequencies, a range of 1 decade can be covered. To cover the full range of symbol frequencies, internal clock frequencies and external (SAW) filters must be switched. Details can be found in the application note.
4. Maximum value is specified for a symbol rate of 45 Msymbols/s, a puncturing rate of $^7/_8$, a clock frequency of 96 MHz and a 3.55 V power supply. The typical value is specified for a symbol rate of 27.5 Msymbols/s, a puncture rate of $^3/_4$ and a clock frequency of 64 MHz.
5. Implementation loss at the demodulator output and minimum S/N to lock the TDA8044 are measured including tuner in a laboratory environment at a symbol rate of 27.5 Msymbols/s and a clock frequency of 64 MHz.

ORDERING INFORMATION

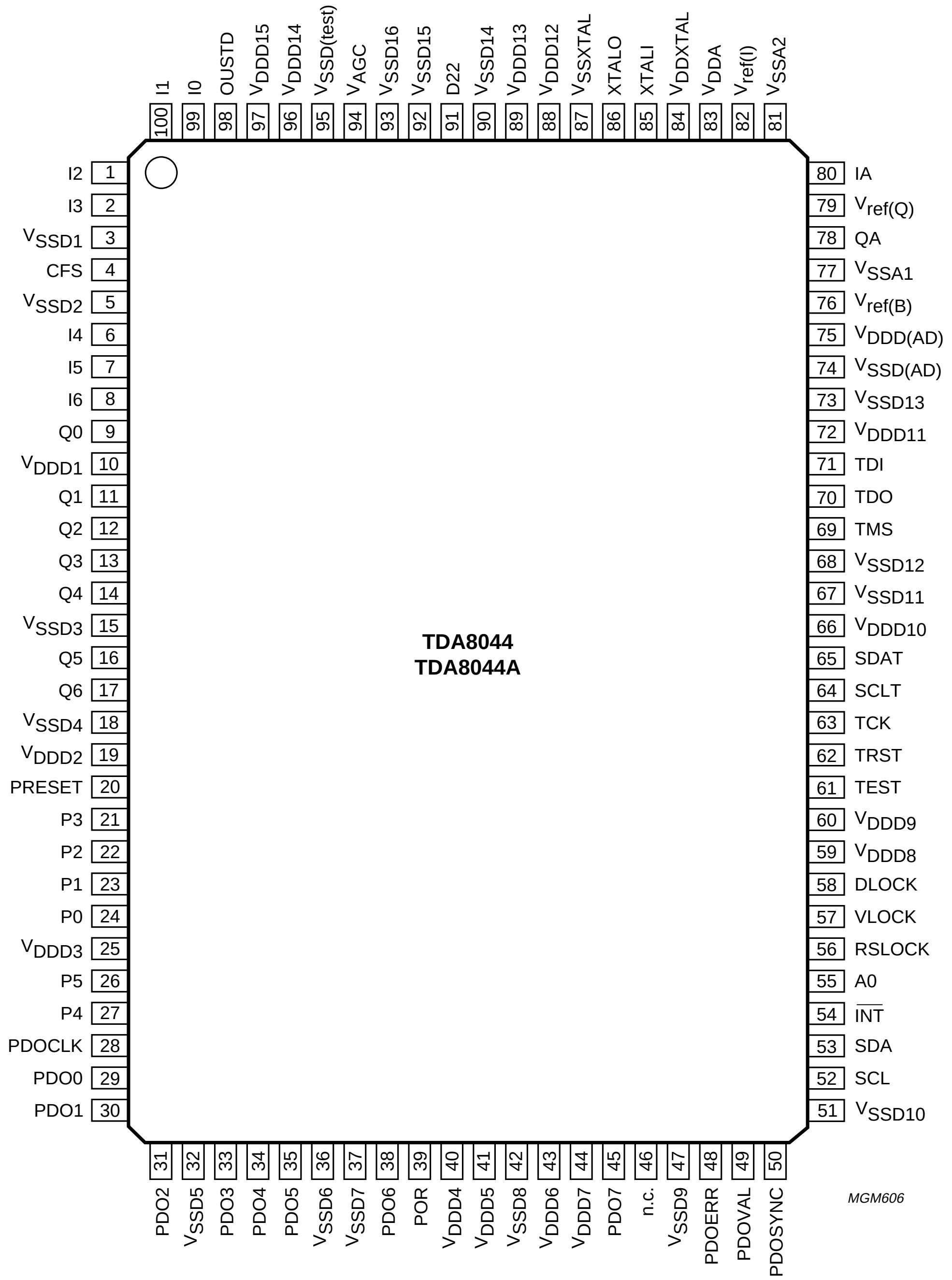
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8044H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT317-2
TDA8044AH			

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
I2	1	I	digital I-input bit 2 (ADC bypass)
I3	2	I	digital I-input bit 3 (ADC bypass)
V_{SSD1}	3	–	digital ground 1
CFS	4	I	clock frequency selection (remains at logic 0 for TDA8044A)
V_{SSD2}	5	–	digital ground 2
I4	6	I	digital I-input bit 4 (ADC bypass)
I5	7	I	digital I-input bit 5 (ADC bypass)
I6	8	I	digital I-input bit 6 (ADC bypass: MSB)
Q0	9	I	digital Q-input bit 0 (ADC bypass: LSB)
V_{DDD1}	10	–	digital supply voltage 1
Q1	11	I	digital Q-input bit 1 (ADC bypass)
Q2	12	I	digital Q-input bit 2 (ADC bypass)
Q3	13	I	digital Q-input bit 3 (ADC bypass)
Q4	14	I	digital Q-input bit 4 (ADC bypass)
V_{SSD3}	15	–	digital ground 3
Q5	16	I	digital Q-input bit 5 (ADC bypass)
Q6	17	I	digital Q-input bit 6 (ADC bypass: MSB)
V_{SSD4}	18	–	digital ground 4
V_{DDD2}	19	–	digital supply voltage 2
PRESET	20	I	set device into default mode
P3	21	I/O	quasi-bidirectional I/O port (bit 3)
P2	22	I/O	quasi-bidirectional I/O port (bit 2)
P1	23	I/O	quasi-bidirectional I/O port (bit 1)
P0	24	I/O	quasi-bidirectional I/O port (bit 0)
V_{DDD3}	25	–	digital supply voltage 3
P5	26	I/O	quasi-bidirectional I/O port (bit 5)
P4	27	I/O	quasi-bidirectional I/O port (bit 4)
PDOCLK	28	O	output clock for transport stream bytes
PDO0	29	O	parallel data output (bit 0)
PDO1	30	O	parallel data output (bit 1)
PDO2	31	O	parallel data output (bit 2)
V_{SSD5}	32	–	digital ground 5
PDO3	33	O	parallel data output (bit 3)
PDO4	34	O	parallel data output (bit 4)
PDO5	35	O	parallel data output (bit 5)
V_{SSD6}	36	–	digital ground 6
V_{SSD7}	37	–	digital ground 7
PDO6	38	O	parallel data output (bit 6)
POR	39	I	Power-on reset [can be connected to PRESET (pin 20)]
V_{DDD4}	40	–	digital supply voltage 4

SYMBOL	PIN	I/O	DESCRIPTION
V_{DDD5}	41	–	digital supply voltage 5
V_{SSD8}	42	–	digital ground 8
V_{DDD6}	43	–	digital supply voltage 6
V_{DDD7}	44	–	digital supply voltage 7
PDO7	45	O	parallel data output (bit 7)
n.c.	46	–	not connected
V_{SSD9}	47	–	digital ground 9
PDOERR	48	0	transport error indicator
PDOVAL	49	O	data valid indicator
PDOSYNC	50	0	transport packet synchronization signal
V_{SSD10}	51	–	digital ground 10
SCL	52	I	serial clock input of I^2C-bus
SDA	53	I/O	serial data of I^2C-bus
$\overline{INT}$	54	O	interrupt output (active LOW)
A0	55	I	I^2C-bus hardware address
RSLOCK	56	O	Reed-Solomon lock indicator
VLOCK	57	O	Viterbi lock indicator
DLOCK	58	O	demodulator lock indicator
V_{DDD8}	59	–	digital supply voltage 8
V_{DDD9}	60	–	digital supply voltage 9
TEST	61	I	test pin (normally connected to ground)
TRST	62	I	BST optional asynchronous reset (normally connected to ground)
TCK	63	I	BST dedicated test clock (normally connected to ground)
SCLT	64	I	serial clock of I^2C-bus loop-through
SDAT	65	I/O	serial data of I^2C-bus loop-through
V_{DDD10}	66	–	digital supply voltage 10
V_{SSD11}	67	–	digital ground 11
V_{SSD12}	68	–	digital ground 12
TMS	69	I	BST input control signal (normally connected to ground)
TDO	70	O	BST serial test data output
TDI	71	I	BST serial test data in (normally connected to ground)
V_{DDD11}	72	–	digital supply voltage 11
V_{SSD13}	73	–	digital ground 13
$V_{SSD(AD)}$	74	–	digital ground ADC
$V_{DDD(AD)}$	75	–	digital supply ADC
$V_{ref(B)}$	76	O	bottom reference voltage for ADC
V_{SSA1}	77	–	analog ground 1
QA	78	–	analog input Q
$V_{ref(Q)}$	79	O	AGC decoupling - Q path
IA	80	I	analog input I
V_{SSA2}	81	–	analog ground 2

SYMBOL	PIN	I/O	DESCRIPTION
$V_{ref(I)}$	82	O	AGC decoupling - I path
V_{DDA}	83	–	analog supply voltage
V_{DDXTAL}	84	–	supply voltage for crystal oscillator
XTALI	85	I	crystal oscillator input
XTALO	86	O	crystal oscillator output
V_{SSXTAL}	87	–	ground for crystal oscillator
V_{DDD12}	88	–	digital supply voltage 12
V_{DDD13}	89	–	digital supply voltage 13
V_{SSD14}	90	–	digital ground 14
D22	91	O	22 kHz output for dish control applications
V_{SSD15}	92	–	digital ground 15
V_{SSD16}	93	–	digital ground 16
V_{AGC}	94	O	AGC output voltage
$V_{SSD(test)}$	95	–	test pin, normally connected to ground
V_{DDD14}	96	–	digital supply voltage 14
V_{DDD15}	97	–	digital supply voltage 15
OUSTD	98	O	general purpose sigma-delta output
I0	99	I	digital I-input bit 0 (ADC bypass: LSB)
I1	100	I	digital I-input bit 1 (ADC bypass)



For compatibility in respect to the TDA8043 see Section “Pin compatibility”.

Fig.1 Pin configuration.

Pin compatibility

The TDA8044 is backwards pin compatible with the TDA8043, this means that the functional pins of the TDA8043 have been left unchanged on the TDA8044. However due to extra functionality of the TDA8044, some of the not connected pins of the TDA8043 have become functional pins on the TDA8044. Table 1 lists the modified pins of the TDA8044.

Table 1 Modified pins of the TDA8044

PIN	TDA8043 FUNCTION	TDA8044 SYMBOL	TDA8044 FUNCTION
4	not connected	CFS	clock frequency selection
5	not connected	V_{SSD2}	digital ground
26	not connected	P5	I/O expander bit 5
27	not connected	P4	I/O expander bit 4
36	not connected	V_{SSD6}	digital ground
37	not connected	V_{SSD7}	digital ground
39	not connected	POR	Power-on reset
47	not connected	V_{SSD9}	digital ground
64	not connected	SCLT	serial clock of I^2C-bus loop-through
65	not connected	SDAT	serial data of I^2C-bus loop-through
91	not connected	D22	22 kHz generation output
92	not connected	V_{SSD15}	digital ground
93	not connected	V_{SSD16}	digital ground
95	not connected	$V_{SSD(test)}$	test pin, connect to ground

If it is required to replace the TDA8043 with the TDA8044 and the pins with extra functionality are not required, then the following measures on the PCB layout must be taken to avoid I/O conflicts in the TDA8044:

- Pin numbers 4, 5, 26, 27, 36, 37, 47, 65, 92, 93 and 95 must be put to ground
- Pin numbers 39, 64 and 91 must be left not connected.

With these measures it is possible to use the TDA8043 and the TDA8044 on the same PCB without any problems. In order to use pins with the extra functionality of the TDA8044, PCB layout changes are necessary.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage pins		–0.3	+3.55	V
V_{max}	maximum voltage on all pins		0	V_{DD}	V
P_{tot}	total power dissipation				
	TDA8044	T_{amb} = 70 °C; note 1	–	1700	mW
	TDA8044A	T_{amb} = 70 °C; note 2	–	1250	mW
T_{stg}	IC storage temperature		–55	+150	°C
T_{amb}	ambient temperature	T_{amb} = 70 °C	0	70	°C
T_j	operating junction temperature		0	125	°C

Notes

1. Maximum power dissipation is specified for 96 MHz clock frequency, 45 Msymbols/s and a puncture rate of $^7/_8$.
2. Maximum power dissipation is specified for 64 MHz clock frequency, 30 Msymbols/s and a puncture rate of $^7/_8$.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However it is good practice to take normal precautions appropriate to handling MOS devices (see *“Handling MOS devices”*).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA8044		34	K/W
	TDA8044A		45	K/W

APPLICATION INFORMATION

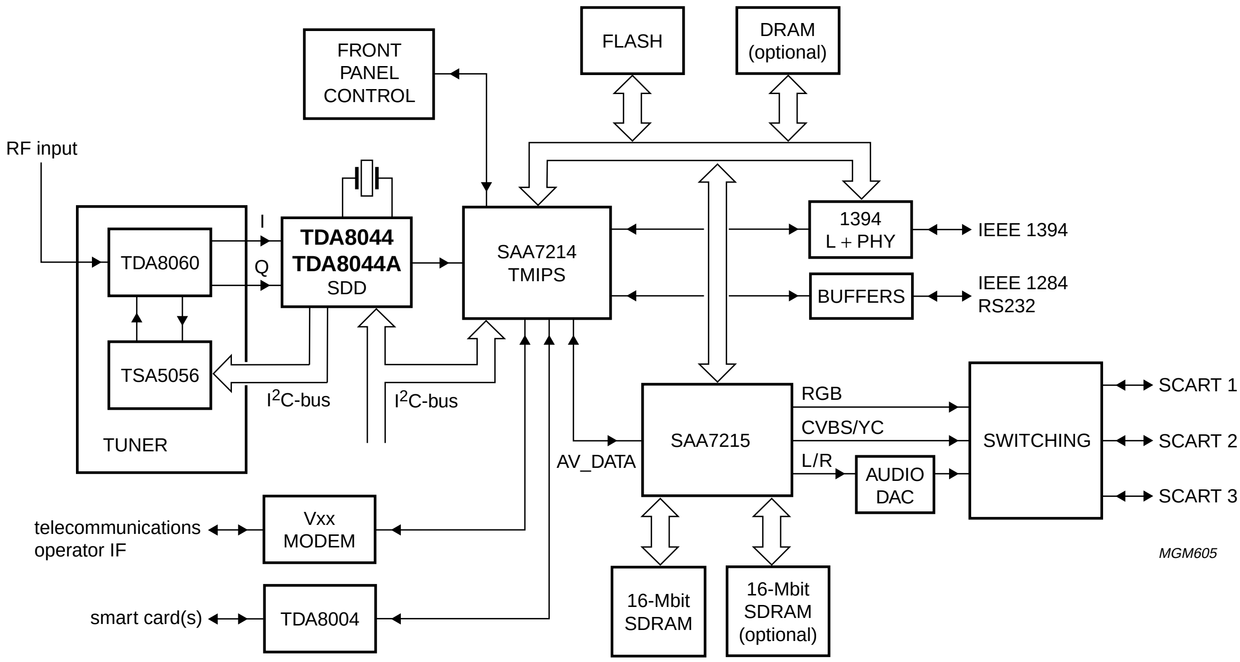
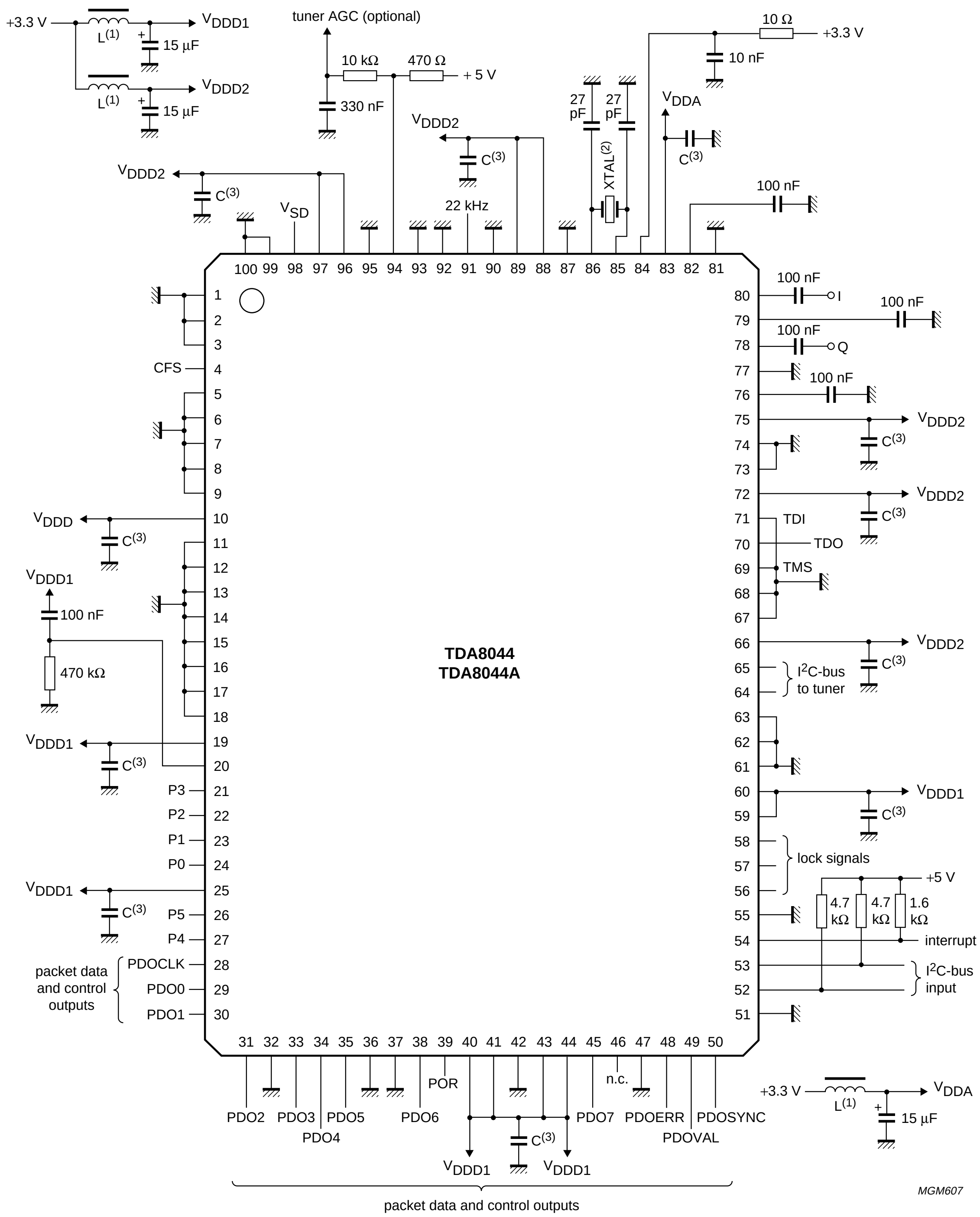


Fig.2 Satellite set-top decoder concept.

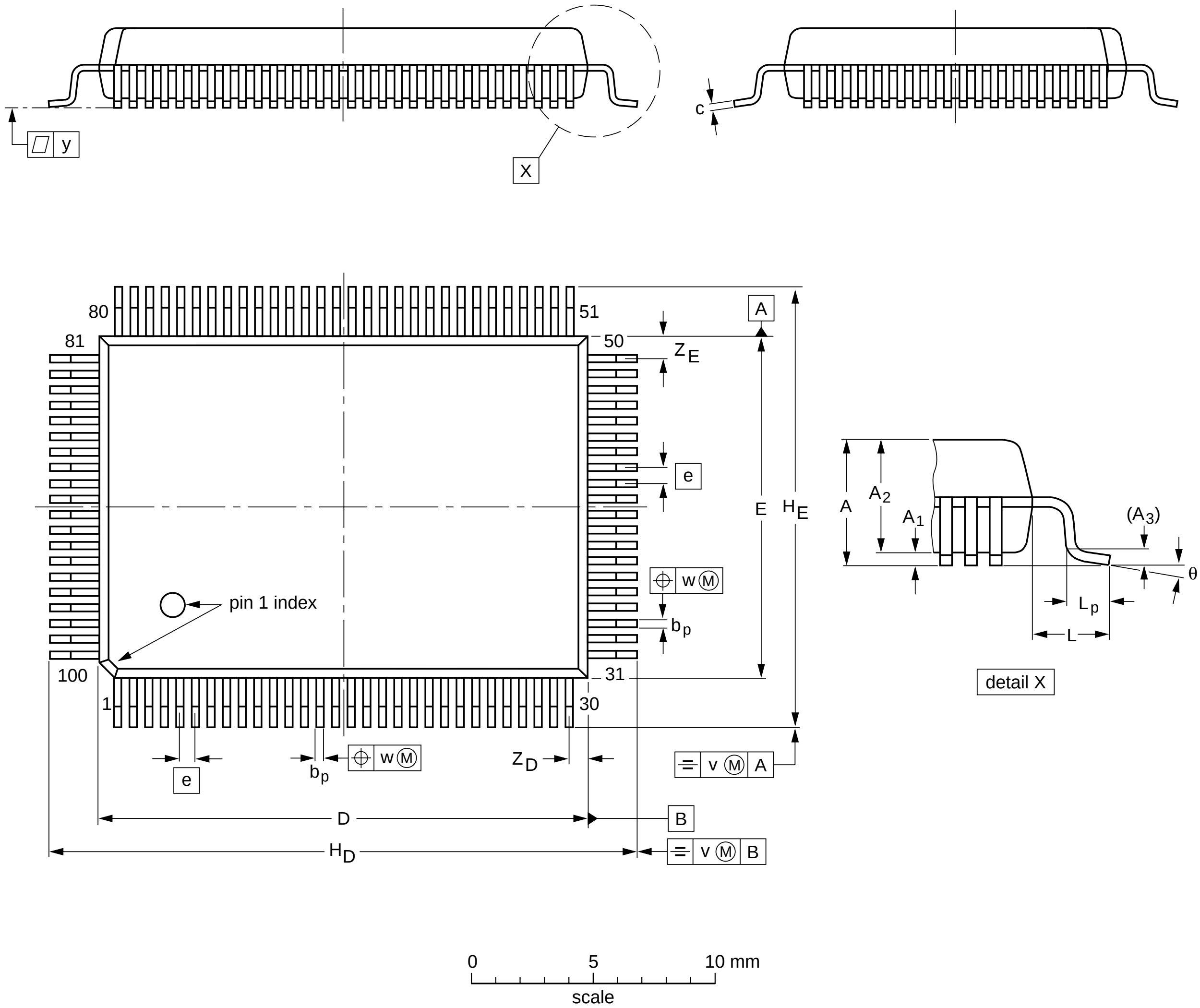


(1) B = SMD bead type C8D8.9/3/3 Grade 4S2.
(2) f_{xtal} = 4 MHz (fundamental).
(3) C = 6.8 nF, SMD.

Fig.3 Application diagram.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2		MO-112				~~97-08-01~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimum results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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