

DATA SHEET

TDA8001 Smart card interface

Product specification
Supersedes data of 1995 Feb 01
File under Integrated Circuits, IC02

1996 Dec 12

Smart card interface

TDA8001

FEATURES

- Protected I/O line
- V_{CC} regulation (5 V \pm 5%, 100 mA max. with controlled rise and fall times)
- V_{PP} generation (12.5, 15 or 21 V \pm 2.5%, 50 mA max., with controlled rise and fall times) (only at TDA8001 and TDA8001T)
- Clock generation (up to 10 MHz), with synchronous frequency doubling
- Overload, thermal and card extraction protections
- Current limitation in case of short-circuit
- Idle mode and special circuitry for spikes killing during powering on and off
- Two voltage supervisors (digital and analog supplies)
- Automatic activation and deactivation sequences through an independent internal clock
- Enhanced ESD protections on card side (4 kV min.)
- Easy chaining for multiple card readers
- ISO 7816 compatibility.

APPLICATIONS

- Pay TV (multistandards conditional access system, videoguard, newsript)
- Multi-application smart card readers (banking, vending machine, electronic payment identification).

GENERAL DESCRIPTION

The TDA8001 is a complete, low-cost analog interface which can be positioned between an asynchronous smart card (ISO 7816) and a microcontroller. It is directly compatible with the new Datacom chip verifier.

The complete supply, protection and control functions are realized with only a few external components, making this product very attractive for consumer applications (see Chapter "Application information").

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8001; TDA8001A	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
TDA8001T; TDA8001AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DD}	supply voltage		6.7	–	18	V
I _{DD}	supply current	idle mode; V _{DD} = 12 V	–	32	–	mA
		active modes; unloaded	–	45	–	mA
V _{th2}	threshold voltage on V _{SUP}		4.5	–	4.72	V
V _{th4}	threshold voltage on V _{DD}		6	–	6.5	V
V _{CC}	card supply voltage	including static and dynamic loads on 100 nF capacitor	4.75	5.0	5.25	V
I _{CC}	card supply current	operating	–	–	–100	mA
		detection	–	–150	–	mA
		limitation	–	–	–200	mA
V _H	high voltage supply for V _{PP}		–	–	30	V
V _{PP}	card programming voltage (only at TDA8001 and TDA8001T) (P = 5, 12.5, 15 and 21 V)	including static and dynamic loads on 100 nF capacitor	P – 2.5%	–	P + 2.5%	V
I _{PP}	programming current (read or write mode)	operating	–	–	–50	mA
		detection	–	–75	–	mA
		limitation	–	–	–100	mA
SR	slew rate on V _{CC} and V _{PP} (rise and fall)	maximum load capacitor 150 nF	–	0.38	–	V/μs
t _{de}	deactivation cycle duration		75	100	125	μs
f _{clk}	clock frequency		0	–	8	MHz
P _{tot}	continuous total power dissipation	TDA8001; T _{amb} = +70 °C; see Fig.10	–	–	0.92	W
		TDA8001T; T _{amb} = +70 °C; see Fig.11	–	–	2	W
T _{amb}	operating ambient temperature		0	–	+70	°C

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BLOCK DIAGRAM

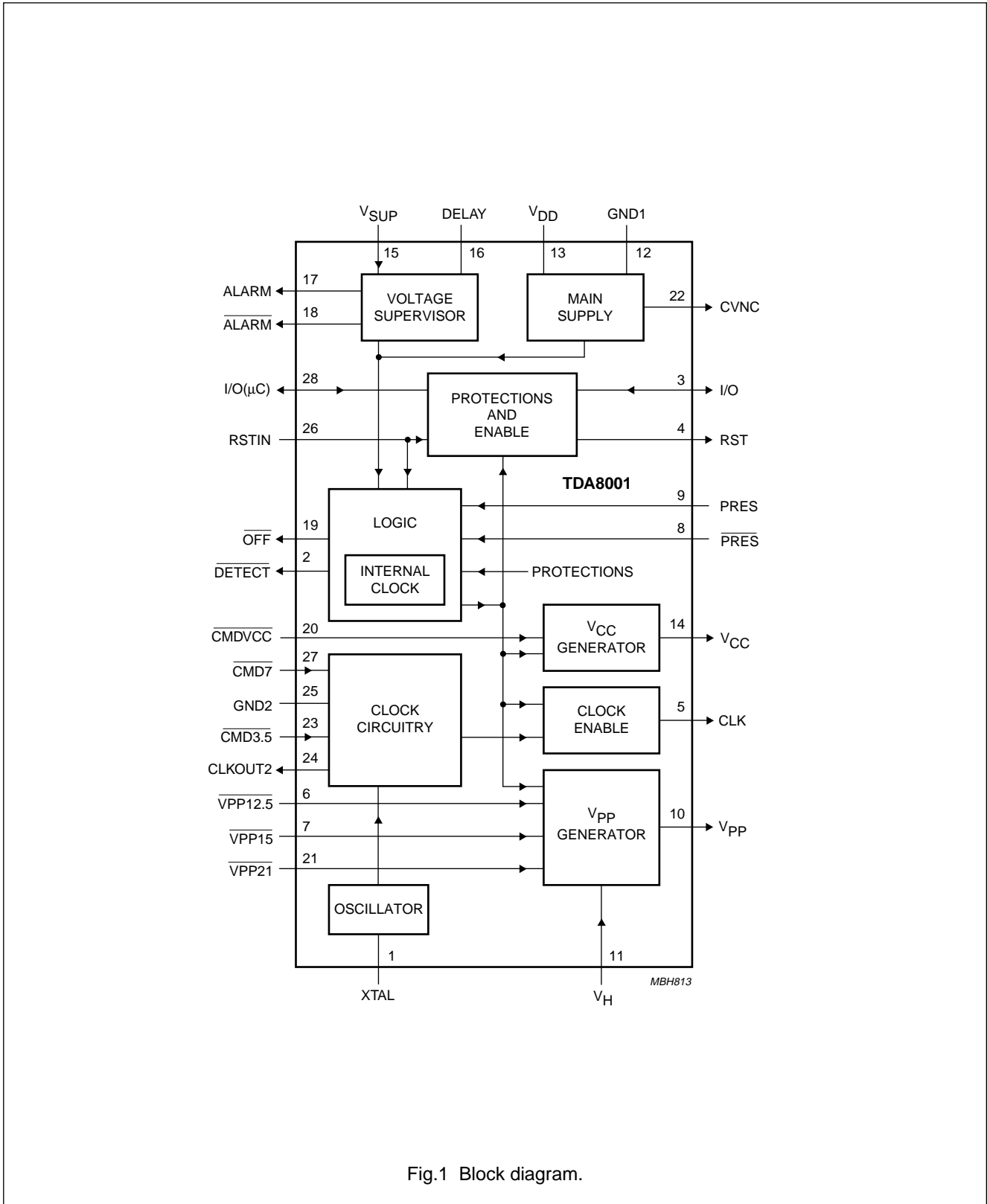


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN		DESCRIPTION
	TDA8001 TDA8001T	TDA8001A TDA8001AT	
XTAL	1	1	crystal connection
$\overline{\text{DETECT}}$	2	2	card extraction open collector output (active LOW)
I/O	3	3	data line to/from the card
RST	4	4	card reset output
CLK	5	5	clock output to the card
$\overline{\text{VPP12.5}}$	6	–	control input for applying the 12.5 V programming voltage (active LOW)
n.c.	–	6	not connected
$\overline{\text{VPP15}}$	7	–	control input for applying the 15 V programming voltage (active LOW)
n.c.	–	7	not connected
$\overline{\text{PRES}}$	8	8	card presence contact input (active LOW)
PRES	9	9	card presence contact input (active HIGH)
V _{PP}	10	–	card programming voltage output
n.c.	–	10	not connected
V _H	11	11	HIGH voltage supply for V _{PP} generation
GND1	12	12	ground 1
V _{DD}	13	13	positive supply voltage
V _{CC}	14	14	card supply output voltage
V _{SUP}	15	15	voltage supervisor input
DELAY	16	16	external capacitor connection for delayed reset timing
ALARM	17	17	open-collector reset output for the microcontroller (active HIGH)
$\overline{\text{ALARM}}$	18	18	open-collector reset output for the microcontroller (active LOW)
$\overline{\text{OFF}}$	19	19	open-collector interrupt output to the microcontroller (active LOW)
$\overline{\text{CMDVCC}}$	20	20	control input for applying supply voltage to the card (active LOW)
$\overline{\text{VPP21}}$	21	–	control input for applying the 21 V programming voltage (active LOW)
n.c.	–	21	not connected
CVNC	22	22	internally generated 5 V reference, present when V _{DD} is on; to be decoupled externally (100 nF)
CMD3.5 or CDMTC	23	23	control input for having the crystal frequency divided-by-4 at pin CLK
CLKOUT2	24	24	clock output to the microcontroller, or any other R4590 (crystal frequency divided by two)
GND2	25	25	ground 2
RSTIN	26	26	card reset input from the microcontroller (active HIGH)
$\overline{\text{CMD7}}$ or CDMS	27	27	control input for having the crystal frequency divided by 2 at pin CLK
I/O(μC)	28	28	data line to/from the microcontroller

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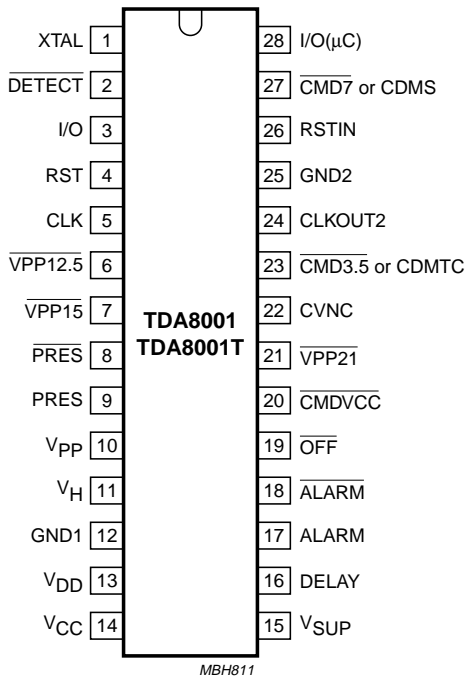


Fig.2 Pin configuration.

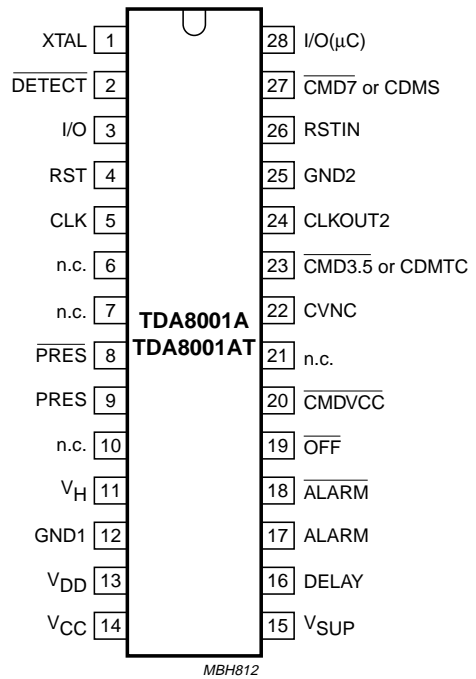


Fig.3 Pin configuration.

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FUNCTIONAL DESCRIPTION**Power supply**

The circuit operates within a supply voltage range of 6.7 to 18 V. V_{DD} and GND are the supply pins. All card contacts remain inactive during power up or down.

POWER UP

The logic part is powered first and is in the reset condition until V_{DD} reaches V_{th1} . The sequencer is blocked until V_{DD} reaches $V_{th4} + V_{hys4}$.

POWER DOWN

When V_{DD} falls below V_{th4} , an automatic deactivation of the contacts is performed.

Voltage supervisor

This block surveys the 5 V supply of the microcontroller (V_{SUP}) in order to deliver a defined reset pulse and to avoid any transients on card contacts during power up or down of V_{SUP} . The voltage supervisor remains active even if V_{DD} is powered-down.

POWER ON

As long as V_{SUP} is below $V_{th2} + V_{hys2}$ the capacitor C_{DEL} , connected to pin DELAY, will be discharged. When V_{SUP} rises to the threshold level, C_{DEL} will be recharged. ALARM and \overline{ALARM} remain active, and the sequencer is blocked until the voltage on the DELAY line reaches V_{th3} .

POWER DOWN (see Fig.4)

If V_{SUP} falls below V_{th2} , C_{DEL} will be discharged, ALARM and \overline{ALARM} become active, and an automatic deactivation of the contacts is performed.

Clock circuitry (see Fig.5)

The clock signal (CLK) can be applied to the card in two different methods:

1. Generation by a crystal oscillator: the crystal, or the ceramic resonator (4 to 16 MHz) is connected to the XTAL pin.
2. Use of a signal frequency (up to 20 MHz), already present in the system and connected to the XTAL pin via a 10 nF capacitor (see Fig.14). In both cases the frequency is first divided-by-two.

If $\overline{CMD7}$ (respectively $\overline{CMD3.5}$) is LOW, the clock signal (its frequency again divided by two) is enabled and buffered before being fed to the CLK pin.

$\overline{CMD3.5}$ and internal ENRST are sampled in order to give the first clock pulse the correct width, and to avoid false pulses during frequency change.

The CLKOUT2 pins may be used to clock a microcontroller or an other TDA8001. The signal $\frac{1}{2} f_{xtal}$ is available when the circuit is powered up.

State diagram

Once activated, the circuit has six possible modes of operation:

- Idle
- Activation
- Read
- Write
- Deactivation
- Fault.

Figure 6 shows the way these modes are accessible.

IDLE MODE

After reset, the circuit enters the IDLE state. A minimum number of circuits are active while waiting for the microcontroller to start a session.

- All card contacts are inactive
- I/O(μ C) is high impedance
- Voltage generators are stopped
- Oscillator or XTAL input is running, delivering CLKOUT2
- Voltage supervisors are active.

The \overline{DETECT} line is HIGH if a card is present (PRES and \overline{PRES} active) and LOW if a card is not present. The OFF line is HIGH if no hardware problem is detected.

ACTIVATION SEQUENCE

From the IDLE mode, the circuit enters the ACTIVATION mode when the microcontroller sets the \overline{CMDVCC} line (active LOW). The I/O(μ C) signal must not be LOW. The internal circuitry is activated, the internal clock starts and the sequence according to ISO7816 is performed:

- V_{CC} rises from 0 to 5 V
- V_{PP} rises from 0 to 5 V and I/O is enabled
- CLK and RST are enabled.

The time interval between steps 1 and 2 is 16 μ s, and 64 μ s between steps 2 and 3 (see Fig.7).

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READ MODE

When the activation sequence is completed and, after the card has replied its Answer-to-Reset, the TDA8001 will be in the READ mode. Data is exchanged between the card and the microcontroller via the I/O line.

WRITE MODE

Cards with EPROM memory need a programming voltage (V_{PP}). When it is required to write to the internal memory of the card, the microcontroller sets one of the $\overline{VPP12.5}$, $\overline{VPP15}$ and $\overline{VPP21}$ lines LOW, according to the programming value given in the Answer-to-Reset. V_{PP} rises from 5 V to the selected value with a typical slew rate of $0.38 \text{ V}/\mu\text{s}$. In order to respect the ISO 7816 slopes, the circuit generates V_{PP} by charging and discharging an internal capacitor. The voltage on this capacitor is then amplified by a power stage gain of 5, powered via an external supply pin V_H (30 V max).

DEACTIVATION SEQUENCE (see Fig.8)

When the session is completed, the microcontroller sets the \overline{CMDVCC} line to its HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back:

- RST falls to LOW and CLK is stopped
- I/O(μC) becomes high impedance and V_{PP} falls to 0 V
- V_{CC} falls to 0 V.

The circuit returns to the IDLE mode on the next rising edge of the clock.

PROTECTIONS

Main fault conditions are monitored by the circuit:

- Short-circuit or overcurrent on V_{CC}
- Short-circuit or overcurrent on V_{PP}
- Card extraction during transaction
- Overheating problem
- V_{SUP} drop-out
- V_{DD} drop-out.

When one of these fault conditions is detected, the circuit pulls the interrupt line \overline{OFF} to its active LOW state and returns to the FAULT mode. The current on I/O is internally limited to 5 mA.

FAULT MODE (see Fig.9)

When a fault condition is written to the microcontroller via the \overline{OFF} line, the circuit initiates a deactivation sequence. After the deactivation sequence has been completed, the \overline{OFF} line is reset to its HIGH state after the microcontroller has reset the \overline{CMDVCC} line HIGH.

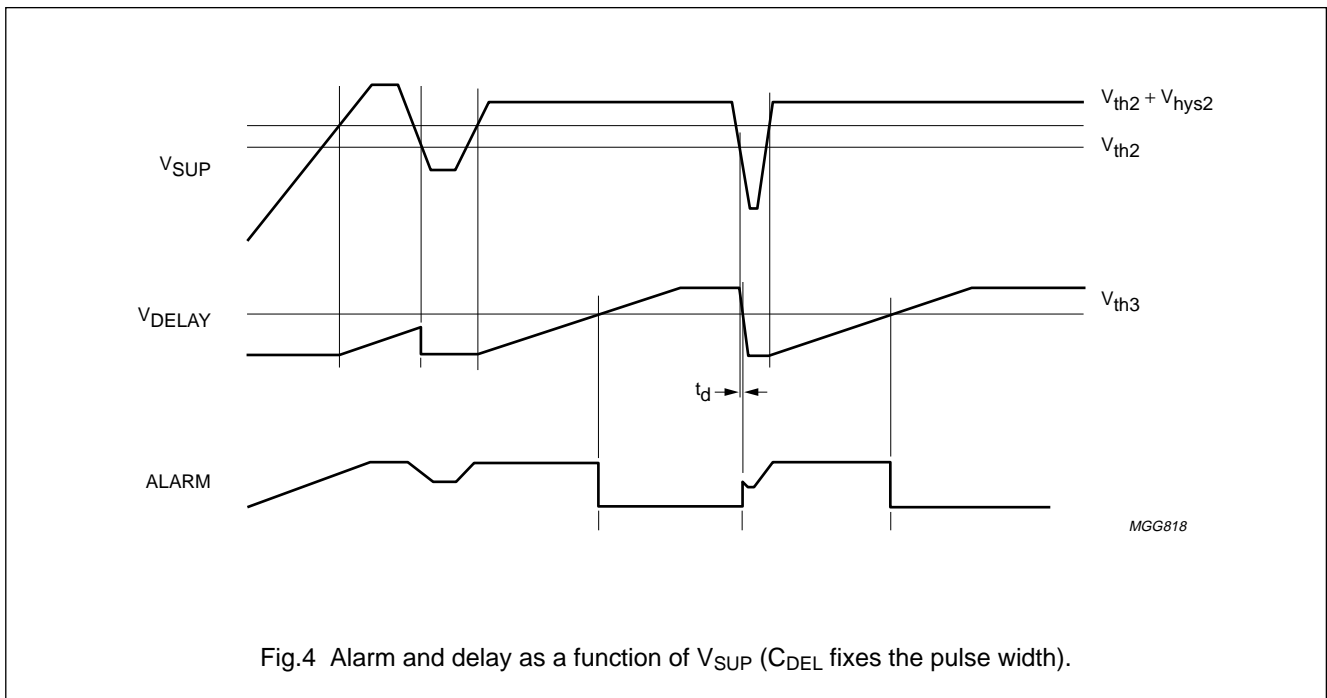
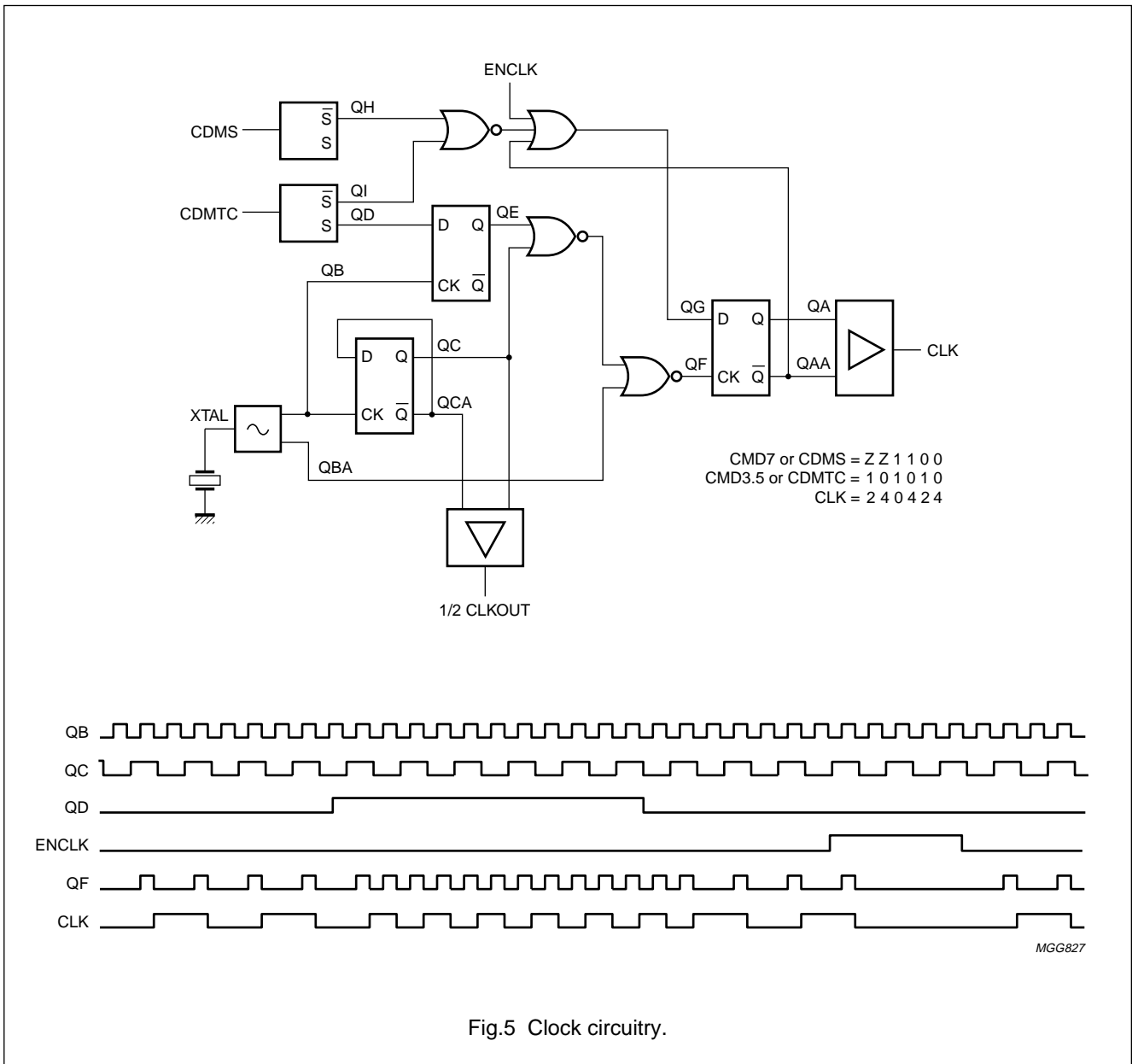


Fig.4 Alarm and delay as a function of V_{SUP} (C_{DEL} fixes the pulse width).

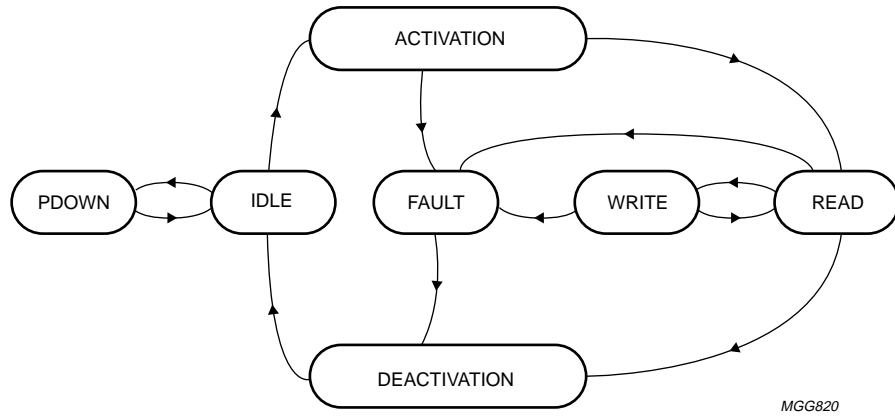
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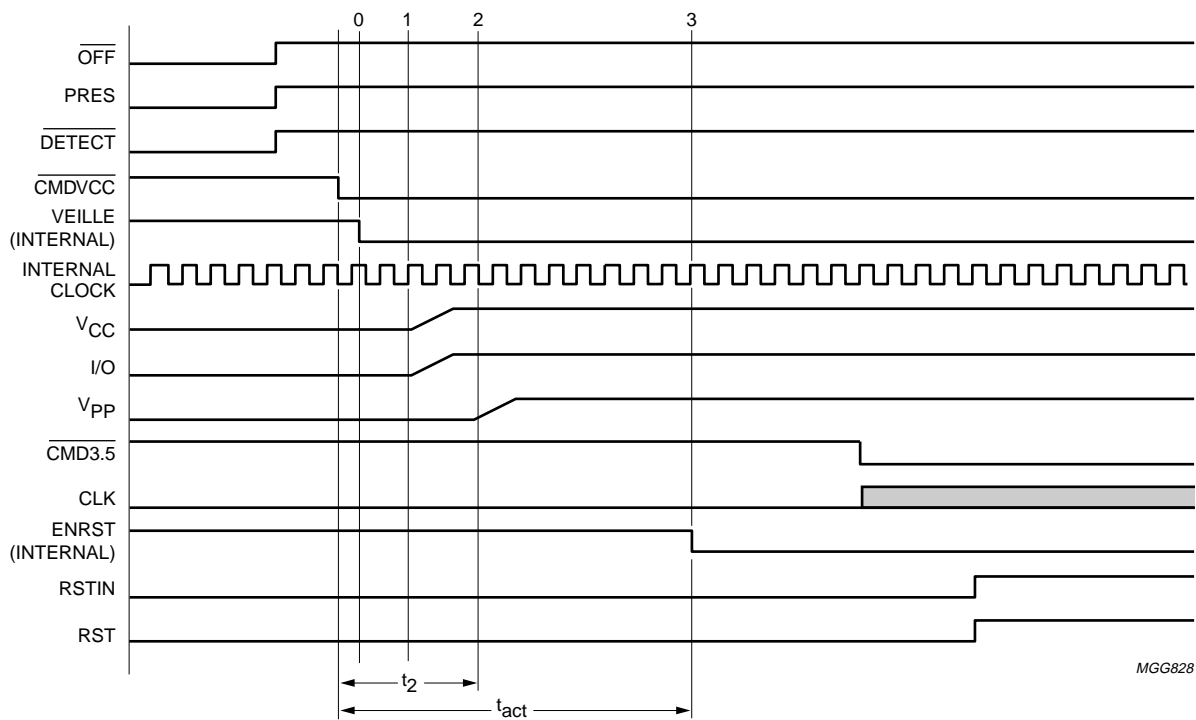
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Fig.6 State diagram.



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Fig.7 Activation sequence.

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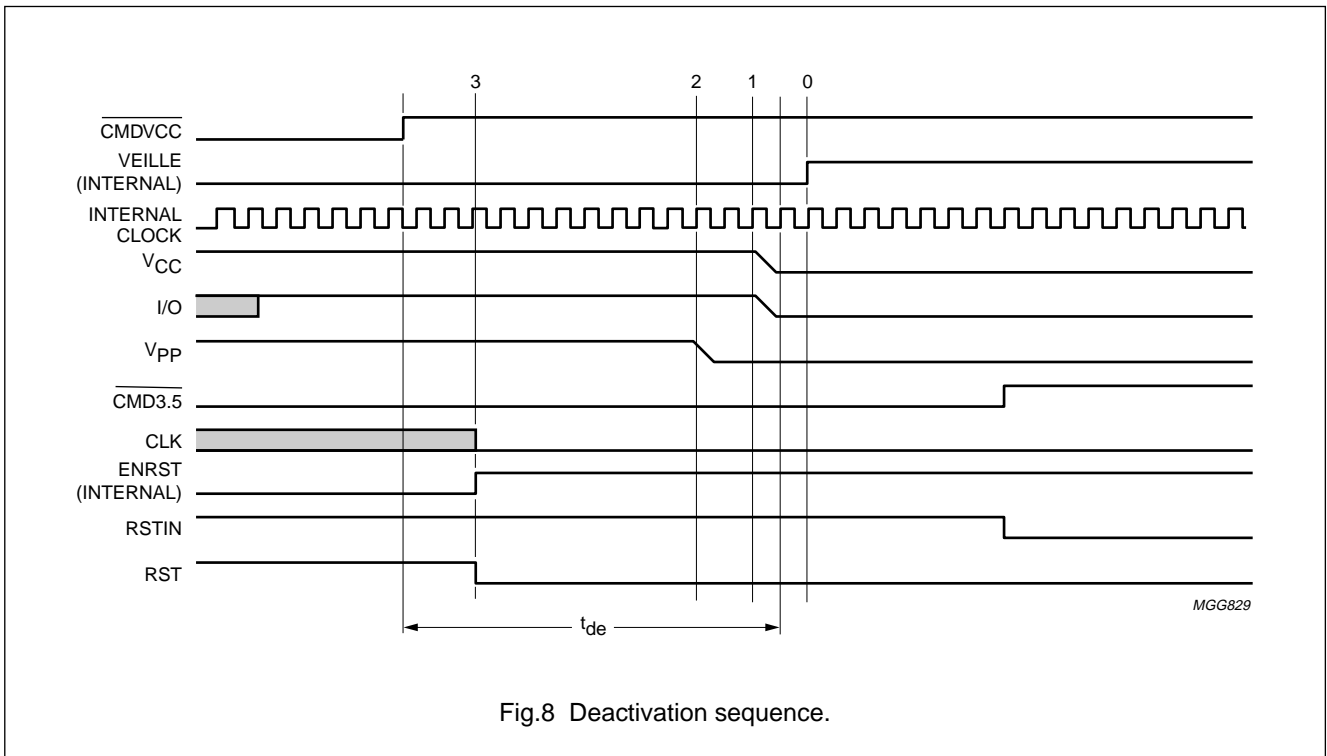


Fig.8 Deactivation sequence.

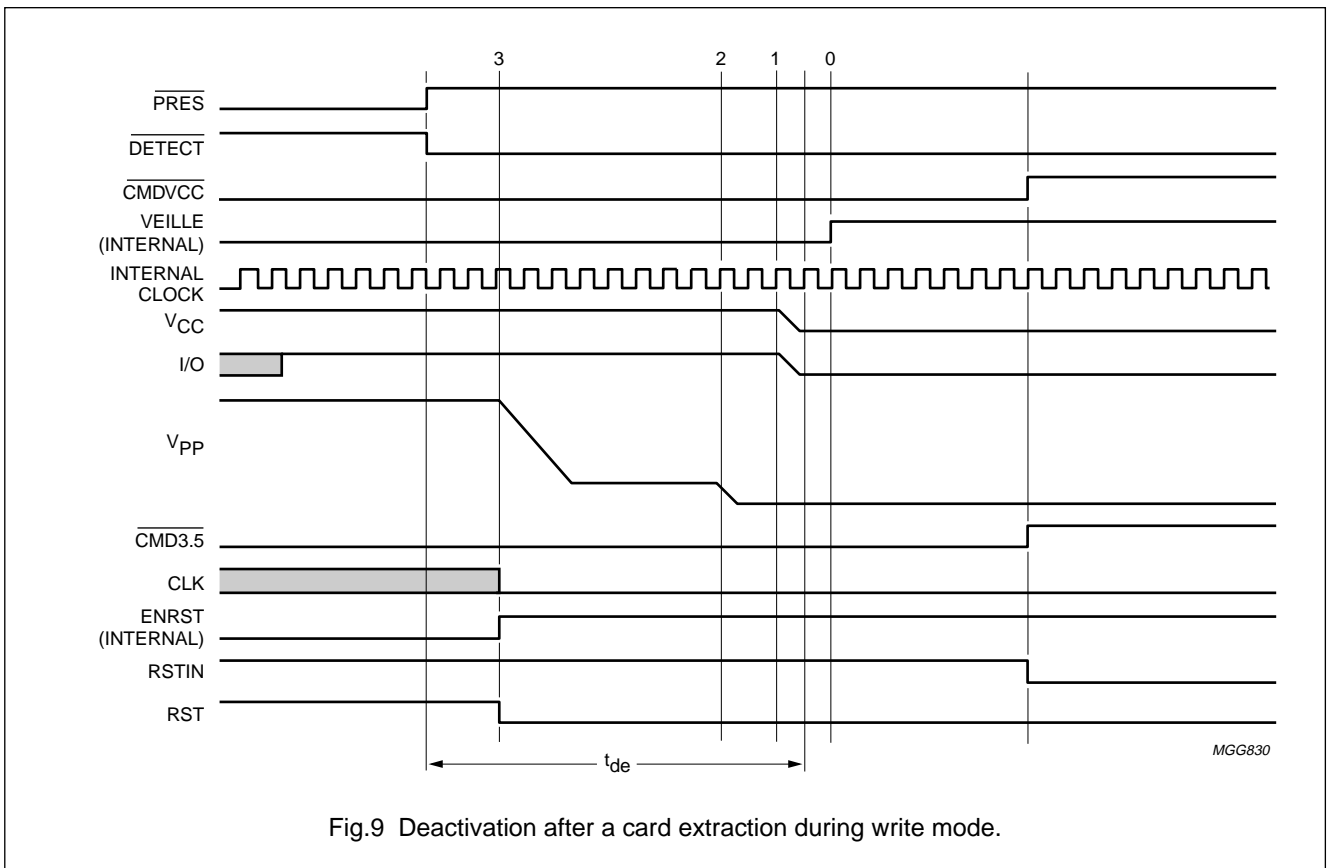


Fig.9 Deactivation after a card extraction during write mode.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

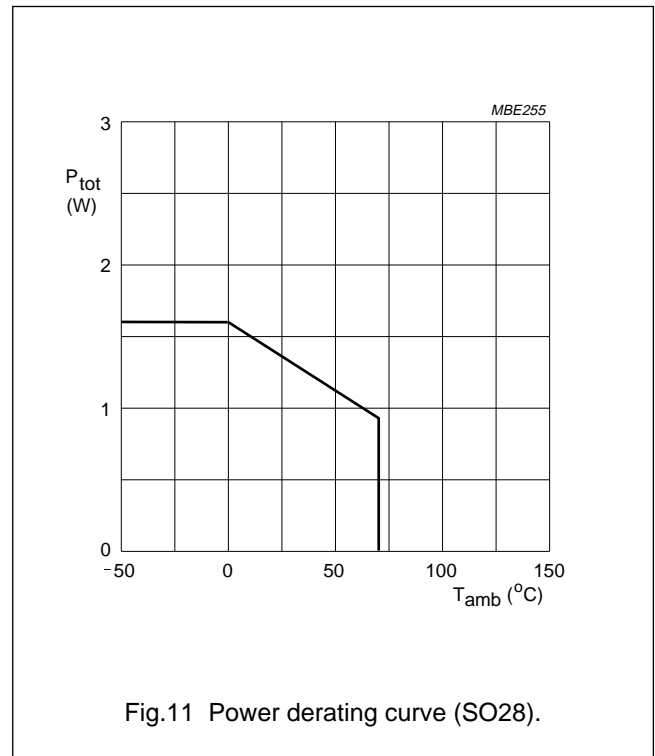
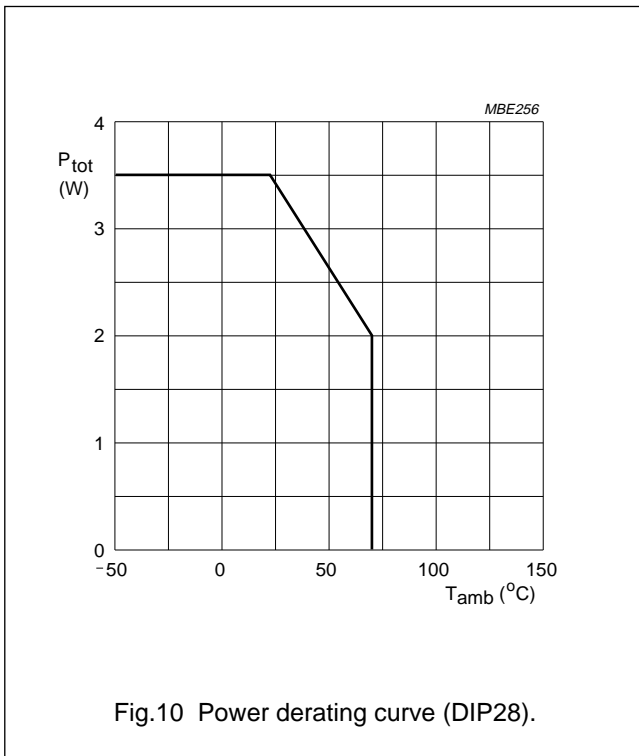
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DD}	supply voltage		-0.3	18	V
V _{x1}	voltage on pins $\overline{VPP21}$, $\overline{VPP15}$, $\overline{VPP12.5}$, \overline{PRES} , \overline{PRES} , \overline{CMDVCC} , \overline{OFF} , \overline{ALARM} , \overline{DETECT} and \overline{RSTIN}		0	V _{DD}	V
V _H	voltage on pin V _H		0	30	V
V _{PP}	voltage on pin V _{PP}		0	V _H	V
V _{SUP}	voltage on pin V _{SUP}		0	12	V
V _{x2}	voltage on pins \overline{ALARM} and \overline{DELAY}		0	V _{SUP}	V
V _{x3}	voltage on pins XTAL, I/O(μ C), $\overline{CLKOUT2}$, $\overline{CMD7}$, $\overline{CMD3.5}$ and \overline{CVNC}		0	6.0	V
V _{x4}	voltage on pins I/O, \overline{RST} , \overline{CLK} and V _{CC}	duration < 1 ms	0	7.0	V
P _{tot}	continuous total power dissipation	TDA8001; T _{amb} = +70 °C; note 1; see Fig.10	-	2	W
		TDA8001T; T _{amb} = +70 °C; note 1; see Fig.11	-	0.92	W
T _{stg}	storage temperature		-55	+150	°C
V _{es}	electrostatic voltage on pins I/O, V _{CC} , V _{PP} , \overline{RST} , \overline{CLK} , \overline{PRES} and \overline{PRES}		-6	+6	kV
	electrostatic voltage on other pins		-2	+2	kV

Note

1. $P_{tot} = V_{DD} \times (I_{DD(unloaded)} + \sum I_{signals}) + I_{CC} \times (V_{DD} - V_{CC}) + \max.\{(V_H - V_{PP}) \times I_{PP(read)} + (V_H - V_{PP}) \times I_{PP(write)}\} + V_H \times I_{H(unloaded)} + V_{SUP} \times I_{SUP} + (V_{DD} - CVNC) \times I_{CVNC}$, where 'signals' means all signal pins, except supply pins.

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HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM 1500 Ω, 100 pF) 3 pulses positive and 3 pulse negative on each pin referenced to ground.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient in free air		
	SOT117-1	30	K/W
	SOT136-1	70	K/W

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CHARACTERISTICS

$V_{DD} = 12\text{ V}$; $V_H = 25\text{ V}$; $V_{SUP} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		6.7	–	18	V
I_{DD}	supply current	idle mode; $V_{DD} = 8\text{ V}$	20	30	38	mA
		idle mode; $V_{DD} = 18\text{ V}$	22	34	42	mA
		active mode; unloaded	35	45	55	mA
V_{th1}	threshold voltage for power-on reset		–	3.0	4.0	V
V_{th4}	threshold voltage on V_{DD} (falling)		6.0	–	6.5	V
V_{hys4}	hysteresis on V_{th4}		50	–	200	mV
Voltage supervisor						
V_{SUP}	voltage supply for the supervisor		–	5.0	–	V
I_{SUP}	input current at V_{SUP}		–	1.8	2.4	mA
V_{th2}	threshold voltage on V_{SUP} (falling)		4.5	–	4.72	V
V_{hys2}	hysteresis on V_{th2}		10	–	80	mV
V_{th3}	threshold voltage on DELAY		2.35	–	2.65	V
I_{DEL}	output current at DELAY	pin grounded (charge)	–5	–	–2	μA
		$V_{DEL} = 4\text{ V}$ (discharge)	6	–	–	mA
V_{DEL}	voltage on pin DELAY		–	–	3.5	V
ALARM, $\overline{\text{ALARM}}$ (open-collector outputs)						
I_{OH}	HIGH level output current on pin $\overline{\text{ALARM}}$	$V_{OH} = 5\text{ V}$	–	–	25	μA
V_{OL}	LOW level output voltage on pin $\overline{\text{ALARM}}$	$I_{OL} = 2\text{ mA}$	–	–	0.4	V
I_{OL}	LOW level output current on pin $\overline{\text{ALARM}}$	$V_{OL} = 0\text{ V}$	–	–	–25	μA
V_{OH}	HIGH level output voltage on pin $\overline{\text{ALARM}}$	$I_{OH} = -2\text{ mA}$	$V_{SUP} - 1$	–	–	V
t_d	delay between V_{SUP} and $\overline{\text{ALARM}}$	$C_{DEL} = 47\text{ nF}$; see Fig.4	–	–	10	μs
t_{pulse}	$\overline{\text{ALARM}}$ pulse width	$C_{DEL} = 47\text{ nF}$	15	–	50	ms
Interrupt lines $\overline{\text{OFF}}$ and $\overline{\text{DETECT}}$ (open-collector)						
I_{OH}	HIGH level output current	$V_{OH} = 5\text{ V}$	–	–	25	μA
V_{OL}	LOW level output voltage	$I_{OL} = 1\text{ mA}$	–	–	0.4	V
Logic inputs ($\overline{\text{CMDVCC}}$, $\overline{\text{VPP21}}$, $\overline{\text{VPP15}}$, $\overline{\text{VPP12.5}}$, $\overline{\text{CMD7}}$, $\overline{\text{CMD3.5}}$, $\overline{\text{PRES}}$, $\overline{\text{PRES}}$ and $\overline{\text{RSTIN}}$); note 1						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		1.5	–	–	V
I_{IL}	LOW level input current	$V_{IL} = 0\text{ V}$	–	–	–10	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IH}	HIGH level input current	$V_{IH} = 5\text{ V}$	–	–	10	μA
Reset output to the card (RST)						
V_{IDLE}	output voltage in IDLE		–	–	0.4	V
V_{OL}	LOW level output voltage	$I_{OL} = 200\ \mu\text{A}$	–	–	0.45	V
V_{OH}	HIGH level output voltage	$I_{OH} = -200\ \mu\text{A}$	4.3	–	V_{CC}	V
		$I_{OH} = -10\ \mu\text{A}$	$V_{CC} - 0.7$	–	V_{CC}	V
t_{RST}	delay between RSTIN and RST	RST enabled; see Fig.7	–	–	2	μs
Clock output to the card (CLK)						
V_{IDLE}	output voltage in IDLE		–	–	0.4	V
V_{OL}	LOW level output voltage	$I_{OL} = 200\ \mu\text{A}$	–	–	0.4	V
V_{OH}	HIGH level output voltage	$I_{OH} = -200\ \mu\text{A}$	2.4	–	V_{CC}	V
		$I_{OH} = -20\ \mu\text{A}$	$0.7V_{CC}$	–	V_{CC}	V
		$I_{OH} = -10\ \mu\text{A}$	$V_{CC} - 0.7$	–	V_{CC}	V
t_r	rise time	$C_L = 30\ \text{pF}$; note 2	–	–	14	ns
t_f	fall time	$C_L = 30\ \text{pF}$; note 2	–	–	14	ns
δ	duty factor	$C_L = 30\ \text{pF}$; note 2	45	–	55	%
Card programming voltage (V_{PP})						
V_{PP}	output voltage	idle mode	–	–	0.4	V
		read mode	$V_{CC} - 4\%$	–	$V_{CC} + 4\%$	V
		write mode; $I_{PP} < 50\ \text{mA}$	$P - 2.5\%^{(3)}$	–	$P + 2.5\%^{(3)}$	V
		$\Delta I_{PP}/\Delta t < 40\ \text{mA}/100\ \text{ns}$; note 4	$P - 2.5\%^{(3)}$	–	$P + 2.5\%^{(3)}$	V
I_{PP}	output current	active; from 0 to P ⁽³⁾	–	–	–50	mA
		V_{PP} shorted to GND	–	–	–100	mA
SR	slew rate	up or down	0.3	0.4	0.5	V/ μs
High voltage input (V_H)						
V_H	input voltage		–	–	30	V
I_H	input current at V_H	idle mode; active mode; unloaded	4	–	6	mA
		$P = 5\ \text{V}$	5	–	9	mA
		$P = 12.5\ \text{V}$	6.5	–	10.5	mA
		$P = 15\ \text{V}$	7	–	11	mA
		$P = 21\ \text{V}$	8	–	12	mA
$V_H - V_{PP}$	voltage drop		–	–	2.2	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Card supply voltage (V_{CC})						
V _{CC}	output voltage	idle mode; active mode	–	–	0.4	V
		I _{CC} < 100 mA	4.75	–	5.25	V
		ΔI _{PP} /Δt < 100 mA/100 ns; note 4	4.75	–	5.25	V
I _{CC}	output current	V _{CC} from 0 to 5 V	–	–	–100	mA
		V _{CC} shorted to GND	–	–	–200	mA
SR	slew rate	up or down	0.3	0.4	0.5	V/μs
5 V reference output voltage (CVNC)						
V _{CVNC}	output voltage at pin CVNC		4.5	5.0	5.5	V
I _{CVNC}	output current at pin CVNC		–	–	–50	mA
Crystal connection (XTAL)						
R _{xtal(neg)}	negative resistance at pin XTAL	2 MHz < f _i < 16 MHz; note 5	–	–	300	Ω
V _{xtal}	DC voltage at pin XTAL		3.0	–	4.0	V
f _{xtal}	resonant frequency		4	–	16	MHz
	external frequency		0	–	20	MHz
Clock output (CLKOUT2)						
f _{CLKOUT2}	frequency on CLKOUT2		1	–	8	MHz
V _{OL}	LOW level output voltage	I _{OL} = 2 mA	–	–	0.4	V
V _{OH}	HIGH level output voltage	I _{OH} = –200 μA	3.0	–	–	V
		I _{OH} = –10 μA	4.0	–	–	V
t _r , t _f	rise and fall times	C _L = 15 pF; note 2	–	–	25	ns
δ	duty factor	C _L = 15 pF; note 2	40	–	60	%
Data line [I/O, I/O(μC)]						
V _{OH}	HIGH level output voltage on pin I/O	4.5 V < V _{SUP} < 5.5 V; 4.5 V < V _{I/O(μC)} < 5.5 V; I _{OH} = –20 μA	4.0	–	V _{CC} + 0.1	V
		4.5 V < V _{SUP} < 5.5 V; 4.5 V < V _{I/O(μC)} < 5.5 V; I _{OH} = –200 μA	2.4	–	–	V
V _{OL}	LOW level output voltage on pin I/O	I _{I/O} = 1 mA; I/O(μC) grounded	–	–	100	mV
I _{IL}	LOW level input current on pin I/O(μC)	I/O(μC) grounded	–	–	–500	μA
V _{OH}	HIGH level output voltage on pin I/O(μC)	4.5 V < V _{I/O} < 5.5 V	4.0	–	V _{SUP} + 0.2	V
V _{OL}	LOW level output voltage on pin I/O(μC)	I _{I/O(μC)} = 1 mA; I/O grounded	–	–	70	mV
I _{IL}	LOW level input current on pin I/O	I/O grounded	–	–	–500	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{IDLE}	voltage on pin I/O outside a session		–	–	0.4	V
Z _{IDLE}	impedance on pin I/O(μC) outside a session		10	–	–	MΩ
R _{pu}	internal pull-up resistance between pin I/O and V _{CC}		8	10	12	kΩ
t _r , t _f	rise and fall times	C _i = C _o = 30 pF	–	–	0.5	μs
Protections						
T _{sd}	shut-down local temperature		–	135	–	°C
I _{CC(sd)}	shut-down current at V _{CC}		–	–150	–	mA
I _{PP(sd)}	shut-down current at V _{PP}		–	–75	–	mA
I _{I/O(lim)}	current limitation on pin I/O	from I/O to I/O(μC)	3	–	5	mA
Timing						
t _{act}	activation sequence duration	see Fig.7	–	110	–	μs
t _{de}	deactivation sequence duration	see Fig.8	–	100	–	μs
t ₃	start of the window for sending CLK to the card		–	–	70	μs
t ₅	end of the window for sending CLK to the card		80	–	–	μs
t _{st}	maximum pulse width on CMDV _{CC} before V _{CC} starts rising		–	–	30	μs

Notes

1. Pins $\overline{\text{CMDVCC}}$, $\overline{\text{VPP21}}$, $\overline{\text{VPP15}}$, $\overline{\text{VPP12.5}}$, $\overline{\text{CMD7}}$, $\overline{\text{CMD3.5}}$ and $\overline{\text{PRES}}$ are active LOW; pins RSTIN and PRES are active HIGH.
2. The transition time and duty cycle definitions are shown in Fig.12; $\delta = \frac{t_1}{t_1 + t_2}$.
3. P is the card programming voltage set by pin $\overline{\text{VPP12.5}}$, $\overline{\text{VPP15}}$ or $\overline{\text{VPP21}}$.
4. The tests for dynamic response of both V_{PP} and V_{CC} are performed at 1 Hz, 10 kHz, 100 kHz and 1 MHz, with a capacitive load of 100 nF.
5. This condition ensures proper starting of the oscillator with crystals having a series resistance up to 100 Ω.

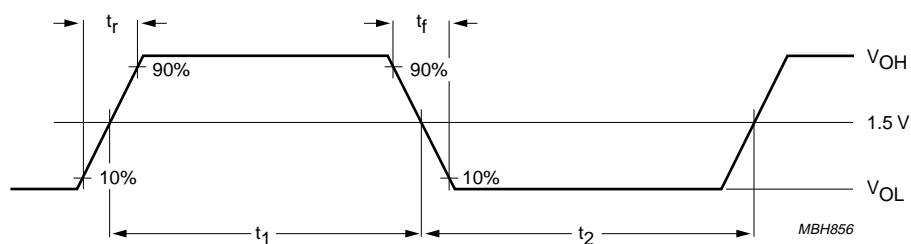


Fig.12 Definition of transition times.

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INTERNAL PIN CONFIGURATION

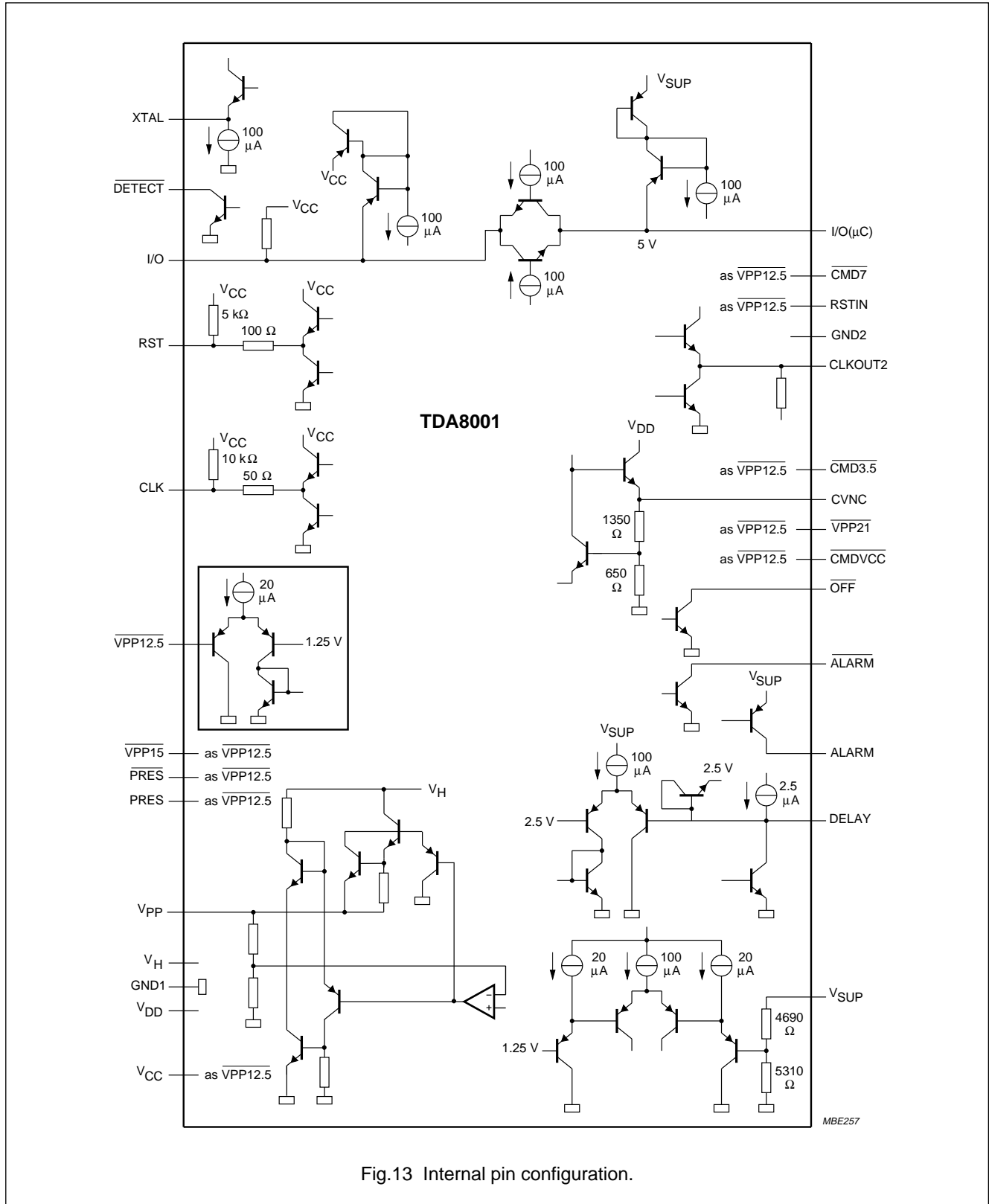
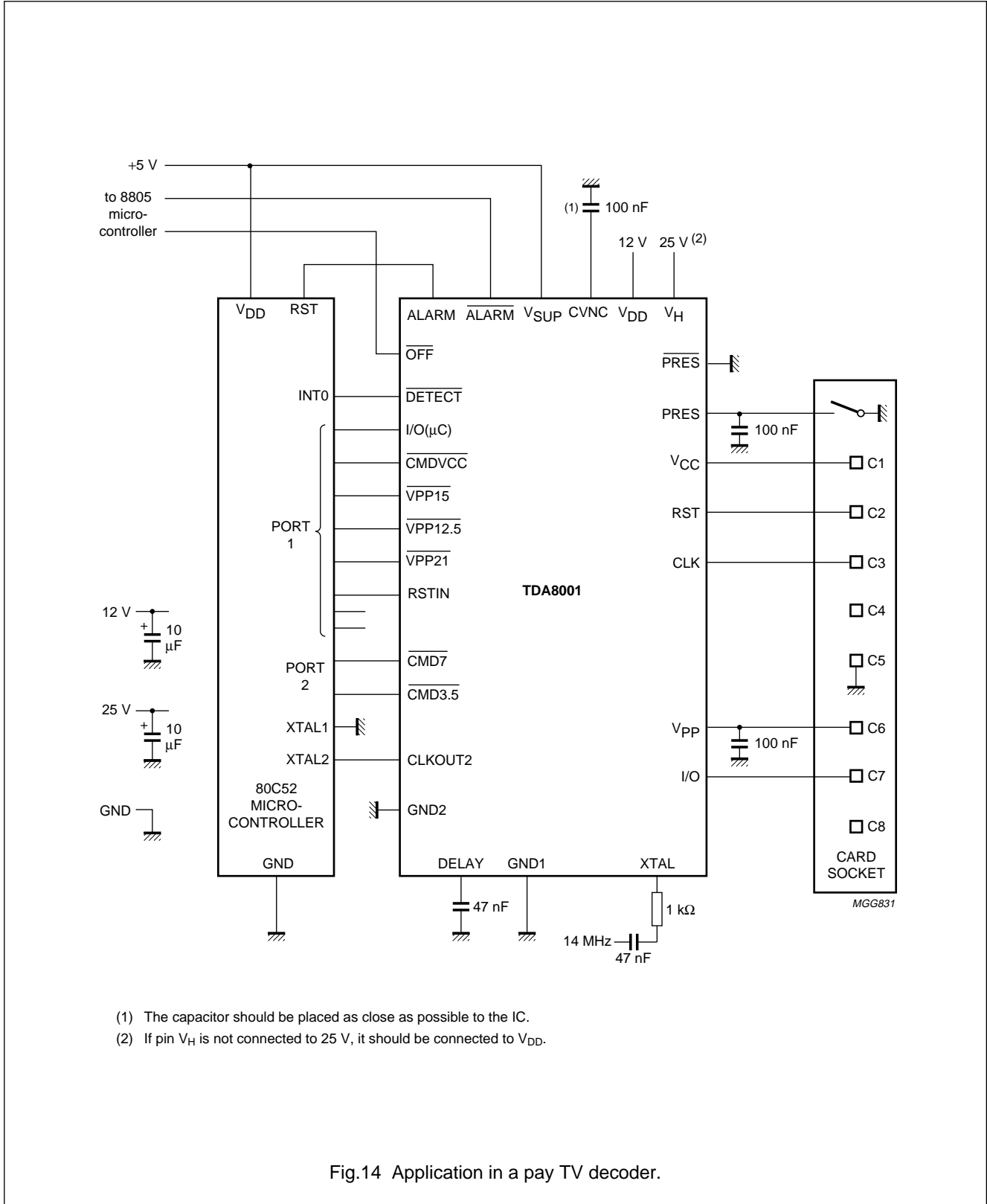


Fig.13 Internal pin configuration.

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APPLICATION INFORMATION



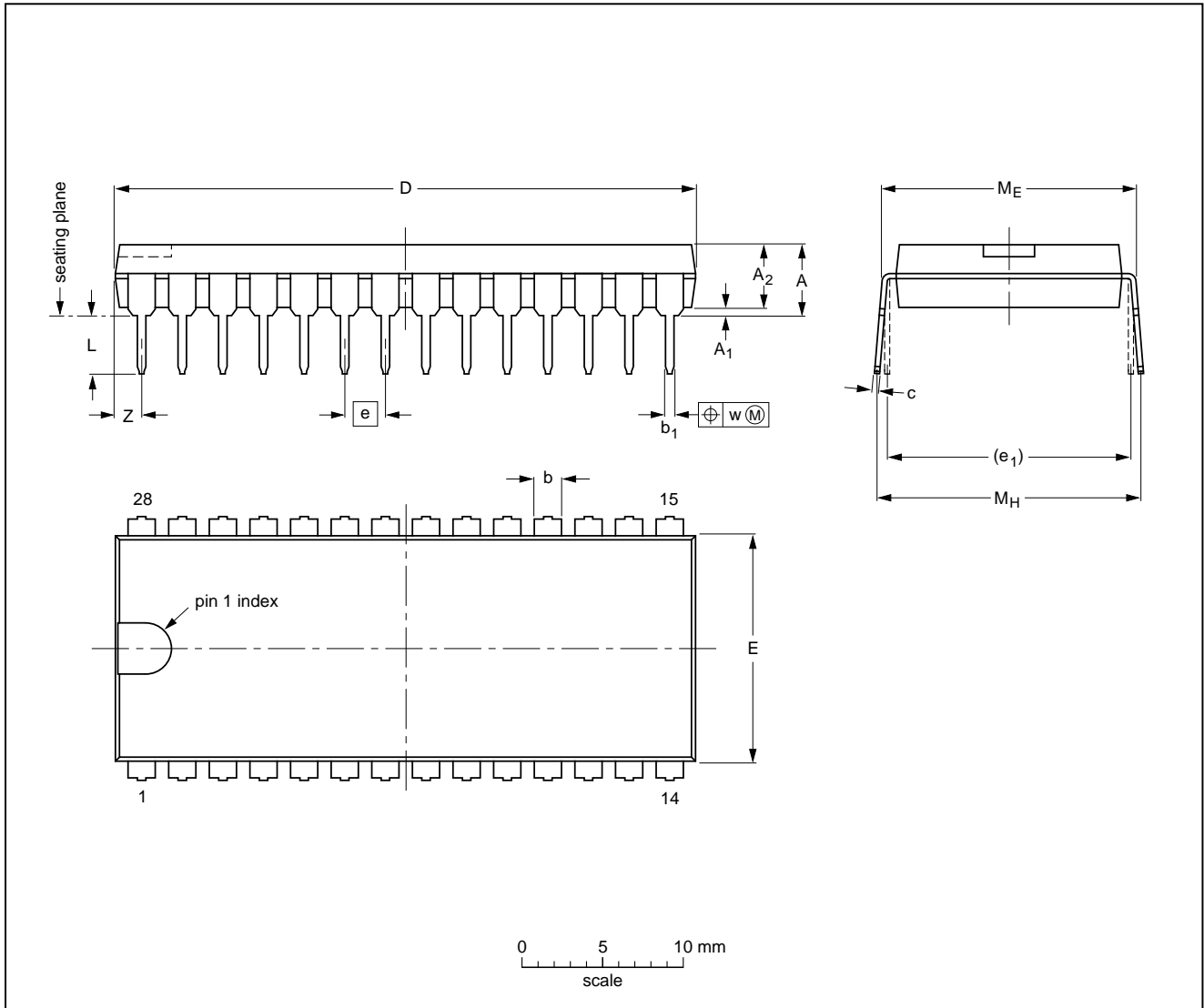
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PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

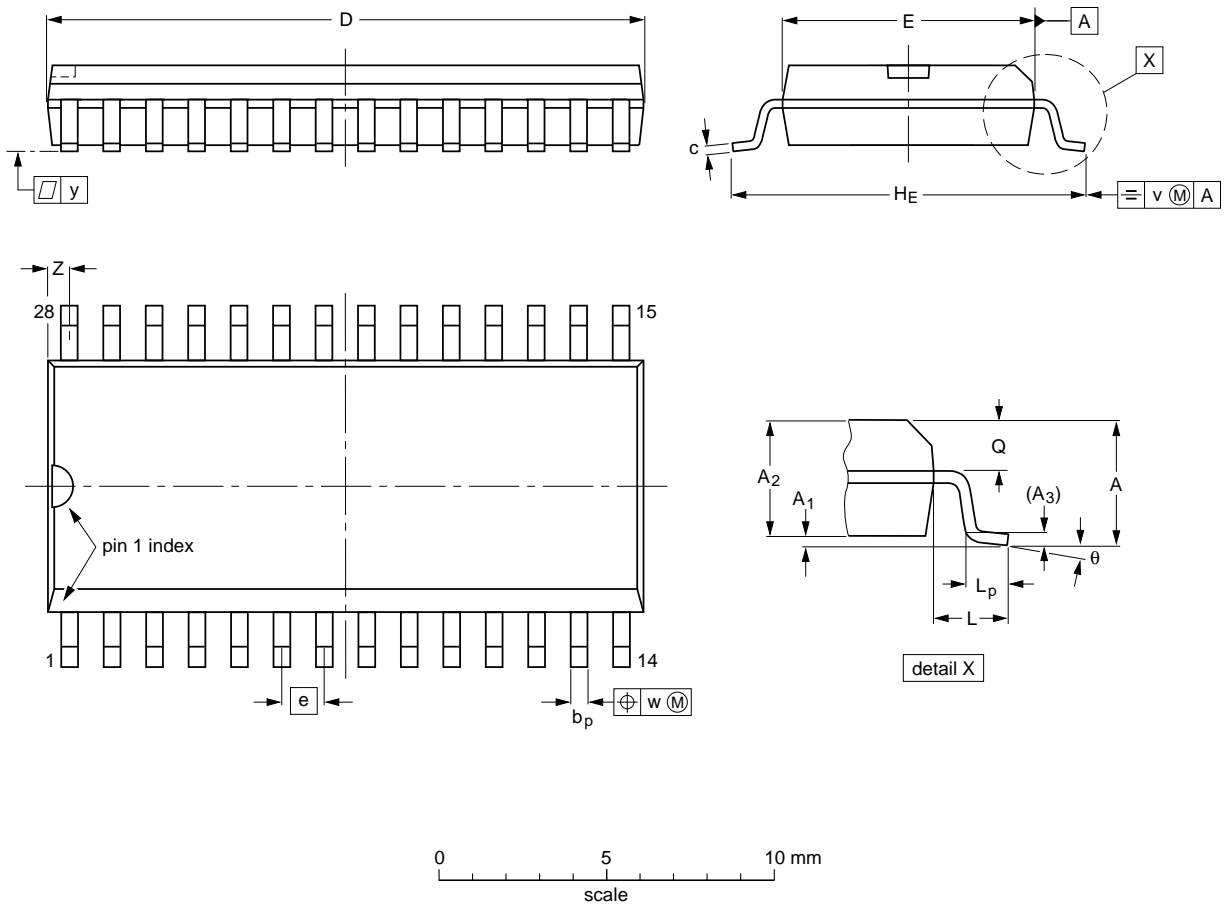
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				92-11-17 95-01-14

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SO28: plastic small outline package; 28 leads; body width 7.5 mm

SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				91-08-13 95-01-24

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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