

# DATA SHEET

## **TDA4866**

**Full bridge current driven vertical  
deflection booster**

Product specification  
Supersedes data of 1996 Oct 10  
File under Integrated Circuits, IC02

1999 Jun 14

# Full bridge current driven vertical deflection booster

## TDA4866

### FEATURES

- Fully integrated, few external components
- No additional components in combination with the deflection controller TDA485x, TDA4841PS
- Pre-amplifier with differential high CMRR current mode inputs
- Low offsets
- High linear sawtooth signal amplification
- High efficient DC-coupled vertical output bridge circuit
- Powerless vertical shift
- High deflection frequency up to 160 Hz
- Power supply and flyback supply voltage independent adjustable to optimize power consumption and flyback time
- Excellent transition behaviour during flyback
- Guard circuit for screen protection.

### GENERAL DESCRIPTION

The TDA4866 is a power amplifier for use in 90 degree colour vertical deflection systems for frame frequencies of 50 to 160 Hz. The circuit provides a high CMRR current driven differential input. Due to the bridge configuration of the two output stages DC-coupling of the deflection coil is achieved. In conjunction with TDA485x, TDA4841PS the ICs offer an extremely advanced system solution.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>DC supply; note 1</b>						
$V_P$	supply voltage (pin 3)		8.2	–	25	V
$V_{FB}$	flyback supply voltage (pin 7)	note 2	–	–	60	V
$I_q$	quiescent current (pin 7)		–	7	10	mA
<b>Vertical circuit</b>						
$I_{defl}$	deflection current (peak-to-peak value; pins 4 and 6)		0.6	–	2	A
$I_{id}$	differential input current (peak-to-peak value)	note 3	–	$\pm 500$	$\pm 600$	$\mu A$
<b>Flyback generator</b>						
$I_{FB}$	maximum current during flyback (peak-to-peak value; pin 7)		–	–	2	A
<b>Guard circuit; note 1</b>						
$V_8$	guard voltage	guard on	7.5	8.5	10	V
$I_8$	guard current	guard on	5	–	–	mA

### Notes

1. Voltages refer to pin 5 (GND).
2. Up to  $60 V \geq V_{FB} \geq 40 V$  a decoupling capacitor  $C_{FB} = 22 \mu F$  (between pin 7 and pin 5) and a resistor  $R_{FB} = 100 \Omega$  (between pin 7 and  $V_{FB}$ ) are required (see Fig.4).
3. Differential input current  $I_{id} = I_1 - I_2$ .

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**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4866	SIL9P	plastic single in-line power package; 9 leads	SOT131-2

**BLOCK DIAGRAM**

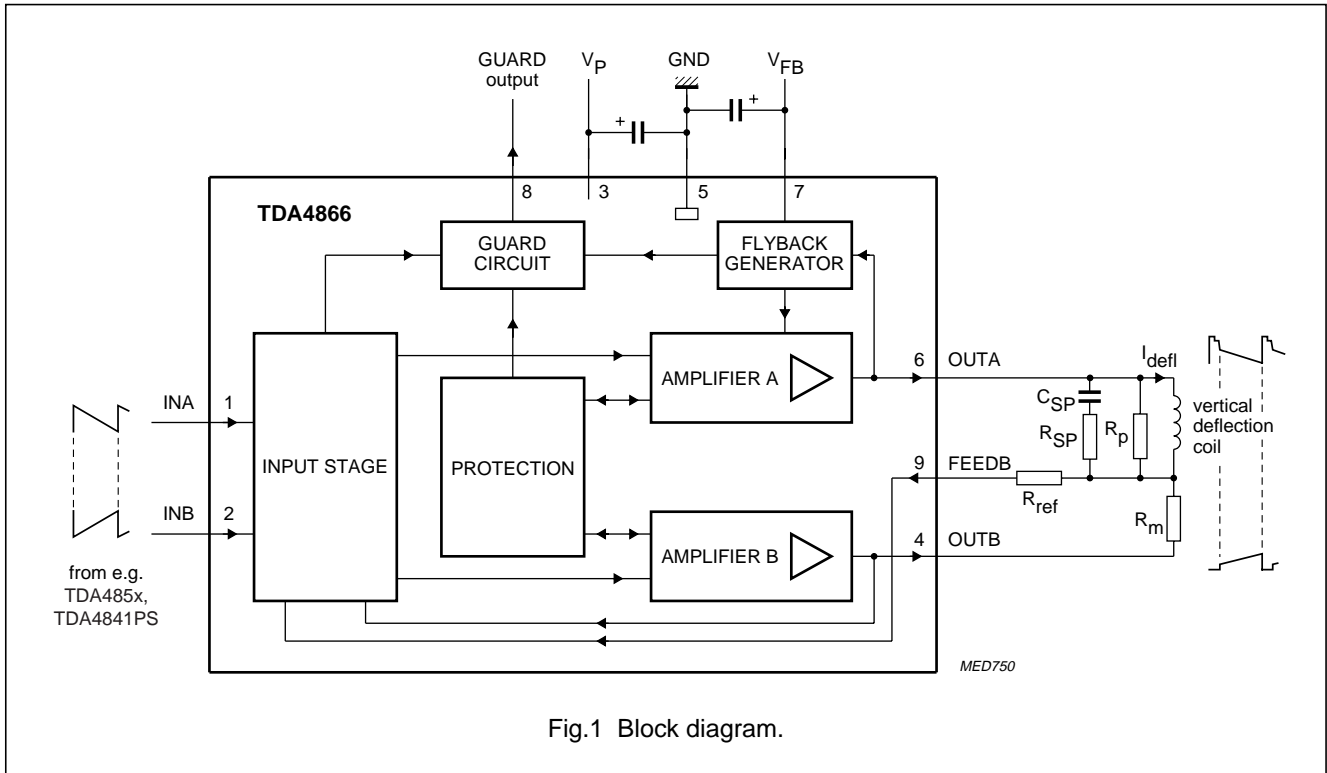


Fig.1 Block diagram.

**PINNING**

SYMBOL	PIN	DESCRIPTION
INA	1	input A
INB	2	input B
V <sub>P</sub>	3	supply voltage
OUTB	4	output B
GND	5	ground
OUTA	6	output A
V <sub>FB</sub>	7	flyback supply voltage
GUARD	8	guard output
FEEDB	9	feedback input

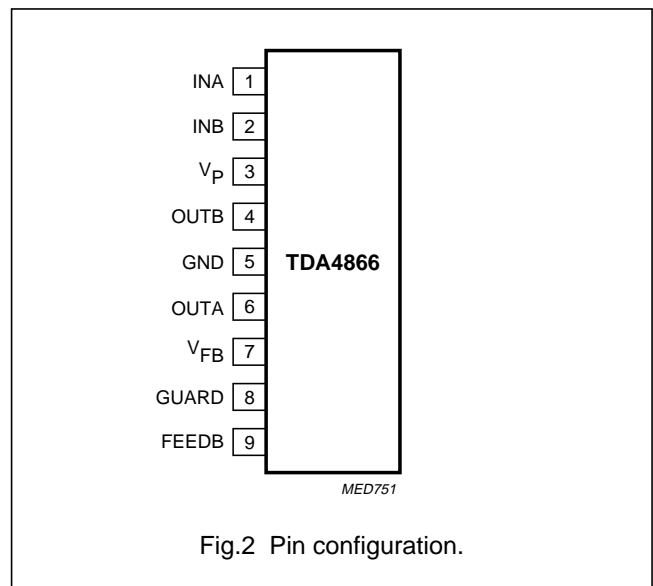


Fig.2 Pin configuration.

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## FUNCTIONAL DESCRIPTION

The TDA4866 consists of a differential input stage, two output stages, a flyback generator, a protection circuit for the output stages and a guard circuit.

### Differential input stage

The differential input stage has a high CMRR differential current mode input (pins 1 and 2) that results in a high electro-magnetic immunity and is especially suitable for driver units with differential (e.g. TDA485x, TDA4841PS) and single ended current signals. Driver units with voltage outputs are simply applicable as well (e.g. two additional resistors are required).

The differential input stage delivers the driver signals for the output stages.

### Output stages

The two output stages are current driven in opposite phase and operate in combination with the deflection coil in a full bridge configuration. Therefore the TDA4866 requires no external coupling capacitor (e.g. 2200  $\mu$ F) and operates with one supply voltage  $V_P$  and a separate adjustable flyback supply voltage  $V_{FB}$  only. The deflection current through the coil ( $I_{defl}$ ) is measured with the resistor  $R_m$  which produces a voltage drop ( $U_{rm}$ ) of:  $U_{rm} \approx R_m \times I_{defl}$ . At the feedback input (pin 9) a part of  $I_{defl}$  is fed back to the input stage. The feedback input has a current input characteristic which holds the differential voltage between pin 9 and the output pin 4 on zero. Therefore the feedback current ( $I_g$ ) through  $R_{ref}$  is:

$$I_g \approx \frac{R_m}{R_{ref}} \times I_{defl}$$

The input stage directly compares the driver currents into pins 1 and 2 with the feedback current  $I_g$ . Any difference of this comparison leads to a more or less driver current for the output stages. The relation between the deflection current and the differential input current ( $I_{id}$ ) is:

$$I_{id} = I_g \approx \frac{R_m}{R_{ref}} \times I_{defl}$$

Due to the feedback loop gain ( $V_{U loop}$ ) and internal bondwire resistance ( $R_{bo}$ ) correction factors are required to determine the accurate value of  $I_{defl}$ :

$$I_{defl} = I_{id} \times \frac{R_{ref}}{R_m + R_{bo}} \times \left(1 - \frac{1}{V_{U loop}}\right)$$

with  $R_{bo} \approx 70 \text{ m}\Omega$  and  $\left(1 - \frac{1}{V_{U loop}}\right) \approx 0.98$

for  $I_{defl} = 0.7 \text{ A}$ .

The deflection current can be adjusted up to  $\pm 1 \text{ A}$  by varying  $R_{ref}$  when  $R_m$  is fixed to  $1 \Omega$ .

High bandwidth and excellent transition behaviour is achieved due to the transimpedance principle this circuit works with.

### Flyback generator

During flyback the flyback generator supplies the output stage A with the flyback voltage. This makes it possible to optimize power consumption (supply voltage  $V_P$ ) and flyback time (flyback voltage  $V_{FB}$ ). Due to the absence of a decoupling capacitor the flyback voltage is fully available.

In parallel with the deflection yoke and the damping resistor ( $R_p$ ) an additional RC combination ( $R_{SP}$ ;  $C_{SP}$ ) is necessary to achieve an optimized flyback behaviour.

### Protection

The output stages are protected against:

- Thermal overshoot
- Short-circuit of the coil (pins 4 and 6).

### Guard circuit

The internal guard circuit provides a blanking signal for the CRT. The guard signal is active HIGH:

- At thermal overshoot
- When feedback loop is out of range
- During flyback.

The internal guard circuit will not be activated, if the input signals on pins 1 and 2 delivered from the driver circuit are out of range or at short-circuit of the coil (pins 4 and 6).

For this reason an external guard circuit can be applied to detect failures of the deflection (see Fig.6). This circuit will be activated when flyback pulses are missing, which is the indication of any abnormal operation.

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages referenced to pin 5 (GND); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_P$	supply voltage (pin 3)		0	30	V
$V_{FB}$	flyback supply voltage (pin 7)		0	60	V
$I_{FB}$	flyback supply current		0	$\pm 1.8$	A
$V_1, V_2$	input voltage		0	$V_P$	V
$I_1, I_2$	input current		0	$\pm 5$	mA
$V_4, V_6$	output voltage		0	$V_P$	V
$I_4, I_6$	output current	note 1	0	$\pm 1.8$	A
$V_9$	feedback voltage		0	$V_P$	V
$I_9$	feedback current		0	$\pm 5$	mA
$V_8$	guard voltage	note 2	0	$V_P + 0.4$	V
$I_8$	guard current		0	$\pm 5$	mA
$T_{stg}$	storage temperature		-20	+150	°C
$T_{amb}$	operating ambient temperature		-20	+75	°C
$T_j$	junction temperature	note 3	-20	+150	°C
$V_{es}$	electrostatic handling for all pins	note 4	-500	+500	V

### Notes

1. Maximum output currents  $I_4$  and  $I_6$  are limited by current protection.
2. For  $V_P > 13$  V the guard voltage  $V_8$  is limited to 13 V.
3. Internally limited by thermal protection; switching point  $\geq 150$  °C.
4. Equivalent to discharging a 200 pF capacitor through a 0  $\Omega$  series resistor.

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	4	K/W

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### CHARACTERISTICS

$V_P = 15\text{ V}$ ;  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ;  $V_{\text{FB}} = 40\text{ V}$ ; voltages referenced to pin 5 (GND); parameters are measured in test circuit (see Fig.3); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	supply voltage (pin 3)		8.2	–	25	V
$V_{\text{FB}}$	flyback supply voltage (pin 7)	note 1	$V_P + 6$	–	60	V
$I_{\text{FB}}$	quiescent feedback current (pin 7)	no load; no signal	–	7	10	mA
<b>Input stage</b>						
$I_{\text{id(p-p)}}$	differential input current ( $I_{\text{id}} = I_1 - I_2$ ) (peak-to-peak value)		–	$\pm 500$	$\pm 600$	$\mu\text{A}$
$I_{1, 2(\text{p-p})}$	single ended input current (peak-to-peak value)	note 2	0	$\pm 300$	$\pm 600$	$\mu\text{A}$
CMRR	common mode rejection ratio	note 3	–	–54	–	dB
$V_1$	input clamp voltage	$I_1 = 300\text{ }\mu\text{A}$	2.7	3.0	3.3	V
$V_2$	input clamp voltage	$I_2 = 300\text{ }\mu\text{A}$	2.7	3.0	3.3	V
$\text{TC}_{i,1}$	input clamp signal TC on pin 1		0	–	$\pm 800$	$\mu\text{V/K}$
$\text{TC}_{i,2}$	input clamp signal TC on pin 2		0	–	$\pm 800$	$\mu\text{V/K}$
$V_1 - V_2$	differential input voltage	$I_{\text{id}} = 0$	0	–	$\pm 10$	mV
$I_9$	feedback current		–	$\pm 500$	$\pm 600$	$\mu\text{A}$
$V_9$	feedback voltage		1	–	$V_P - 1$	V
$I_{\text{id(offset)}}$	differential input offset current ( $I_{\text{id(offset)}} = I_1 - I_2$ )	$I_{\text{defl}} = 0$ ; $R_{\text{ref}} = 1.5\text{ k}\Omega$ ; $R_{\text{m}} = 1\text{ }\Omega$	0	–	$\pm 20$	$\mu\text{A}$
$C_{i\text{ INA}}$	input capacity pin 1 referenced to GND		–	–	5	pF
$C_{i\text{ INB}}$	input capacity pin 2 referenced to GND		–	–	5	pF
<b>Output stages A and B</b>						
$I_4$	output current		–	–	$\pm 1$	A
$I_6$	output current		–	–	$\pm 1$	A
$V_6$	output A saturation voltage to GND	$I_6 = 0.7\text{ A}$	–	1.3	1.5	V
		$I_6 = 1.0\text{ A}$	–	1.6	1.8	V
$V_{6,3}$	output A saturation voltage to $V_P$	$I_6 = 0.7\text{ A}$	–	2.3	2.9	V
		$I_6 = 1.0\text{ A}$	–	2.7	3.3	V
$V_4$	output B saturation voltage to GND	$I_4 = 0.7\text{ A}$	–	1.3	1.5	V
		$I_4 = 1.0\text{ A}$	–	1.6	1.8	V
$V_{4,3}$	output B saturation voltage to $V_P$	$I_4 = 0.7\text{ A}$	–	1.0	1.6	V
		$I_4 = 1.0\text{ A}$	–	1.3	1.9	V
LE	linearity error	$I_{\text{defl}} = \pm 0.7\text{ A}$ ; note 4	–	–	2	%
$V_4$	DC output voltage	$I_{\text{id}} = 0\text{ A}$ ; closed-loop	6.6	7.2	7.8	V
$V_6$	DC output voltage	$I_{\text{id}} = 0\text{ A}$ ; closed-loop	6.6	7.2	7.8	V
$G_{\text{oi}}$	open-loop current gain ( $I_4, 6/I_{\text{id}}$ )	$I_4, 6 < 100\text{ mA}$ ; note 5	–	100	–	dB
$G_{\text{ofb}}$	open-loop current gain ( $I_4, 6/I_9$ )	$I_4, 6 < 100\text{ mA}$ ; note 5	–	100	–	dB
$G_{\text{ifb}}$	current ratio ( $I_{\text{id}}/I_9$ )	closed-loop	–	–0.2	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{\text{def(ripple)}}$	output ripple current as a function of supply ripple	$V_{\text{P(ripple)}} = \pm 0.5 \text{ V}$ ; $I_{\text{id}} = 0$ ; closed-loop	–	$\pm 1$	–	mA
<b>Flyback generator</b>						
$V_{7,6}$	voltage drop during flyback reverse	$I_{\text{def}} = 0.7 \text{ A}$	–	–2.0	–3.0	V
		$I_{\text{def}} = 1.0 \text{ A}$	–	–2.3	–3.5	V
	forward	$I_{\text{def}} = 0.7 \text{ A}$	–	+5.6	+6.1	V
		$I_{\text{def}} = 1.0 \text{ A}$	–	+5.9	+6.5	V
$V_6$	switching on threshold voltage		$V_{\text{P}} - 1$	–	$V_{\text{P}} + 1.5$	V
$V_6$	switching off threshold voltage		$V_{\text{P}} - 1.5$	–	$V_{\text{P}} + 1$	V
$I_7$	flyback current during flyback		–	–	$\pm 1$	A
<b>Guard circuit</b>						
$V_8$	output voltage	guard on	7.5	8.5	10	V
$V_8$	output voltage	guard on; $V_{\text{P}} = 8.2 \text{ V}$	6.9	–	$V_{\text{P}} - 0.4$	V
$I_8$	output current	guard on	5	–	–	mA
$V_8$	output voltage	guard off	–	–	0.4	V
$I_8$	output current	guard off; $V_8 = 5 \text{ V}$	0.5	1	1.5	mA
$V_{8(\text{ext.})}$	allowable external voltage on pin 8		0	–	13	V
		$V_{\text{P}} \leq 13 \text{ V}$	0	–	$V_{\text{P}} + 0.3$	V

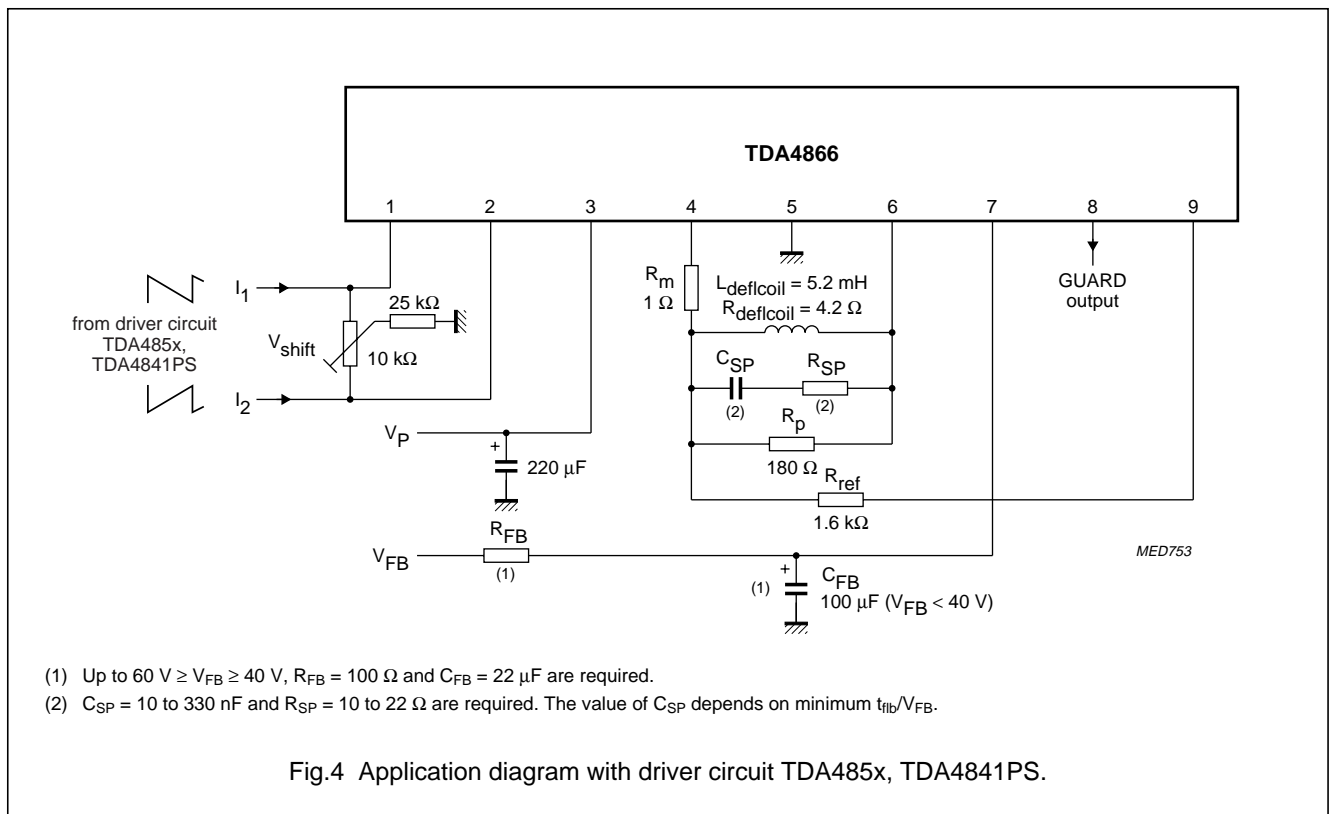
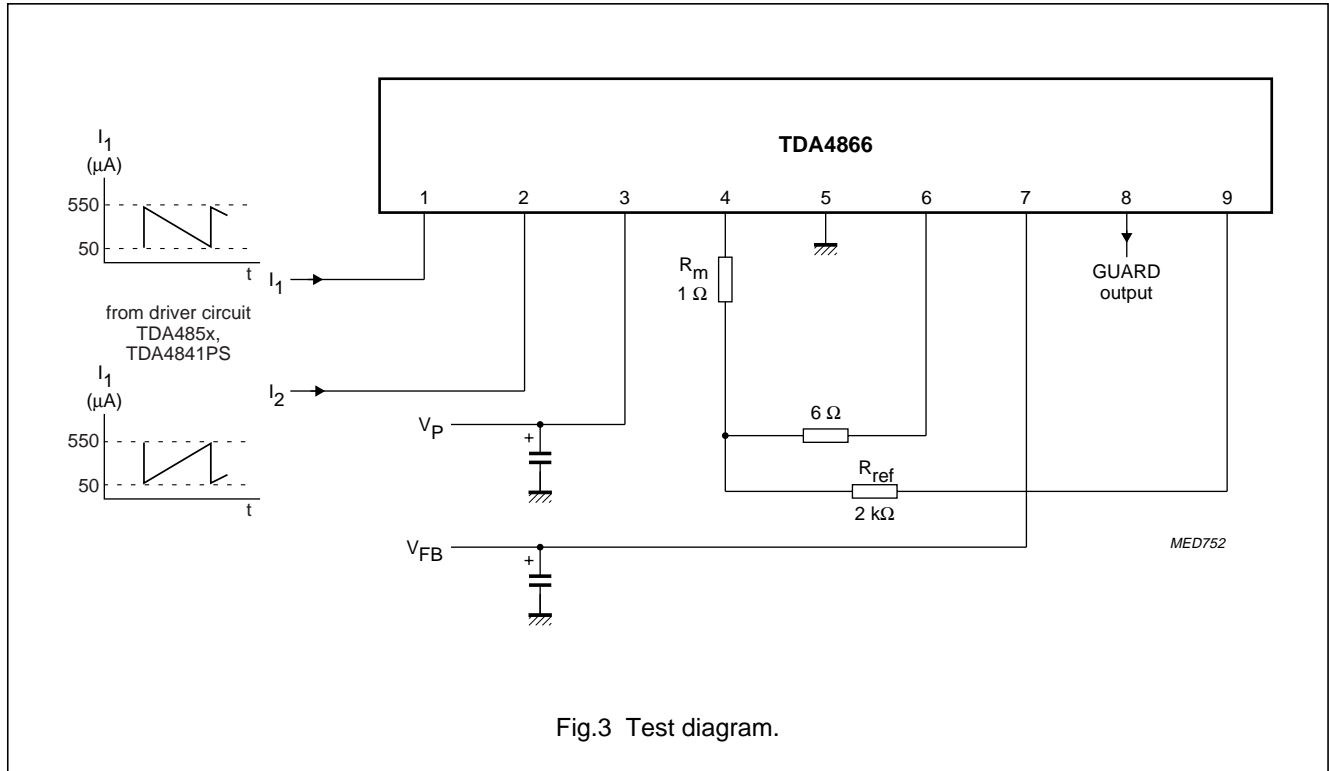
**Notes**

- Up to  $60 \text{ V} \geq V_{\text{FB}} \geq 40 \text{ V}$  a decoupling capacitor  $C_{\text{FB}} = 22 \mu\text{F}$  (between pins 7 and 5) and a resistor  $R_{\text{FB}} = 100 \Omega$  (between pin 7 and  $V_{\text{FB}}$ ) are required (see Fig.4).
- Saturation voltages of output stages A and B can be increased in the event of negative input currents  $I_{1,2} < -500 \mu\text{A}$ .
- $D_i = \frac{I_{\text{deflc}}}{I_{\text{idc}}} \times \frac{I_{\text{id}}}{I_{\text{def}}}$  with  $I_{\text{deflc}}$  = common mode deflection current and  $I_{\text{idc}}$  = common mode input current.
- Deviation of the output slope at a constant input slope.
- Frequency behaviour of  $G_{\text{oi}}$  and  $G_{\text{ofb}}$ :
  - 3 dB open-loop bandwidth ( $-45^\circ$ ) at 15 kHz; second pole ( $-135^\circ$ ) at 1.3 MHz.
  - Open-loop gain at second pole ( $-135^\circ$ ) 55 dB.

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## TEST AND APPLICATION INFORMATION





# Full bridge current driven vertical deflection booster

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**Example**

SYMBOL	VALUE	UNIT
<b>Values given from application</b>		
$I_{defl(max)}$	0.71	A
$L_{deflcoil}$	5.2	mH
$R_{deflcoil}$	5.4 [= 4.2 + 7% + $\Delta R(\vartheta)$ ]	$\Omega$
$R_m$	1 (+1%)	$\Omega$
$R_p$	180	$\Omega$
$R_{ref}$	1.6	k $\Omega$
$V_{FB}$	35	V
$T_{amb}$	+50	$^{\circ}C$
$T_{deflcoil}$	+75	$^{\circ}C$
$R_{th(j-mb)}$	4	K/W
$R_{th(mb-amb)}^{(1)}$	8	K/W
<b>Calculated values</b>		
$V_P$	8.6	V
$t_{flb}$	270	$\mu s$
$P_{tot}$	3.65	W
$P_{defl}$	0.9	W
$P_{IC}$	2.75	W
$R_{th(tot)}$	12	K/W
$T_{j(max)}^{(2)}$	+83	$^{\circ}C$

**Notes**

1. A layer of silicon grease between the mounting base and the heatsink optimizes thermal resistance.
2.  $T_{j(max)} = P_{IC} \times [R_{th(j-mb)} + R_{th(mb-amb)}] + T_{amb}$

Calculation formula for supply voltage and power consumption

$$V_{b1} = V_{6,3} + R_{deflcoil} \times I_{defl(max)} - U'_L + R_m \times I_{defl(max)} + V_4$$

$$V_{b2} = V_6 + R_{deflcoil} \times I_{defl(max)} + U'_L + R_m \times I_{defl(max)} + V_{4,3}$$

for  $V_{b1} > V_{b2}$  :  $V_P = V_{b1}$

for  $V_{b2} > V_{b1}$  :  $V_P = V_{b2}$

with:

$$U'_L = L_{deflcoil} \times 2I_{defl(max)} \times f_v$$

$f_v$  = vertical deflection frequency.

$$P_{tot} = V_P \times \frac{I_{defl(max)}}{2} + V_P \times 0.03 \text{ A} + 0.1 \text{ W} + V_{FB} \times I_{FB}$$

$$P_{defl} = \frac{1}{3} (R_{deflcoil} + R_m) \times I_{defl(max)}^2$$

$$P_{IC} = P_{tot} - P_{defl}$$

$P_{IC}$  = power dissipation of the IC

$P_{defl}$  = power dissipation of the deflection coil

$P_{tot}$  = total power dissipation.

Calculation formula for flyback time ( $t_{flb}$ )

$$t_{flb} = \frac{L_{deflcoil}}{R_{deflcoil} + R_m} \times \ln \left( \frac{1 + \frac{(R_{deflcoil} + R_m) \times I_{defl(max)}}{V_{FB} + V_{7r} - V_{6r}}}{1 - \frac{(R_{deflcoil} + R_m) \times I_{defl(max)}}{V_{FB} - (V_{7f} - V_{6f})}} \right) + t_{flb(off)}$$

with:

$t_{flb(off)}$  = flyback switch off time = 50  $\mu s$  for this application ( $t_{flb(off)}$  depends on  $V_{FB}$ ,  $I_{defl(max)}$ ,  $L_{deflcoil}$  and  $C_{SP}$ ).

To achieve good noise suppression the following values for  $R_p$  are recommended:

**Recommended values**

$L_{deflcoil}$ (mH)	$R_p$ ( $\Omega$ )
3	100
6	180
10	240
15	390

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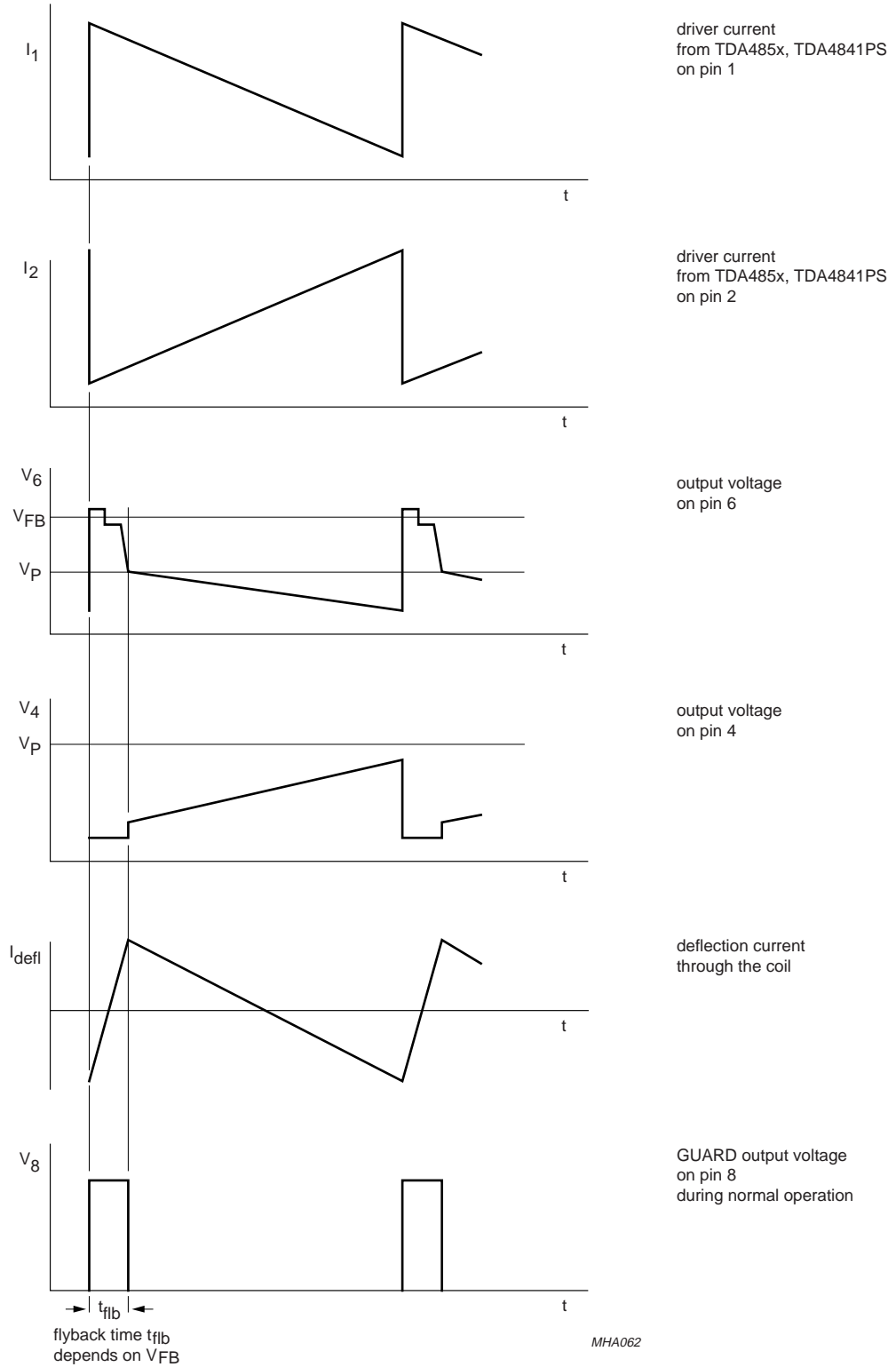


Fig.5 Timing diagram.

# Full bridge current driven vertical deflection booster

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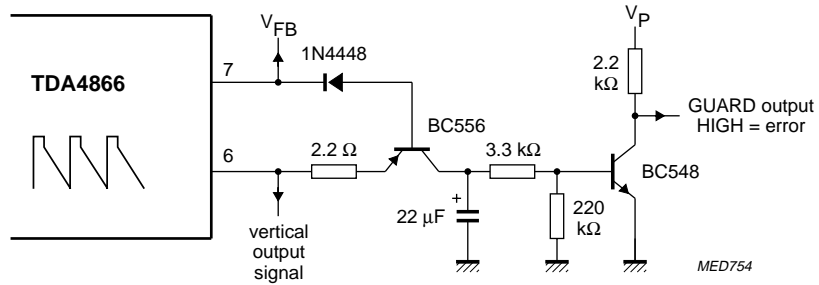


Fig.6 Application circuit for external guard signal generation.

## INTERNAL PIN CONFIGURATION

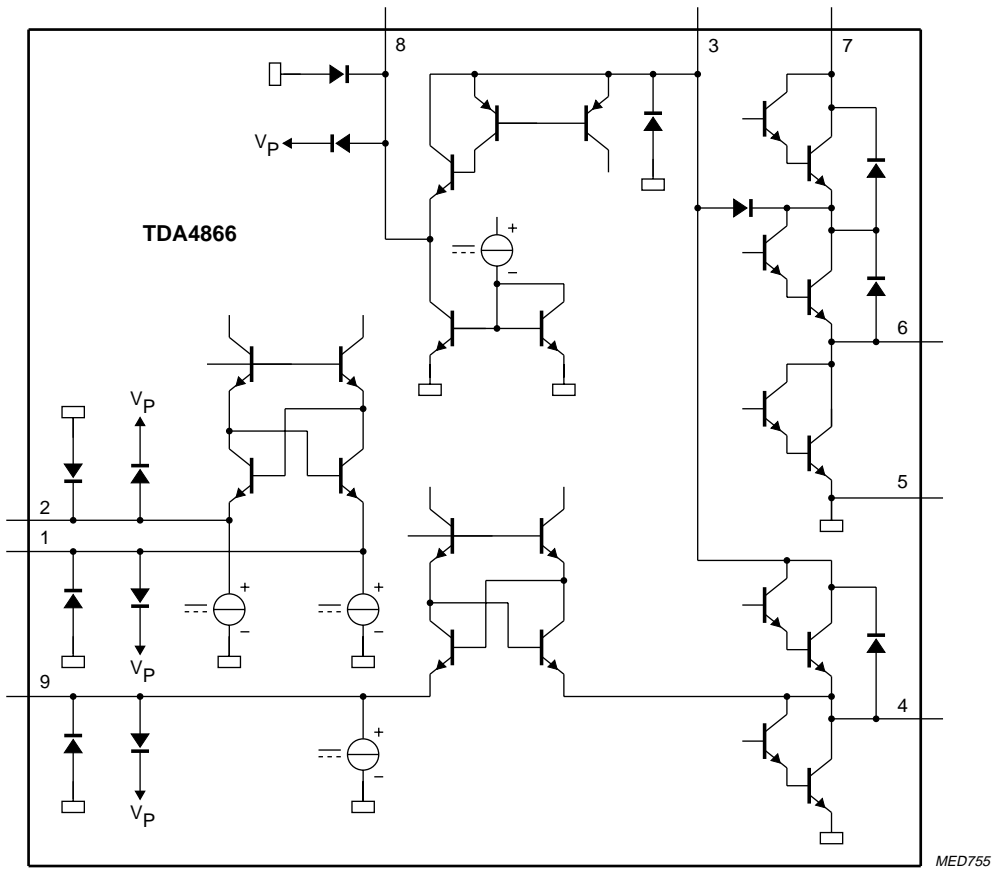


Fig.7 Internal circuits.

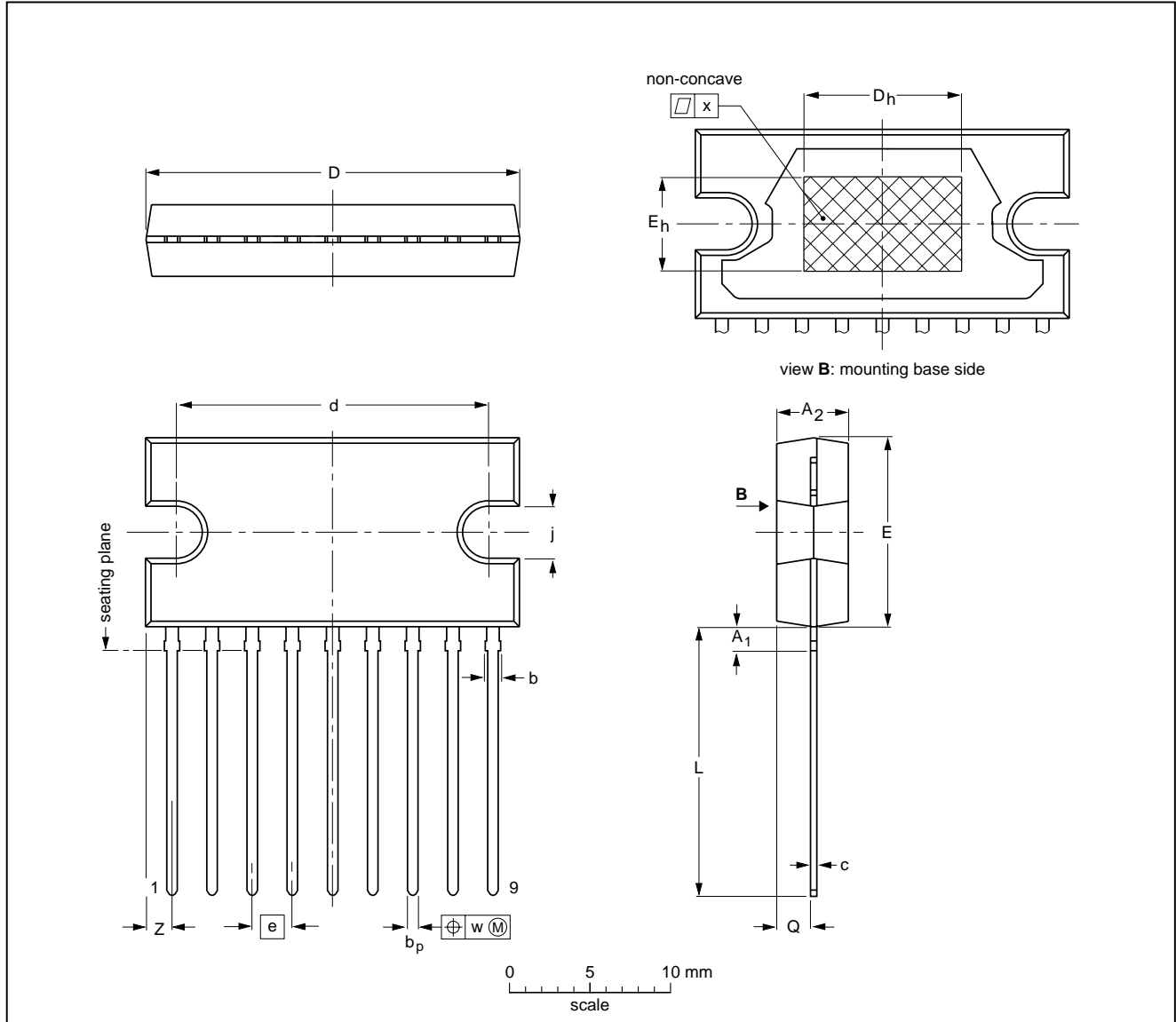
# Full bridge current driven vertical deflection booster

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**PACKAGE OUTLINE**

**SIL9P: plastic single in-line power package; 9 leads**

**SOT131-2**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sub>1</sub> max.	A <sub>2</sub>	b max.	b <sub>p</sub>	c	D <sup>(1)</sup>	d	D <sub>h</sub>	E <sup>(1)</sup>	e	E <sub>h</sub>	j	L	Q	w	x	Z <sup>(1)</sup>
mm	2.0	4.6 4.2	1.1	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	6	3.4 3.1	17.2 16.5	2.1 1.8	0.25	0.03	2.00 1.45

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT131-2						92-11-17 95-03-11

## Full bridge current driven vertical deflection booster

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### SOLDERING

#### Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

#### Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg(max)}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable <sup>(1)</sup>

#### Note

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

### DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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**NOTES**

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 02 67 52 2531, Fax. +39 02 67 52 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 319762,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,  
Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,  
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 62 5344, Fax. +381 11 63 5777

**For all other countries apply to:** Philips Semiconductors,  
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,  
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

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