

# DATA SHEET

## **TDA4651**

Multistandard colour decoder with  
negative colour difference output  
signals

Preliminary specification  
File under Integrated Circuits, IC02

August 1993

# Multistandard colour decoder with negative colour difference output signals

## TDA4651

### FEATURES

Identifies and demodulates PAL, SECAM, NTSC 3.58 and NTSC 4.43 chrominance signals with:

- Gain controlled chrominance amplifier
- ACC demodulation controlled by system scanning
- Internal colour difference signal output filters to remove the residual subcarrier
- PAL / NTSC demodulation
  - H (burst) and V blanking
  - PAL switch (disabled for NTSC)
  - NTSC phase shift (disabled for PAL)
  - PLL-controlled reference oscillator
  - two reference oscillator crystals on separate pins with automatic switching
  - quadrature demodulator with subcarrier reference
- SECAM demodulation
  - limiter amplifier
  - quadrature demodulator with a single external reference tuned circuit
  - alternate line blanking, H and V blanking
  - de-emphasis
- Identification
  - automatic standard identification by sequential inquiry
  - secure SECAM identification at 50 Hz only, with PAL priority
  - four switched outputs for chrominance filter selection and display control
  - external service switch for oscillator adjustment

### GENERAL DESCRIPTION

The TDA4651 is a monolithic integrated multistandard colour decoder for PAL, SECAM and NTSC (3.58 and 4.43 MHz) with negative colour difference output signals. The colour difference output signals are fed to the TDA4661, switched capacitor delay line.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	positive supply voltage (pin 13)		10.8	12	13.2	V
$I_P$	supply current (pin 13)		–	60	–	mA
$V_{i(p-p)}$	chrominance input voltage (pin 15) (peak-to-peak value)	see note 1	20	200	400	mV
<b>Colour difference output signals</b> (see note 2)						
$V_{1(p-p)}$	–(R–Y) output (peak-to-peak value)	PAL	442	525	624	mV
		NTSC	370	440	523	mV
		SECAM	883	1050	1248	mV
$V_{3(p-p)}$	–(B–Y) output (peak-to-peak value)	PAL	559	665	791	mV
		NTSC	468	557	662	mV
		SECAM	1119	1330	1581	mV

### Notes to quick reference data

1. Within 3 dB output voltage deviation.
2. Burst key width for PAL 4.3  $\mu$ s, for NTSC 3.6  $\mu$ s  
Burst width for PAL and NTSC 2.25  $\mu$ s, ratio burst-chrominance-amplitude 1/2.2.

### ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4651	28	DIL	plastic	SOT117 <sup>(1)</sup>
TDA4651WP	28	PLCC	plastic	SOT261CG <sup>(2)</sup>

### Note

1. SOT117-1; 1996 November 25.
2. SOT261-2; 1996 November 25.

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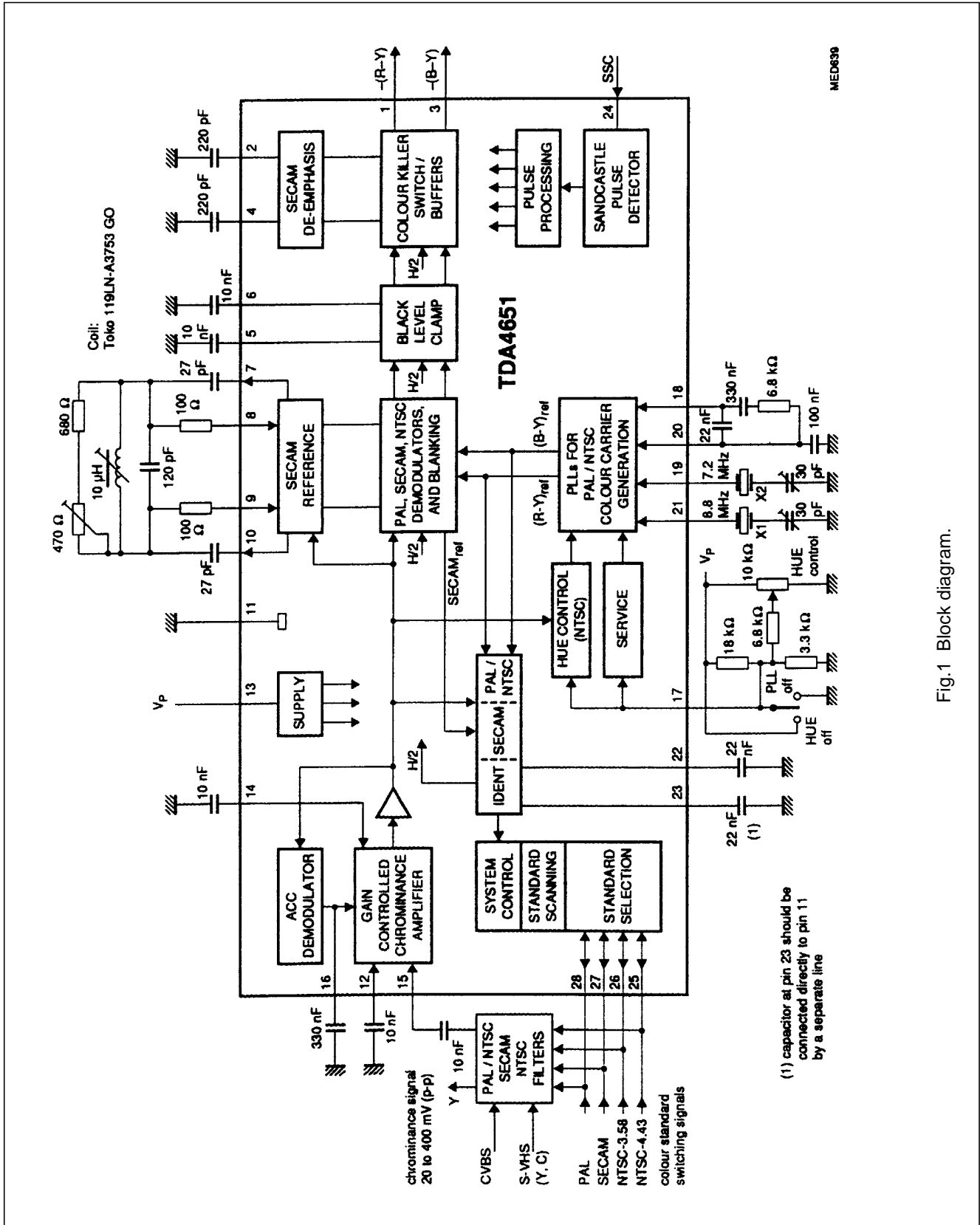


Fig.1 Block diagram.

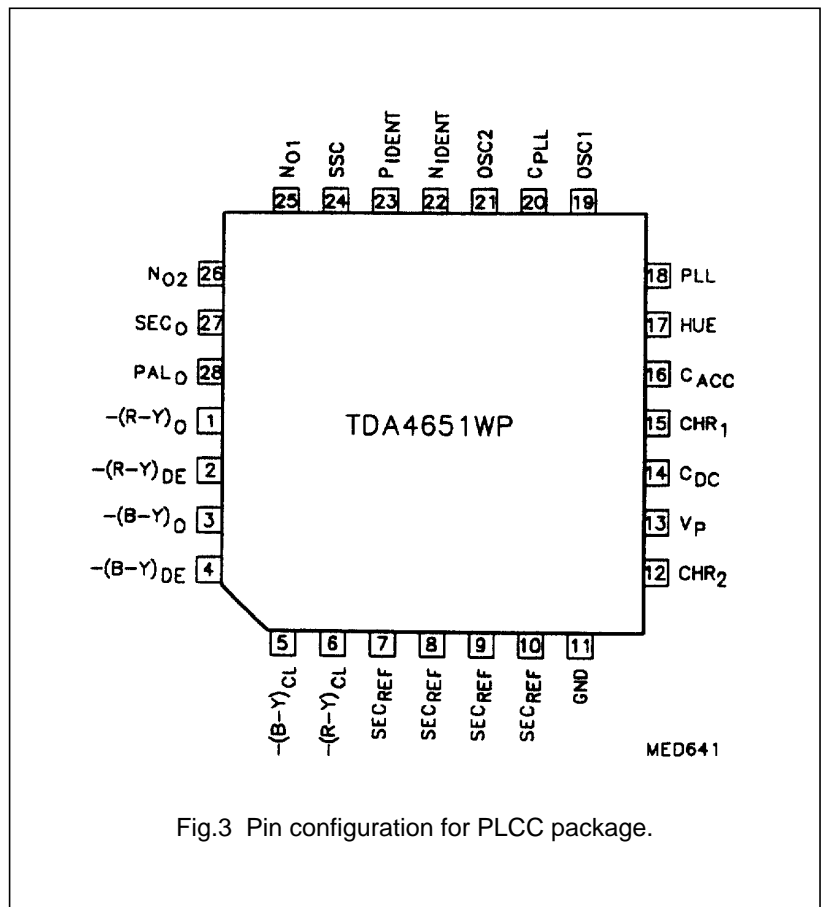
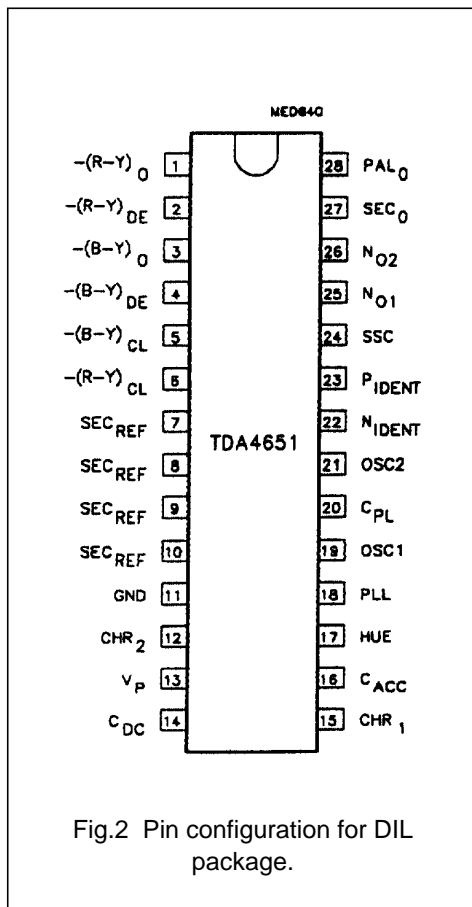
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## PINNING

SYMBOL	PIN	DESCRIPTION
$-(R-Y)_o$	1	$-(R-Y)$ output
$-(R-Y)_{DE}$	2	$(R-Y)$ de-emphasis
$-(B-Y)_o$	3	$-(B-Y)$ output
$-(B-Y)_{DE}$	4	$(B-Y)$ de-emphasis
$-(B-Y)_{CL}$	5	$(B-Y)$ clamping
$-(R-Y)_{CL}$	6	$(R-Y)$ clamping
SEC <sub>REF</sub>	7	SECAM reference tuned circuit
	8	
	9	
	10	
GND	11	ground
CHR <sub>2</sub>	12	DC for ACC
V <sub>P</sub>	13	supply voltage
C <sub>DC</sub>	14	DC feedback

CHR <sub>1</sub>	15	chrominance input
C <sub>ACC</sub>	16	automatic colour control
HUE	17	hue control
PLL	18	PLL time constant
OSC1	19	input for 7.15 MHz oscillator
C <sub>PLL</sub>	20	PLL DC reference
OSC2	21	input for 8.86 MHz oscillator
N <sub>IDENT</sub>	22	NTSC identification
P <sub>IDENT</sub>	23	PAL/SECAM identification
SSC	24	super sandcastle pulse input
N <sub>O1</sub>	25	NTSC (4.43 MHz) identification
N <sub>O2</sub>	26	NTSC (3.58 MHz) identification
SEC <sub>0</sub>	27	SECAM identification
PAL <sub>0</sub>	28	PAL identification



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### FUNCTIONAL DESCRIPTION

The IC (see block diagram Fig.1) contains all functions required for the identification and demodulation of PAL, SECAM, NTSC 4.43 MHz and NTSC 3.58 MHz signals. When an unknown signal is fed into the input, the circuit has to identify the standard of the signal; to achieve this it has to switch on successively the appropriate input filter, crystal (8.8 or 7.2 MHz) and demodulator and finally, after having identified the signal, it has to switch on the colour and, in the event of NTSC reception, the hue control. The two colour difference signals  $-(R-Y)$  and  $-(B-Y)$  are available at the outputs. The identification circuit is able to discriminate between NTSC signals with colour carrier frequencies of 3.58 MHz or 4.43 MHz.

### Chrominance amplifier

The chrominance amplifier has an asymmetrical input. The input signal has to be AC coupled (pin 15). The differential amplifier stage at the input is followed by the gain control stage and a differential amplifier with lateral PNP transistors having the function of a level shifter. The gain control stage consists of two ACC-rectifier circuits. One rectifier circuit is switched on during SECAM reception respectively during the SECAM part of the system-control-scanning (it is switched on during part of the burst gate pulse and it is disabled during the prolonged frame flyback); the other rectifier is switched on during the burst, when PAL or NTSC signals are received respectively during the PAL and NTSC parts of the system control scanning. The DC-potential of the symmetrical signal connections to the demodulators is kept at the same level by means of a working point control stage.

### Reference oscillator

The reference oscillator for PAL and NTSC operates at twice the colour carrier frequency. It is followed by a divider stage, providing the  $(R-Y)$  and  $(B-Y)$  reference signal with the correct phase relation to the PAL/NTSC demodulator and the identification part.

### Demodulators

The demodulation of the colour signal requires three demodulators. Two are common for PAL and NTSC and one for the SECAM signals. In the event of NTSC reception, the symmetrical signal is fed into two differential amplifier stages with the correct gain and from there the signal is fed into two demodulators each consisting of four transistors. During NTSC reception the PAL switch between the differential amplifier of the  $(R-Y)$  channel and the corresponding demodulator is disabled. These transistors are switched on and off by the appropriate reference signals. In the event of PAL reception, the symmetrical signal is fed into the same differential amplifiers and the PAL switch is active.

The SECAM demodulator is a combined demodulator for  $-(B-Y)$  and  $-(R-Y)$  with artificial black level being inserted alternately every second line and during line and field flyback. The load resistors of the demodulator are connected to two differential amplifiers, one for  $-(B-Y)$  and one for  $-(R-Y)$ . The unwanted signals occurring every second line ( $(R-Y)$  in the  $-(B-Y)$  channel and  $(B-Y)$  in the  $-(R-Y)$  channel) are blanked.

### Clamp

Behind the demodulators the signals are being filtered and the black level is clamped to a constant DC-level during the burst gate pulse. For the SECAM signals this happens every second line, when the appropriate artificial black level is present.

### De-emphasis and output-buffer

Behind the clamping stages is the de-emphasis for the SECAM signals and just in front of the output stages are the colour killer and blanking stages. The blanking level is the same as the clamping level and the black level.

### Identification

The identification part contains three demodulators.

The first is demodulating during PAL and NTSC identification or reception. It is active during the burst clamping only. The reference signal has the  $(R-Y)$ -phase. The second demodulator is demodulating during the SECAM identification or reception and is active during part of the burst clamping time. It uses the same signals as the SECAM demodulator that is not active during field flyback. These two demodulators are followed by a H/2 switch 'rectifying' the demodulated signal. The result is an identification signal ( $P_{IDENT}$ ) that is positive for a PAL signal during the PAL part of the scanning, for a SECAM signal during the SECAM part of the scanning and for a PAL signal during the NTSC 4.43 part of the scanning. If the  $P_{IDENT}$  is positive during the SECAM part of the scanning, the scanner switches back to the PAL part of the scanning in order to prevent that a PAL signal is erroneously identified as a SECAM signal (PAL priority).

If then the  $P_{IDENT}$  is not positive, the scanner returns to SECAM part and remains there until the  $P_{IDENT}$  is

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positive again. In the event of a field frequency of 60 Hz the signal cannot be identified as a SECAM signal, even if the  $P_{IDENT}$  is positive. If the H/2 signal is of the wrong polarity, the identification signal is negative and the H/2 flip-flop is set to the correct phase.

The third demodulator is demodulating during NTSC identification or reception only. It is active during the burst clamping time. The resulting identification signal ( $N_{IDENT}$ ) is positive for PAL and NTSC 4.43 MHz signal during the NTSC 4.43 part of the scanning and for NTSC 3.58 MHz signal during the

NTSC 3.58 part of the scanning. The reference signal has the (B-Y) phase. The two identification signals allow an unequivocal identification of the received signal. If a signal has been identified, the scanning is stopped and after a delay time the colour is switched on.

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_P$	supply voltage (pin 13)	–	13.2	V
$V_I$	input voltage range at pins 1, 3, 17 and 24 to 28	0	$V_P$	V
$I_O$	output current (pins 1 and 3)	–	–5	mA
$I_{I/O}$	input/output current (pin 25 to 28)	–	–5	$\mu$ A
$T_{amb}$	operating ambient temperature range	0	+70	$^{\circ}$ C
$T_{stg}$	storage temperature range	–25	+150	$^{\circ}$ C
$P_{tot}$	total power dissipation			
	SOT117	–	1.4	W
	SOT261CG	–	1.1	W

### THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	
	SOT117	37 K/W
	SOT261CG	70 K/W

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## CHARACTERISTICS

All voltages are measured to GND (pin 11);  $V_P = 12$  V; chrominance input signal  $V_{15(p-p)} = 200$  mV (with 75% colour bar signal);  $T_{amb} = +25$  °C; measured in test circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_P$	positive supply voltage		10.8	12	13.2	V
$I_P$	supply current		50	60	80	mA
<b>Chrominance part</b>						
$V_{i(p-p)}$	input signal range (pin 15) (peak-to-peak value)	see note 1	20	200	400	mV
$R_I$	input resistance (pin 15)		8.5	10	11.5	k $\Omega$
$C_I$	input capacitance (pin 15)		–	4	5	pF
<b>Demodulator part (PAL/NTSC)</b>						
$V_{1(p-p)}$	colour difference $-(R-Y)$ output signal (peak-to-peak value)	see note 2				
		PAL	442	525	624	mV
		NTSC	370	440	523	mV
$V_{3(p-p)}$	colour difference $-(B-Y)$ output signal (peak-to-peak value)	see note 2				
		PAL	559	665	791	mV
		NTSC	468	557	662	mV
$V_1/V_3$	spread of ratio of colour difference signals $(R-Y)/(B-Y)$	at nominal phase of hue control	–	–	$\pm 5$	%
$V_1/V_1$	spread of signal ratio PAL/NTSC	at nominal phase of hue control	–	–	$\pm 1$	dB
m	signal linearity	$V_{1(p-p)} = 0.8$ V $-(R-Y)$	0.8	–	–	
		$V_{3(p-p)} = 1.0$ V $-(B-Y)$	0.8	–	–	
$V_{1,3}$	DC output level	proportional to $V_P$	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars	–	–	10	mV
$V_{1,3(p-p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	10	mV
		8.87 MHz	–	–	30	mV
$Z_{1,3}$	output impedance		–	–	200	$\Omega$
<b>Demodulator part (SECAM) (see note 3)</b>						
$V_{1(p-p)}$	colour difference $-(R-Y)$ output signal (peak-to-peak value)	every second line blanked	0.88	1.05	1.25	V
$V_{3(p-p)}$	colour difference $-(B-Y)$ output signal (peak-to-peak value)	every second line blanked	1.12	1.33	1.58	V
$V_{1,3}$	DC output level	proportional to $V_P$	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars; every second line blanked	–	–	10	mV
$V_{1,3(p-p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	30	mV
		8.87 MHz	–	–	30	mV
$\Delta V_{1,3}/\Delta V_P$	shift of demodulated $f_o$ levels relative to blanking level	with supply voltage	–	–	3	mV/V
$\Delta V_1/\Delta T$		with temperature	–	0.16	–	mV/K
$\Delta V_3/\Delta T$			–	–0.25	–	mV/K

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Hue control part</b>						
$\phi$	phase shift of reference carrier relative to phase at $V_{17} = 3\text{ V}$	$V_{17} = 2\text{ V}$	-30	-40	-	deg
	phase shift of reference carrier	$V_{17} = 3\text{ V}$	-	0	$\pm 5$	deg
	phase shift of reference carrier relative to phase at $V_{17} = 3\text{ V}$	$V_{17} = 4\text{ V}$	30	40	-	deg
$V_{17}$	internal bias voltage	see note 4	-	3	-	V
	switching voltage for oscillator adjustment	burst OFF; colour ON	0	-	0.5	V
	switching voltage for forced colour ON	hue OFF; colour ON	5.5	-	$V_P$	V
$R_{17}$	input resistance		4.25	5.0	5.75	k $\Omega$
<b>Reference oscillator (PLL) (see note 5)</b>						
$R_{19,21}$	input resistance		-	350	-	$\Omega$
$C_{19,21}$	input capacitance		-	-	10	pF
$f_c$	catching range	at 4.43 MHz	$\pm 400$	-	-	Hz
		at 3.57 MHz	$\pm 330$	-	-	Hz
<b>Identification part (see note 6)</b>						
$V_{25\text{ to }28}$	switching voltages	control voltage OFF state	-	0.05	0.5	V
		control voltage ON state; during scanning	2.35	2.45	2.55	V
		control voltage ON state; internal forced	5.6	5.8	6.0	V
		control voltage ON state; external forced	9.0	-	$V_P$	V
$I_{25\text{ to }28}$	output currents		-	-	-3	mA
$t_d$	delay time for system hold		2	-	3	cycles
	delay time for colour ON		2	-	3	cycles
	delay time for colour OFF		0	-	1	cycles
$t_s$	scanning time for each standard	see note 7	-	4	-	cycles
<b>Super sandcastle pulse detector (see note 8)</b>						
$V_{24}$	input pulse amplitude		7.7	-	$V_P$	V
	input voltage pulse levels to separate V and H blanking pulses	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	voltage pulse amplitude		2.0	2.5	3.0	V
	input voltage pulse levels to separate H blanking pulse	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	voltage pulse amplitude		4.1	4.5	4.9	V
	input voltage pulse levels to separate burst gating pulse	pulse ON	6.2	6.6	7.0	V
pulse OFF		6.0	6.4	6.8	V	
	input voltage	during line scan	-	-	1.0	V
$I_{24}$	input current	during line scan	-	-	-100	$\mu\text{A}$



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## Notes to the characteristics

1. With 20 mV, 3 dB decrease of the output signal is allowed. The level shift at demodulated  $f_0$  relative to blanking level is less than 5 mV.
2. Burst key width for PAL 4.3  $\mu$ s, for NTSC 3.6  $\mu$ s  
Burst width for PAL and NTSC 2.25  $\mu$ s, ratio burst chrominance amplitude 1/2.2.
3. For the SEC+AM standard, amplitude and H/2 ripple content of the CD signals (R-Y) and (B-Y) depend on the characteristics of the external tuned circuit at pins 7 to 10. The resonant frequency of the external tuned circuit must be adjusted such that the demodulated  $f_0$  voltage level is zero in the -(B-Y) output channel at pin 3.  
Now it is possible to adjust the quality of the external circuit such that the demodulated  $f_0$  voltage level is zero in the -(R-Y) output channel at pin 1. If necessary, the  $f_0$  voltage level in the -(B-Y) output channel must be readjusted to zero by the coil of the tuned circuit.  
The external capacitors at pins 2 and 4 (each 220 pF) are matched to the internal resistances of the de-emphasis network such that every alternate scanned line is blanked.
4. Pin 17 open-circuit; proportional to supply voltage.
5. The  $f_0$  frequencies of the 8.8 MHz crystal at pin 21, and the 7.2 MHz crystal at pin 19, can be adjusted when the voltage at pin 17 is less than 0.5 V (burst OFF), thus providing double subcarrier frequencies of the chrominance signal.
6. Switching voltages for chrominance filters and crystals:  
at pin 28 for PAL  
at pin 27 for SECAM  
at pin 26 for NTSC (3.58 MHz)  
at pin 25 for NTSC (4.43 MHz).
7. The inquiry sequence for the standard is: PAL - SECAM - NTSC (3.58 MHz) - NTSC (4.43 MHz). PAL has priority with respect to SECAM, etc.
8. The super sandcastle pulse is compared with three internal threshold levels which are proportional to  $V_P$ .

**Table 1** Specification of quartz crystals in HC-49/U13 holder; standard application.

SYMBOL	PARAMETER	VALUE		UNIT
		43221430405	43221430418	
$f_n$	nominal frequency	8.867238	7.159090	MHz
$C_L$	load capacitance	20		pF
$\Delta f_n$	adjustment tolerance of $f_n$ at +25 °C	±40		ppm
$R_{dld\ max}$	in the drive level range between $10^{-12}$ W and $1.0 \times 10^{-3}$ W, the resonance resistance may not exceed (at +25 °C) the value of $R_{dld\ max}$	100	50	$\Omega$
$R_n$	resonance resistance of unwanted response	$2R_r (+25\ ^\circ\text{C})$		$\Omega$
$C_1$	motional capacitance ( $\pm 20\%$ )	22	19.5	fF
$C_0$	parallel capacitance ( $\pm 20\%$ )	5.5	4.4	pF
T	operating temperature range	-10 to +60		°C
$\Delta f_n$	frequency tolerance over temperature range	±25		ppm
$R_r$	maximum resonance resistance over temperature range	60		$\Omega$

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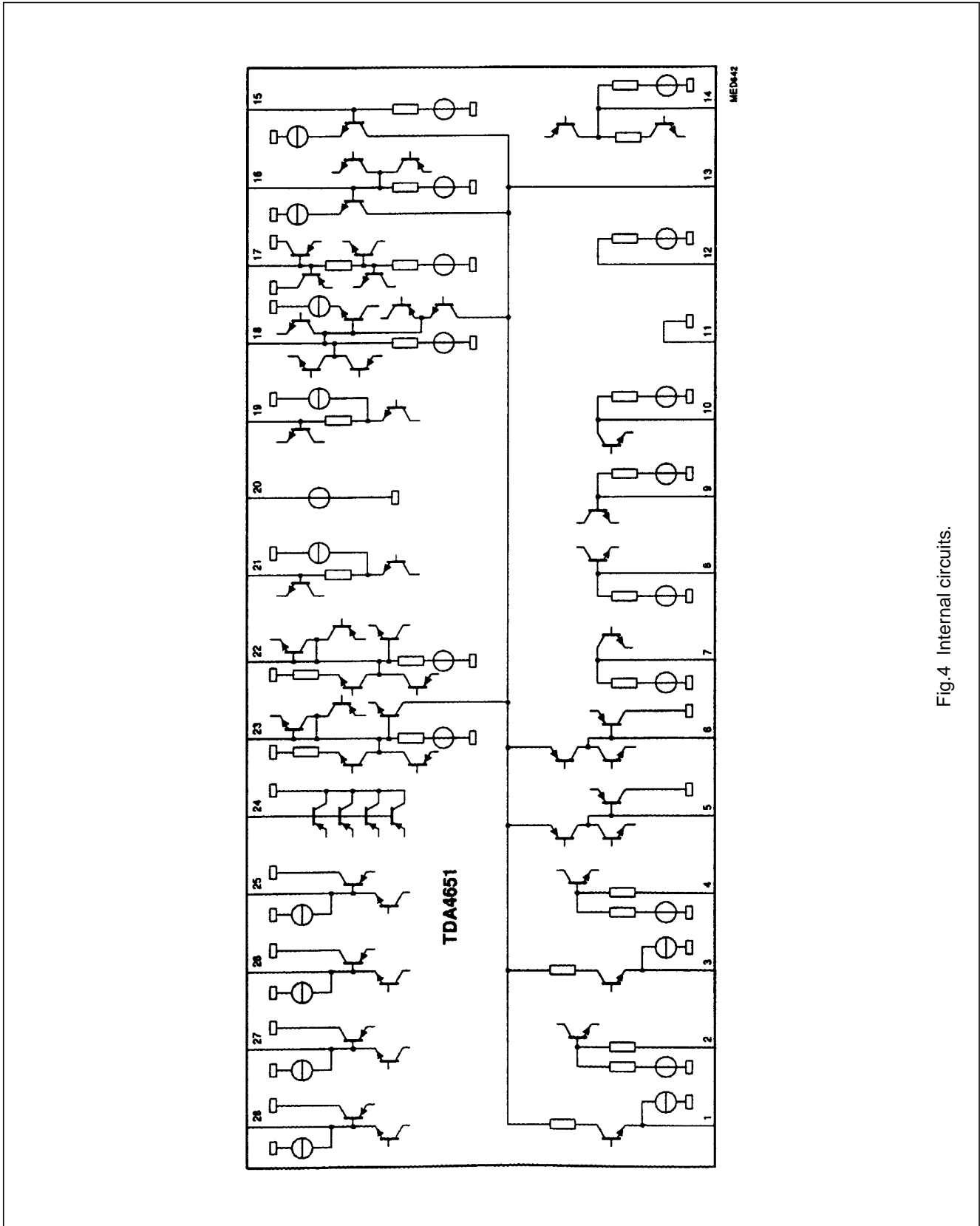


Fig.4 Internal circuits.

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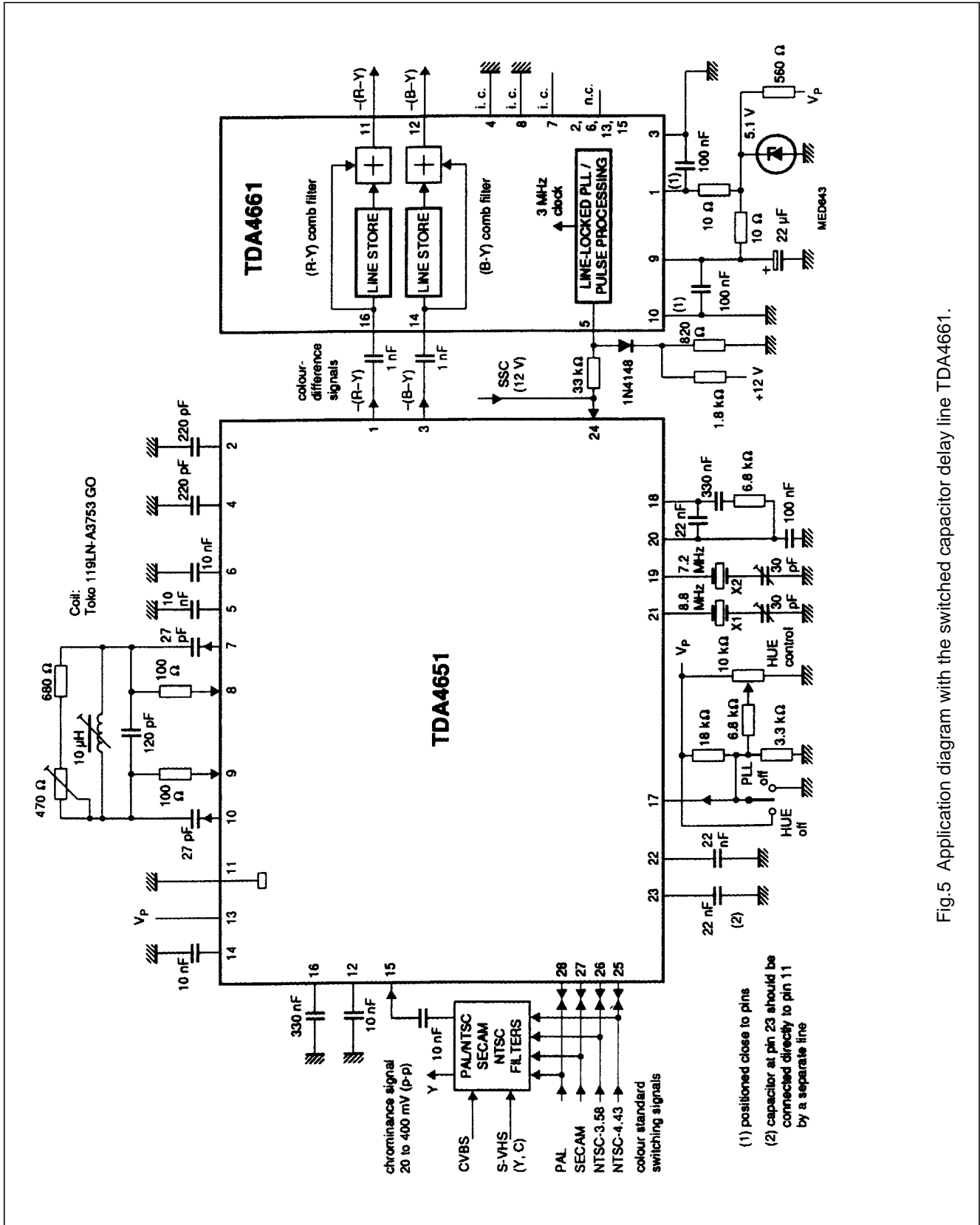


Fig.5 Application diagram with the switched capacitor delay line TDA4661.

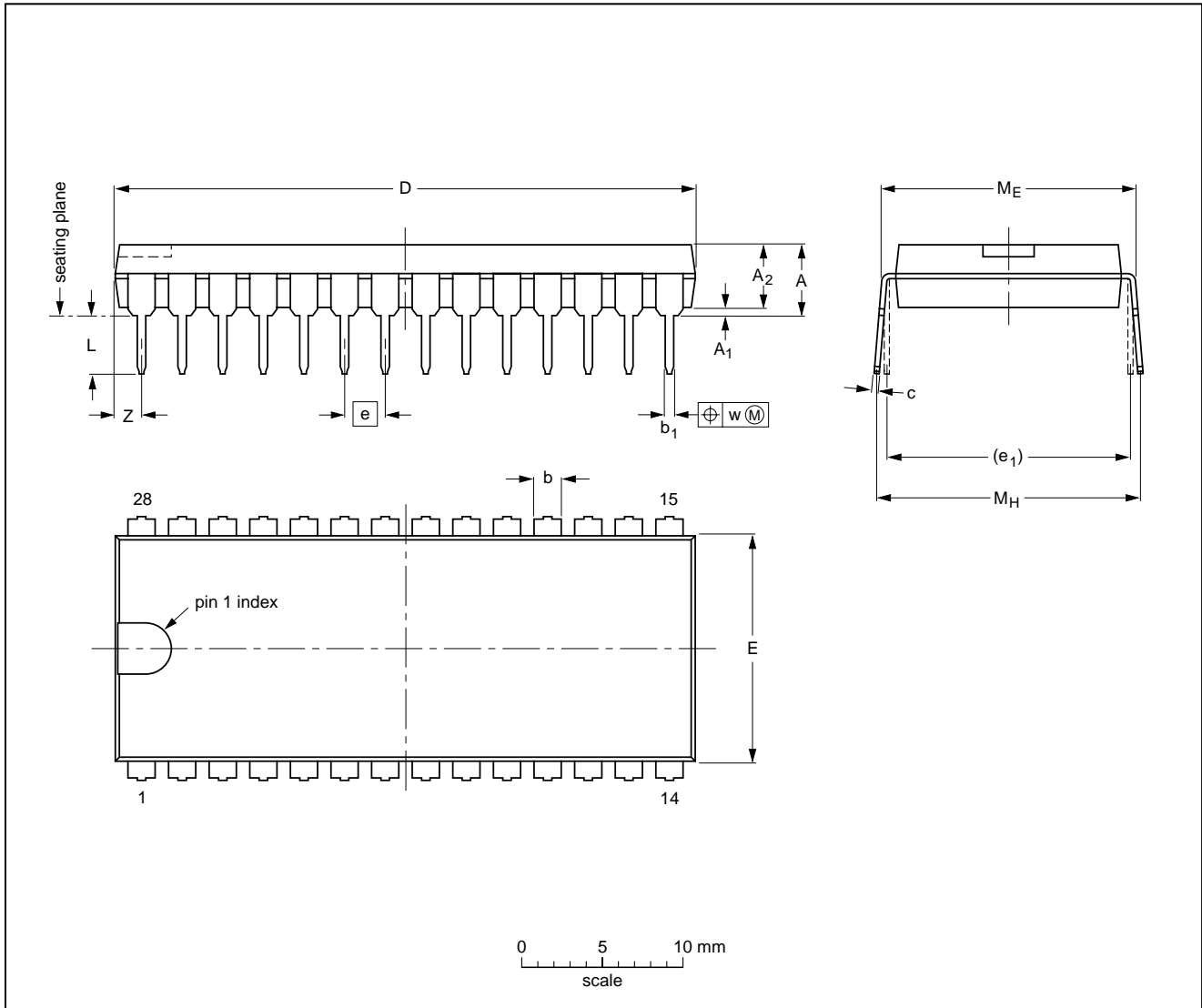
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## PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

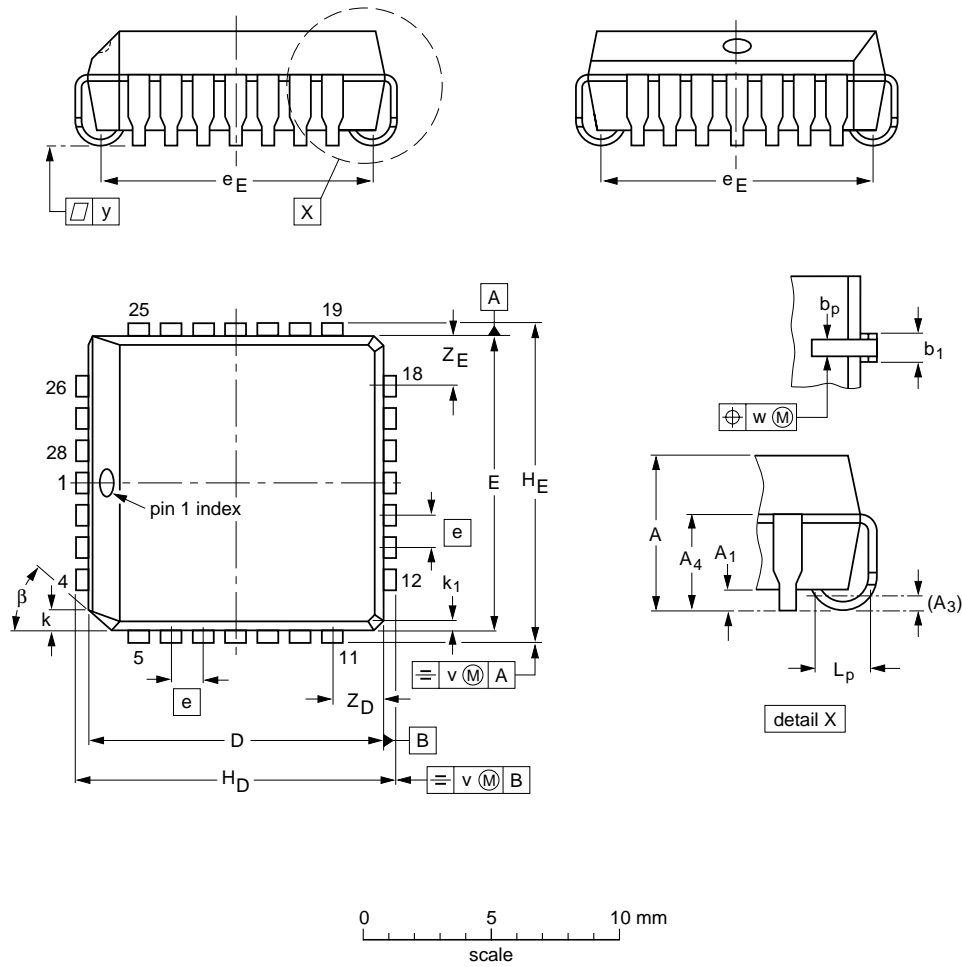
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				92-11-17 95-01-14

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PLCC28: plastic leaded chip carrier; 28 leads

SOT261-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A <sub>1</sub> min.	A <sub>3</sub>	A <sub>4</sub> max.	b <sub>p</sub>	b <sub>1</sub>	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>D</sub>	e <sub>E</sub>	H <sub>D</sub>	H <sub>E</sub>	k	k <sub>1</sub> max.	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup> max.	Z <sub>E</sub> <sup>(1)</sup> max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

**Note**

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT261-2					92-11-17 95-02-25

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### PLCC

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all PLCC packages.

The choice of heating method may be influenced by larger PLCC packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering techniques can be used for all PLCC packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

# Multistandard colour decoder with negative colour difference output signals

TDA4651

## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.