

TYPES SN54LS589, SN74LS589

8-BIT SHIFT REGISTERS WITH INPUT LATCHES AND 3-STATE OUTPUT

REVISED DECEMBER 1983

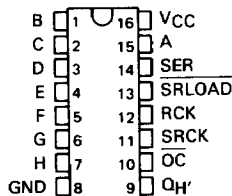
- 8-Bit Parallel Storage Register Inputs
- Shift Register has Direct Overriding Load and Power-Up Clear
- Guaranteed Shift Frequency . . . DC to 20 MHz

description

The 'LS589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register with 3-state outputs. Both the storage register and shift register have positive-edge triggered clocks. The shift register has a direct load (from storage) input.

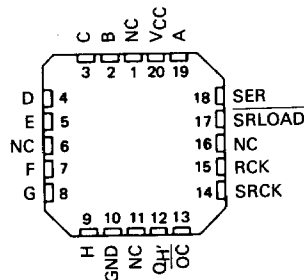
SN54LS589 . . . J PACKAGE
SN74LS589 . . . J OR N PACKAGE

(TOP VIEW)



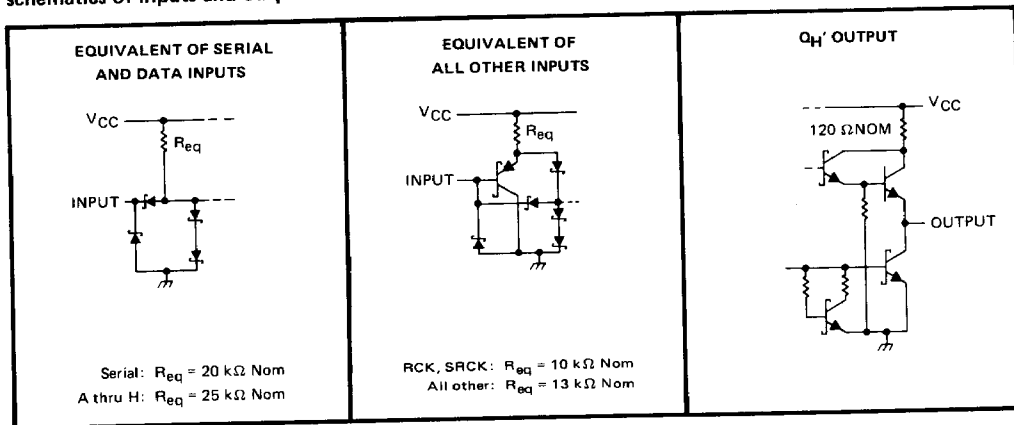
SN54LS589 . . . FK PACKAGE
SN74LS589 . . . FN PACKAGE

(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

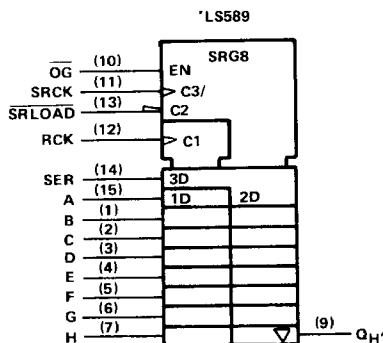
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TYPES SN54LS589, SN74LS589

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logic symbol†



Pin numbers shown on logic notation are for J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS589	-55°C to 125°C
SN74LS589	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS*			SN74LS*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-1	mA
I_{OL}	Low-level output current			8			16	mA
f_{SRCK}	Shift clock frequency	0		20	0		20	MHz
t_w	Pulse duration	SRCK	High	15		15		ns
			Low	35		35		
		RCK	20		20			
		SRLOAD	40		40			
t_{su}	Setup time	Data before RCK ↑	20		20		ns	
		SER before SRCK ↑	20		20			
		SRLOAD inactive before SRCK ↑	30		30			
		RCK ↑ before SRLOAD ↑ (see Note 2)	40		40			
t_h	Hold time	Data after RCK ↑	0		0		ns	
		SER after SRCK ↑	0		0			
T_A	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: The RCK ↑ to SRLOAD setup time ensures the data saved by RCK ↑ will also be loaded into the counter.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*		SN74LS*		UNIT
		MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.5		-1.5		V
V _{OH}	V _{CC} = MIN, I _{OH} = -1 mA	2.4	3.2	2.4	3.2	V
V _{OL}	V _{CC} = MIN, I _{OL} = 8 mA I _{OL} = 16 mA	0.25	0.4	0.25	0.4	V
I _{OZH}	V _{CC} = MAX, V _O = 2.7 V	20		20		μA
I _{OZL}	V _{CC} = MAX, V _O = 0.4 V	-0.2		-0.2		mA
I _{IL}	V _{CC} = MAX, V _I = 7 V	-0.1		-0.1		mA
I _{IH}	V _{CC} = MAX, V _I = 2.7 V	20		20		μA
I _{IL}	SER, A → H	-0.4		-0.4		mA
	Others	-0.2		-0.2		
I _{OS} §	V _{CC} = MAX, V _O = 0 V	-20	-100	-20	-100	mA
I _{CC}	I _{CCH}	30 45		30 45		mA
	I _{CCL}	30 45		30 45		
	I _{CCZ}	35 53		35 53		

† For conditions shown as MIN or MAX use the appropriate values specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS589			UNIT
				MIN	TYP	MAX	
f _{max}	SRCK †			20	35	MAX	MHz
†PLH	SRCK †	Q _H '	R _L = 1 kΩ, C _L = 30 pf	15		23	ns
†PHL				20		30	
†PLH	SRLOAD †	Q _H '		38		57	ns
†PHL				29		44	
†PLH	RCK †	Q _H '	R _L = 1 kΩ, C _L = 30 pf, SRLOAD = L	41		60	ns
†PHL				32		48	
†PZH	OC	Q _H '	R _L = 667 Ω, C _L = 5 pf	10		15	ns
†PZL				18		27	
†PHZ				20		30	
†PLZ				20		30	

NOTE 2: See General Information Section for load circuits and voltage waveforms.

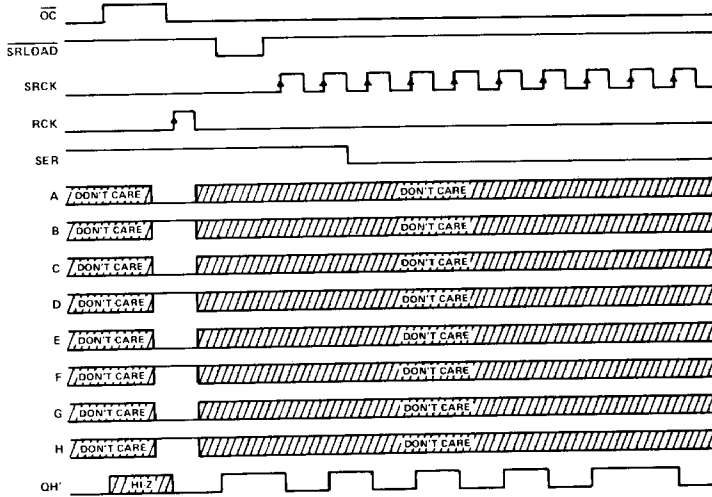
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timing diagram

'LS589



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