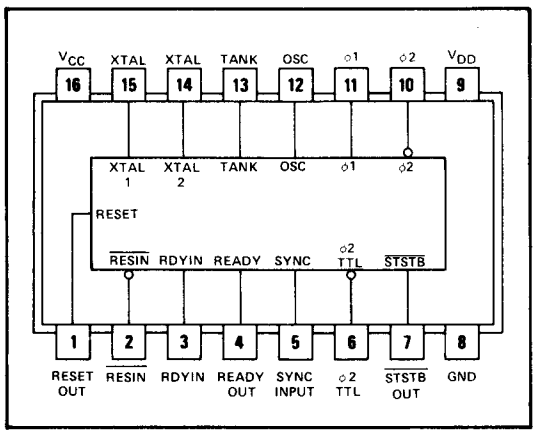
TYPE SN74LS424 (TIM8224)
TWO-PHASE CLOCK GENERATOR/DRIVER

BULLETIN NO. DL-S 12475, OCTOBER 1976—REVISED AUGUST 1977

- Designed to be Interchangeable With Intel 8224
- Single-Chip Clock Driver With Self-Contained Oscillator
- Specifically Designed to Drive All 8080A Microprocessors

J OR N PACKAGE
(TOP VIEW)



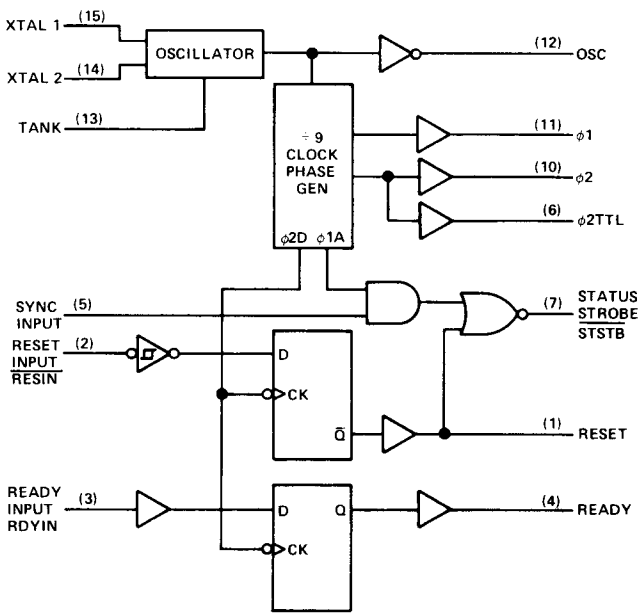
description

This clock generator is capable of driving 12-volt lines. It contains a crystal-controlled oscillator, a divide-by-nine clock phase generator, two high-level drivers, and auxiliary circuitry.

The internal oscillator is designed to operate with fundamental-mode crystals, or with overtone-mode crystals when using a parallel-tuned circuit connected to the tank terminal, pin 13. The oscillator output appears on pin 12 and drives the divide-by-nine counter. The ÷9 clock phase generator output consists of phases $\phi 2$ for driving MOS inputs and $\phi 2$ TTL for driving TTL. Three other TTL outputs, status strobe, reset, and ready, are coupled to the divide-by-nine counter. A sync input from the 8080A is AND'ed with $\phi 1A$ to produce the status strobe. The power-on reset also generates the status strobe signal through an output NOR gate. The reset input works on a voltage-level basis by use of a Schmitt trigger. A rising voltage waveform is triggered at a particular voltage. A synchronized ready output is obtained by clocking with a $\phi 2$ signal.

The SN74LS424 is characterized for operation over the temperature range of 0°C to 70°C.

functional block diagram



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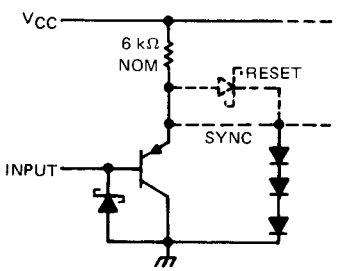
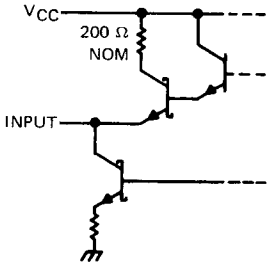
schematics of inputs and outputs

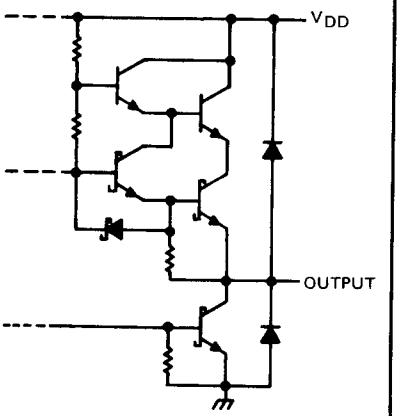
EQUIVALENT OF RESET AND SYNC INPUTS



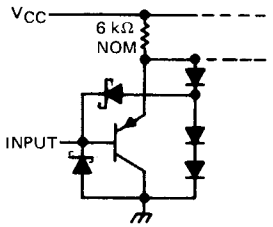
EQUIVALENT OF XTAL 1 AND XTAL 2 NODES



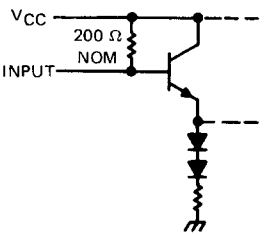
TYPICAL OF $\phi1$, $\phi2$ OUTPUTS



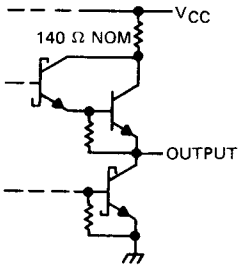
EQUIVALENT OF READY INPUT



EQUIVALENT OF TANK INPUT



TYPICAL OF ALL OUTPUTS EXCEPT $\phi1$, $\phi2$



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Supply voltage, V_{DD}	17 V
Input voltages (sync, reset, ready)	7 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Ready input setup time, $t_{su(RDYIN)}$	$50 - \frac{4t_c}{9}$			ns
Ready input hold time, $t_{h(RDYIN)}$	$\frac{4t_c}{9}$			ns
Operating free-air temperature range, T_A	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	Reset input			2.6			V
		All others			2			
V_{IL}	Low-level input voltage						0.8	V
$V_{T+} - V_{T-}$	Hysteresis	Reset input			0.25			V
V_{IK}	Input clamp voltage		V_{CC} = 4.75 V, V_{DD} = 11.4 V	I_I = −5 mA			−1	V
				I_I = −18 mA			−1.5	
V_{OH}	High-level output voltage	$\phi1$, $\phi2$	V_{CC} = 4.75 V, V_{DD} = 11.6 V	I_{OH} = −100 μA	9.4	10.4		V
		Ready, reset			3.6	3.9		
		Others		I_{OH} = −1 mA	2.4	3.1		
V_{OL}	Low-level output voltage	$\phi1$, $\phi2$, reset, status strobe	V_{CC} = 4.75 V, V_{DD} = 11.4 V	I_{OL} = 2.5 mA		0.2	0.45	V
		$\phi2$ TTL, osc		I_{OL} = 15 mA		0.25	0.45	
I_I	Input current at maximum input voltage		V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 7 V				100	μA
I_{IH}	High-level input current		V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 5.25 V				10	μA
I_{IL}	Low-level input current		V_{CC} = 5.25 V, V_{DD} = 12.6 V, V_I = 0.4 V				−0.25	mA
I_{OS}	Short-circuit circuit current§	All except $\phi1$, $\phi2$	V_{CC} = 5 V, V_{DD} = 12 V		−10		−60	mA
I_{CC}	Supply current from V_{CC}		V_{CC} = 5.25 V, V_{DD} = 12 V			70	115	mA
I_{DD}	Supply current from V_{DD}		V_{DD} = 12.6 V, V_{CC} = 5 V, See Note 2			6	12	mA
C_i	Input capacitance		V_{CC} = 5 V, V_{DD} = 12 V, V_I = 2.5 V, f = 1 MHz, See Note 2				8	pF

‡All typical values are at V_{CC} = 5 V, V_{DD} = 12 V, T_A = 25°C.
§Not more than one output should be shorted at a time. $\phi1$ and $\phi2$ do not have short-circuit protection.
NOTE 2: I_{CC} and I_{DD} are measured with outputs disabled and open.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, T_A = 25°C, see figure 1

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum oscillator frequency		27			MHz
$t_{c(osc)}$	Oscillator cycle time			$\frac{t_c}{9}$†		ns
$t_{w(\phi1)}$	Pulse width, $\phi1$ high	$\phi1$ and $\phi2$: C_L = 20 pF to 110 pF, See Figure 2	$\frac{2t_c}{9} - 20$			ns
$t_{w(\phi2)}$	Pulse width, $\phi2$ high		$\frac{5t_c}{9} - 35$			ns
$t_{w(SS)}$	Pulse width, status strobe low		$\frac{t_c}{9} - 15$			ns
$t_{r(\phi)}$	Rise time, clock outputs	$\phi2$ TTL: C_L = 30 pF, R1 = 300 Ω, R2 = 600 Ω, See Figure 3			20	ns
$t_{f(\phi)}$	Fall time, clock outputs				20	ns
$t_{\phi1L,\phi2H}$	Delay time, $\phi1$ low to $\phi2$ high		0			ns
$t_{\phi2L,\phi1H}$	Delay time, $\phi2$ low to $\phi1$ high	Status Strobe: C_L = 15 pF, R1 = 2 kΩ, R2 = 4 kΩ, See Figure 3	$\frac{2t_c}{9} - 30$			ns
$t_{\phi1H,\phi2H}$	Delay time, $\phi1$ high to $\phi2$ high		$\frac{2t_c}{9}$		$\frac{2t_c}{9} + 20$	ns
$t_{\phi2,\phi2T}$	Delay time, $\phi2$ to $\phi2$ TTL	OSC, Ready, Reset: C_L = 10 pF, R1 = 2 kΩ, R2 = 4 kΩ, See Figure 3	−5		15	ns
$t_{\phi2H,SSL}$	Delay time, $\phi2$ high to status strobe low		$\frac{6t_c}{9} - 50$		$\frac{6t_c}{9}$	ns
$t_{RV,\phi2L}$	Delay time, ready or reset output valid to phase 2 low		$\frac{4t_c}{9} - 25$			ns

† $t_c \equiv t_{c(\phi1)} = t_{c(\phi2)}$

EXAMPLE: switching times for f_{osc} = 20 MHz ($t_{c(\phi1)} = t_{c(\phi2)}$ = 450 ns)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Oscillator frequency	Same as above		20		MHz
$t_{c(osc)}$	Oscillator cycle time			50		ns
$t_{w(\phi1)}$	Pulse width, $\phi1$ high		80			ns
$t_{w(\phi2)}$	Pulse width, $\phi2$ high		215			ns
$t_{w(SS)}$	Pulse width, status strobe		35			ns
$t_{\phi1L,\phi2H}$	Delay time, $\phi1$ low to $\phi2$ high		0			ns
$t_{\phi2L,\phi1H}$	Delay time, $\phi2$ low to $\phi1$ high		70			ns
$t_{\phi1H,\phi2H}$	Delay time, $\phi1$ high to $\phi2$ high		100		120	ns
$t_{\phi2H,SSL}$	Delay time, $\phi2$ high to status strobe low		250		300	ns
$t_{RV,\phi2L}$	Delay time, ready or reset output valid to $\phi2$ low		175			ns

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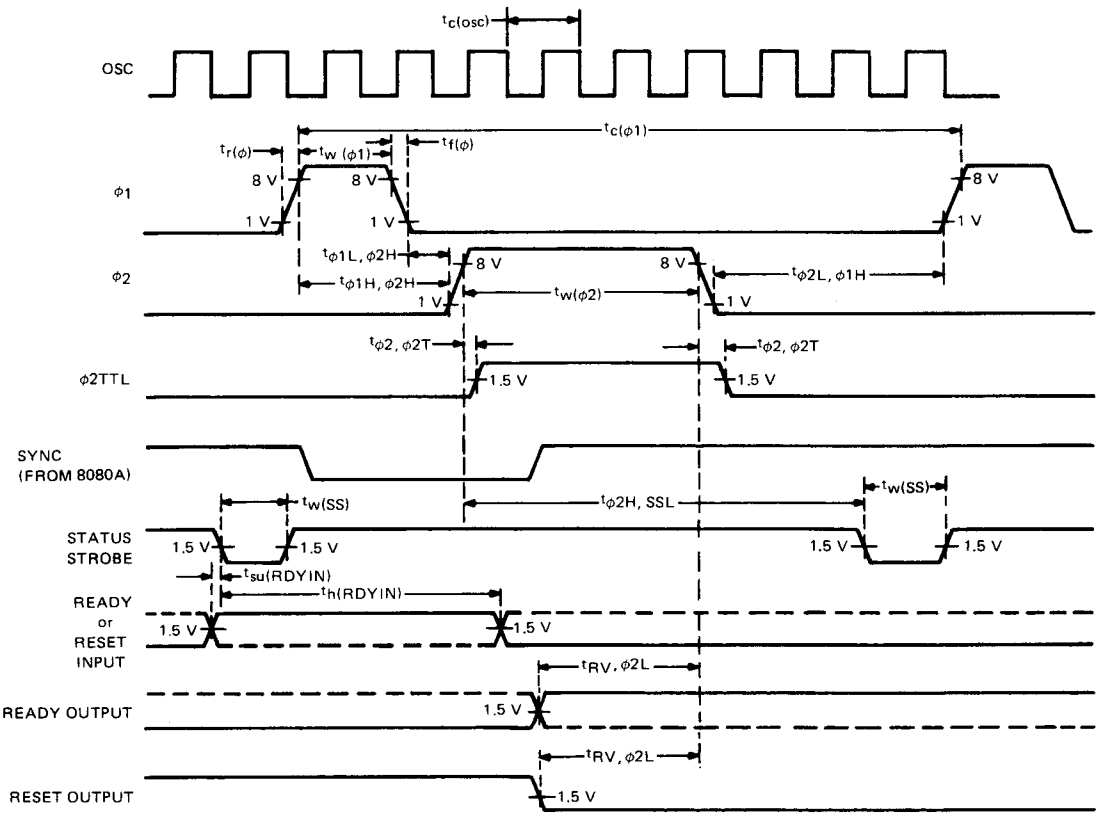
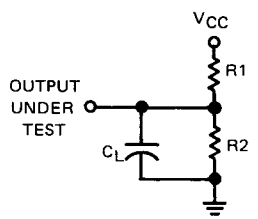
PARAMETER MEASUREMENT INFORMATION



NOTE: Transistion times, pulse widths, and interpulse relationships are distorted in this diagram in order to define various intervals, See Figure 5 for correct relative relationships.

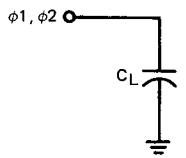
VOLTAGE WAVEFORMS

FIGURE 1



LOAD CIRCUIT

FIGURE 2



LOAD CIRCUIT

FIGURE 3

TYPICAL APPLICATION DATA

The 'LS424 is a single-chip clock generator/driver for 8080A CPU's, furnishing three clocks (ϕ1, ϕ2 and ϕ2 TTL), status strobe, reset, and ready signals. The 'LS424 contains a crystal-controlled oscillator, a divide-by-nine counter, two high-level drivers, and several auxiliary logic functions. Figure 4 is a functional block diagram of the SN74LS424. Figure 5 shows the relationship between ϕ1, ϕ2, and the oscillator frequency period.

oscillator

A high order of clock frequency stability is provided by use of an external quartz crystal to set the oscillator frequency which is nine times the operating frequency of the 8080A. The quartz crystal is operated in a series-resonant mode. A fundamental-mode crystal requires no auxiliary circuitry, but an overtone-mode crystal requires an ac-coupled parallel-resonant circuit to be connected to the tank connection (pin 13). The parallel-resonant circuit, tuned to the oscillator frequency, compensates for the lower Q of the overtone-mode crystal. The required size of the circuit components can be calculated from $f = 1/2\pi\sqrt{LC}$ where f is the oscillator frequency, L is inductance value, and C is capacitance value. Figure 6 shows an ac-coupled parallel-tuned circuit used with the SN74LS424.

clock phase generator

The divide-by-nine clock phase generator contains a divide-by-nine counter, logic required to shape the clock pulses as shown under parameter measurement information, gates and flip-flops to generate auxiliary signals, and output drivers. The divide-by-nine counter waveforms are combined with gates to form a ϕ1 pulse with a width of two periods of the oscillator frequency, repeating at intervals of nine oscillator periods. Similarly, the ϕ2 pulse, having a width of five oscillator frequency periods, is formed lagging the ϕ1 pulse by two oscillator periods.

ϕ1 and ϕ2 outputs are provided by high-level drivers for direct connection to the 8080A CPU. ϕ2 TTL is derived in a manner similar to ϕ1 and ϕ2, but the output driver output is at TTL voltage levels. The ϕ2 TTL pulse width is the same as ϕ2. A ϕ2 TTL application is clocking in direct memory access activities. Figure shows the 'LS424 connected to an 8080A, quartz crystal, and LC circuits.

status strobe

The 8080A CPU puts status information on its data bus at the beginning of each machine cycle that defines the nature of the machine operation for that cycle. A sync signal from the 8080A is gated by an internal timing signal (ϕ1A) and becomes a status strobe to notify system components that the status data is present on 8080A status output lines. The status strobe signal connects directly to the 'S428 system controller.

The status strobe signal is alternatively generated by the reset input. An external RC series network connected to V_{CC} and the reset input will provide a rising voltage waveform when V_{CC} is turned on. An internal Schmitt trigger circuit generates a sharp, fast-rising waveform when the reset input reaches a particular voltage value. The Schmitt trigger is connected to the D input of a flip-flop clocked by ϕ2D. When power is turned on, the combination of internal and external circuitry will produce a status strobe signal. A manual reset switch can be connected as in figure 6 to the RC network to produce reset and status strobe signals for the 8080A.

The ready signal indicates to the 8080A that an external device has completed transfer of data to or from the data bus. A ready signal input to the 'LS424 drives the D input of a flip-flop clocked by an internal ϕ2D signal. Timing requirements of the 8080A machine cycle are met by the synchronization with the system clocks provided by the flip-flop. This implementation saves about 200 ns of system time during memory cycles (as contrasted with generating a "wait request" within the 8080A's MOS logic) since the bipolar logic of the 'LS424 has much less delay.

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TYPICAL APPLICATION DATA

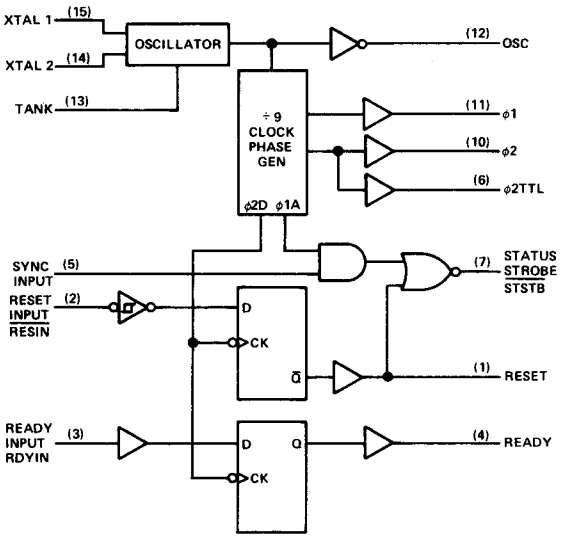
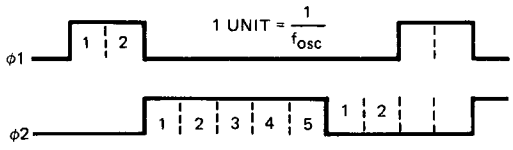
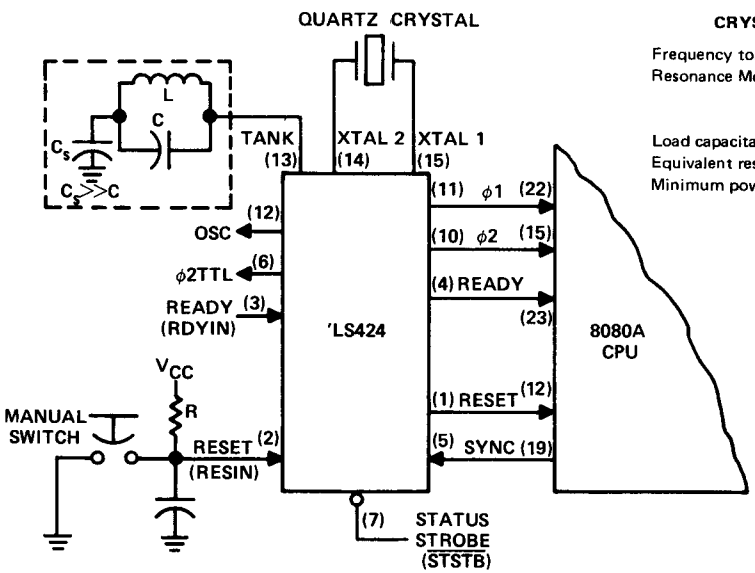


FIGURE 4



Example: 8080A cycle = 450 ns
f_{osc}: 20 MHz (unit = 50 ns)
$t_{w(\phi1)}$ = 100 ns (2 X 50 ns)
$t_{w(\phi2)}$ = 250 ns (5 X 50 ns)
$t_{\phi2L, \phi1H}$ = 100 ns (2 X 50 ns)

FIGURE 5



CRYSTAL REQUIREMENTS

Frequency tolerance: ±0.005% for 0°C to 70°C
Resonance Mode: series, fundamental (use 3rd overtone mode with tank circuit)
Load capacitance: 20 pF to 35 pF
Equivalent resistance: 20 Ω to 75 Ω
Minimum power dissipation: 4 mW

FIGURE 6