

# SN54ALS996, SN74ALS996 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

SDAS098B – OCTOBER 1984 – REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- $T/\bar{C}$  Determines True or Complementary Data at Q Outputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

## description

These 8-bit latches are designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. The Q outputs are designed with bus-driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) input when the enable ( $\bar{E}N$ ) input is low. Data can be read back onto the data inputs by taking the read ( $\bar{R}D$ ) input low, in addition to having  $\bar{E}N$  low. When  $\bar{E}N$  is high, both the read-back and write modes are disabled. Transitions on  $\bar{E}N$  should only be made with CLK high to prevent false clocking.

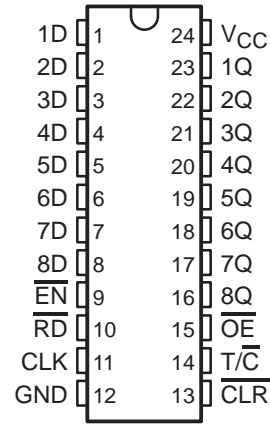
The polarity of the Q outputs can be controlled by the polarity ( $T/\bar{C}$ ) input. When  $T/\bar{C}$  is high, Q is the same as is stored in the flip-flops. When  $T/\bar{C}$  is low, the output data is inverted. The Q outputs can be placed in the high-impedance state by taking the output-enable ( $\bar{O}E$ ) input high.  $\bar{O}E$  does not affect the internal operation of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear ( $\bar{C}LR$ ) input resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

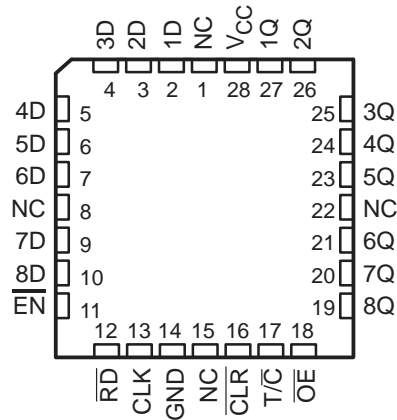
The -1 version of the SN74ALS996 is identical to the standard version, except that the recommended maximum  $I_{OL}$  for the -1 version is increased to 48 mA. There is no -1 version of the SN54ALS996.

The SN54ALS996 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS996 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**SN54ALS996 . . . JT PACKAGE  
SN74ALS996 . . . DW OR NT PACKAGE  
(TOP VIEW)**



**SN54ALS996 . . . FK PACKAGE  
(TOP VIEW)**

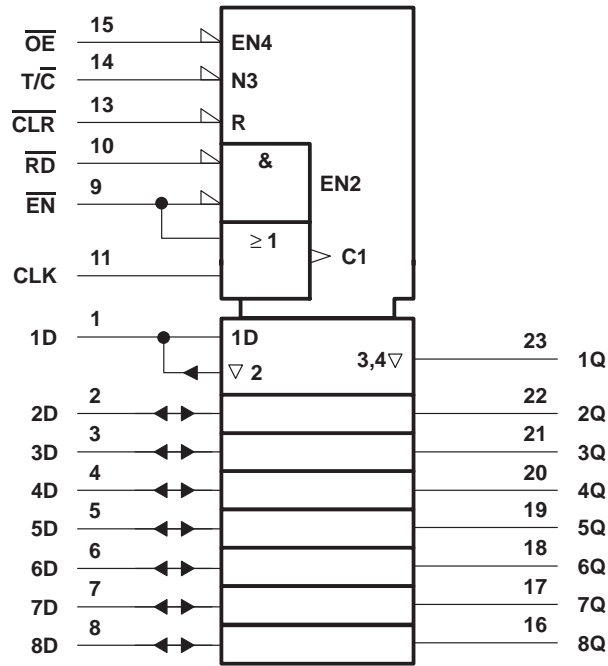


NC – No internal connection

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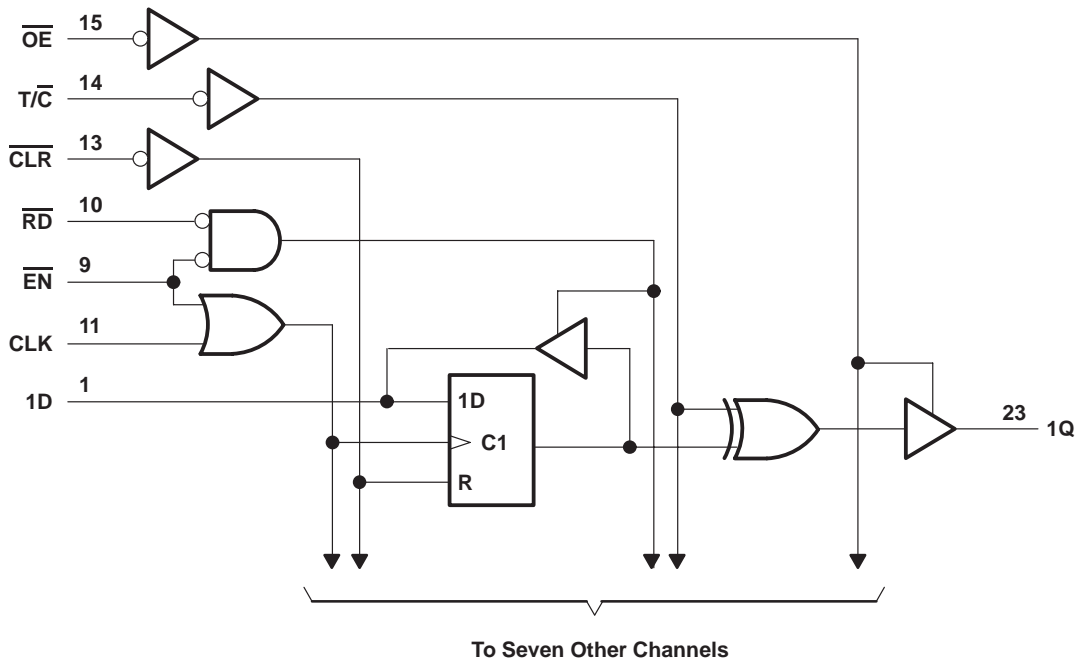
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)

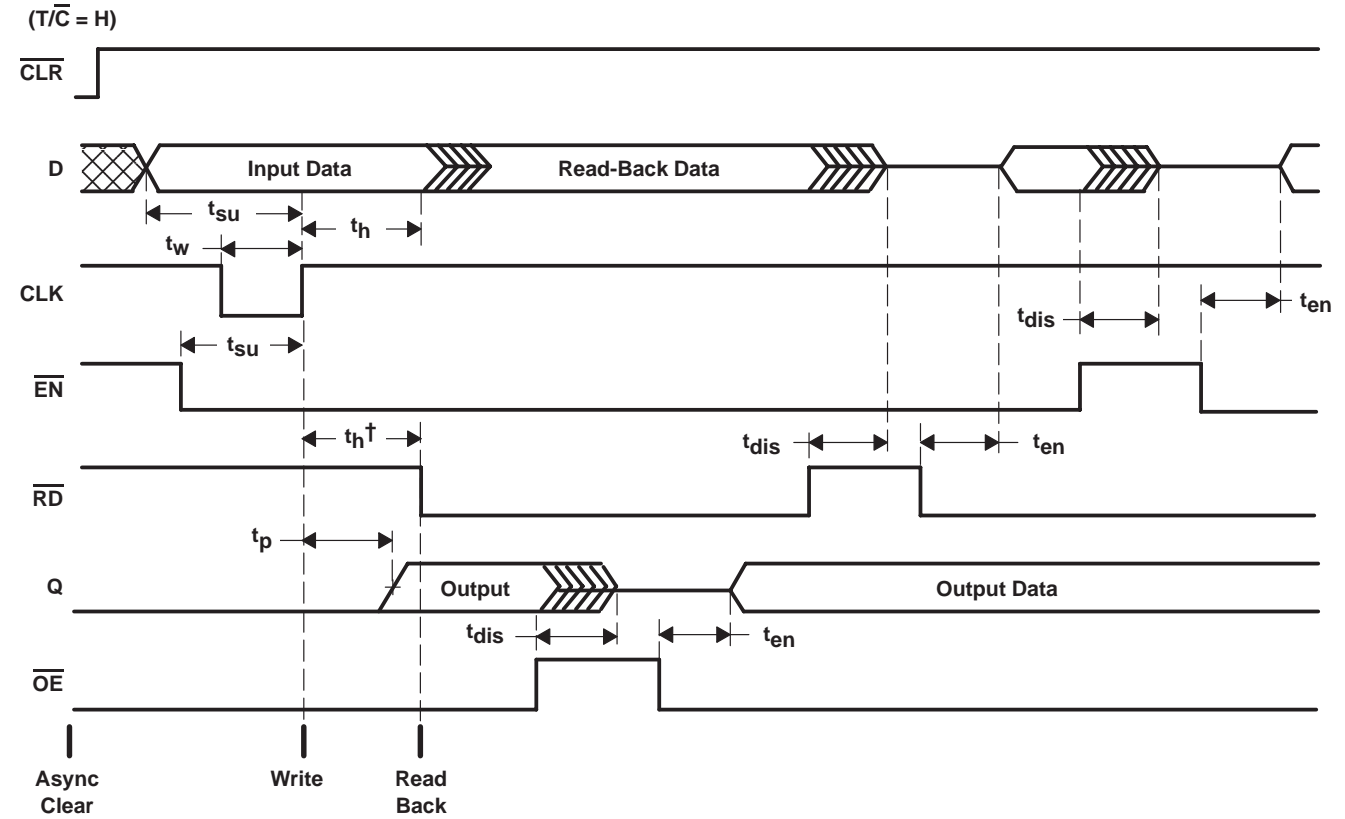


Pin numbers shown are for the DW, JT, and NT packages.

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## timing diagram



$^\dagger$  This hold time ensures that the read-back circuit will not create a conflict on the input data bus.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $^\ddagger$

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ ( $\overline{OE}$ , $\overline{RD}$ , $\overline{EN}$ , CLK, $\overline{CLR}$ , and $T/\overline{C}$ ) .....	7 V
Voltage applied to D inputs and to disabled 3-state outputs .....	5.5 V
Operating free-air temperature range, $T_A$ : SN54ALS996 .....	-55°C to 125°C
SN74ALS996 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

$^\ddagger$  Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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## 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

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### recommended operating conditions

			SN54ALS996			SN74ALS996			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.5	5	5.5	V	
V <sub>IH</sub>	High-level input voltage	All inputs				2			V	
		All inputs except $\overline{OE}$ , $\overline{RD}$	2							
		$\overline{OE}$ , $\overline{RD}$	2.2							
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V	
I <sub>OH</sub>	High-level output current	Q	-1			-2.6			mA	
		D	-0.4			-0.4				
I <sub>OL</sub>	Low-level output current	Q	12			24			mA	
		D	8			8				
f <sub>clock</sub>	Clock frequency	0	35			0	35			MHZ
t <sub>w</sub>	Pulse duration	$\overline{CLR}$ low	10			10			ns	
		CLK low	14.5			14.5				
		CLK high	14.5			14.5				
t <sub>su</sub>	Setup time	Data before CLK↑	15			15			ns	
		$\overline{EN}$ low before CLK↑	10			10				
		CLK high before $\overline{EN}$ ↑‡	15			15				
		$\overline{CLR}$ high (inactive) before CLK↑	10			10				
t <sub>h</sub>	Hold time	Data after CLK↑	1			0			ns	
		$\overline{EN}$ low after CLK↑	5			5				
		$\overline{RD}$ high after CLK↑§	5			5				
T <sub>A</sub>	Operating free-air temperature	-55	125			0	70			°C

† Applies only to the -1 version and only if V<sub>CC</sub> is maintained between 4.75 V and 5.25 V

‡ This setup time ensures that  $\overline{EN}$  will not false clock the data register.

§ This hold time ensures that there will be no conflict on the input data bus.

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## 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54ALS996		SN74ALS996		UNIT	
				MIN	TYP†	MAX	MIN		TYP†
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA		-1.2		-1.2		V	
V <sub>OH</sub>	All outputs	V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA		V <sub>CC</sub> - 2		V <sub>CC</sub> - 2		V	
	Q	V <sub>CC</sub> = 4.5 V		2.4	3.2	2.4	3.2		
V <sub>OL</sub>	D	V <sub>CC</sub> = 4.5 V		I <sub>OL</sub> = 4 mA		0.25 0.4		V	
				I <sub>OL</sub> = 8 mA		0.35 0.5			
	Q	V <sub>CC</sub> = 4.5 V		I <sub>OL</sub> = 12 mA		0.25 0.4			
				I <sub>OL</sub> = 24 mA		0.35 0.5			
				I <sub>OL</sub> = 48 mA‡		0.35 0.5			
I <sub>OZH</sub>	Q	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V		20		20		μA	
I <sub>OZL</sub>	Q	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.4 V		-20		-20		μA	
I <sub>I</sub>	D inputs	V <sub>CC</sub> = 5.5 V		V <sub>I</sub> = 5.5 V		0.1		mA	
	All others			V <sub>I</sub> = 7 V		0.1			
I <sub>IH</sub>	D inputs§	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		20		20		μA	
	All others			20		20			
I <sub>IL</sub>	D inputs§	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-0.1		-0.1		mA	
	All others			-0.1		-0.1			
I <sub>O</sub> ¶	V <sub>CC</sub> = 5.5 V, CLR = 2.5 V		V <sub>O</sub> = 2.25 V		-20	-112	-30	-112	mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, EN, RD low		Outputs high		35	55	35	55	mA
			Outputs low		55	85	55	85	
			Outputs disabled		42	65	42	65	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ Applies only to the -1 version and only if V<sub>CC</sub> is maintained between 4.75 V and 5.25 V

§ For I/O ports (Q<sub>A</sub> thru Q<sub>H</sub>), the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

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## 8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

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### switching characteristics (see Figure 1)

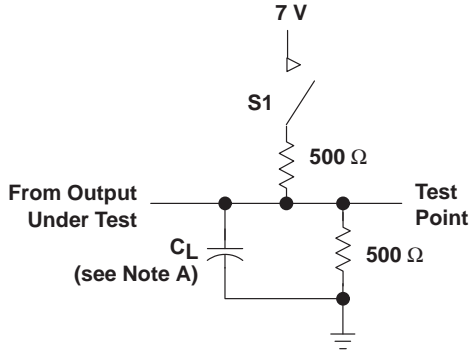
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54ALS996		SN74ALS996		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			35		35	MHz	
t <sub>PLH</sub>	CLK (T/C = H or L)	Q	5	30	5	28	ns
t <sub>PHL</sub>			5	24	5	28	
t <sub>PLH</sub>	CLR (T/C = L)	Q	5	27	7	27	ns
t <sub>PHL</sub>	CLR (T/C = H)		5	23	7	23	
t <sub>PLH</sub>	T/C	Q	4	23	5	23	ns
t <sub>PHL</sub>			5	23	5	23	
t <sub>PHL</sub>	CLR	D	5	30	8	30	ns
t <sub>en</sub> ‡	RD	D	2	18	3	16	ns
t <sub>dis</sub> §			1	19	3	19	
t <sub>en</sub> ‡	EN	D	2	17	3	16	ns
t <sub>dis</sub> §			1	19	3	19	
t <sub>en</sub> ‡	OE	Q	2	15	4	15	ns
t <sub>dis</sub> §			1	11	1	10	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

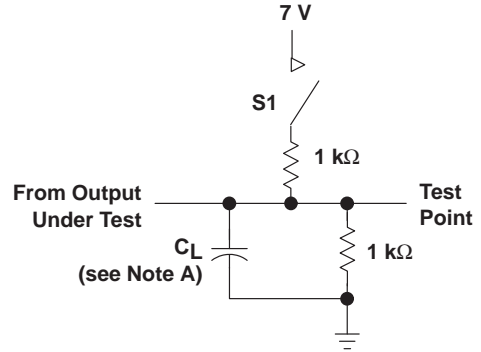
‡ t<sub>en</sub> = t<sub>PZH</sub> or t<sub>PZL</sub>

§ t<sub>dis</sub> = t<sub>PHZ</sub> or t<sub>PLZ</sub>

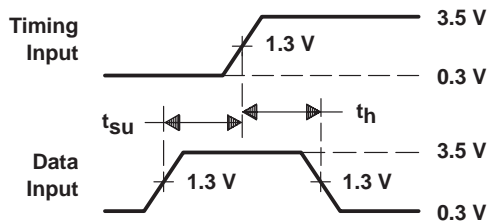
PARAMETER MEASUREMENT INFORMATION



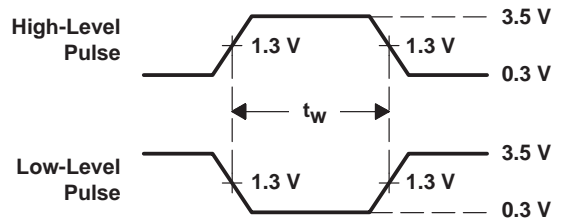
LOAD CIRCUIT FOR Q OUTPUTS



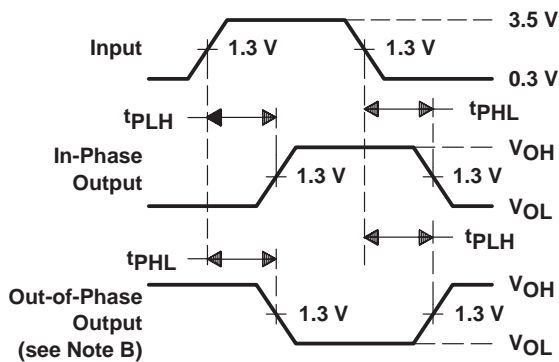
LOAD CIRCUIT FOR D OUTPUTS



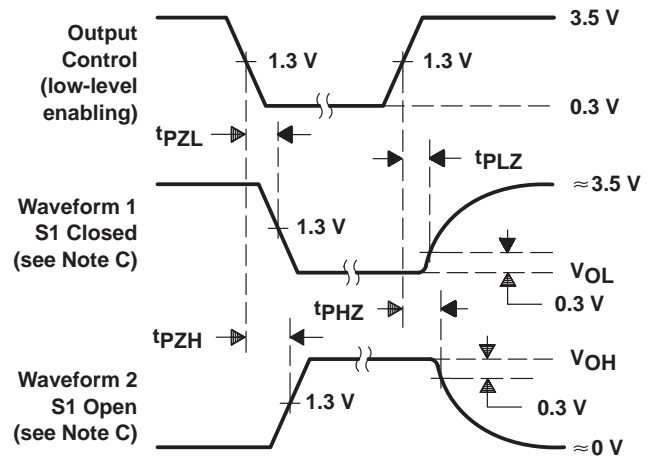
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. When measuring propagation delay times of 3-state outputs, switch S1 is open.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. All input pulses have the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $t_r = t_f = 2 \text{ ns}$ , duty cycle = 50%.

Figure 1. Load Circuits and Voltage Waveforms





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