

# SN74143

## 4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVER

NOVEMBER 1971—REVISED MARCH 1988

- **15-mA Constant-Current Outputs**

For Driving Common-Anode LEDs such as TIL302 or TIL303 Without Series Resistors

- **Universal Logic Capabilities**

Ripple Blanking of Extraneous Zeros  
Latch Outputs Can Drive Logic Processors Simultaneously

Decimal Point Driver Is Included

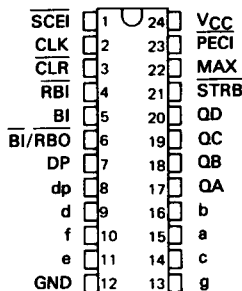
- **Synchronous BCD Counter Capability**

Cascadable to N-Bits

Look-Ahead-Enable Techniques Minimize Speed Degradation When Cascaded for Large-Word Display

Direct Clear Input

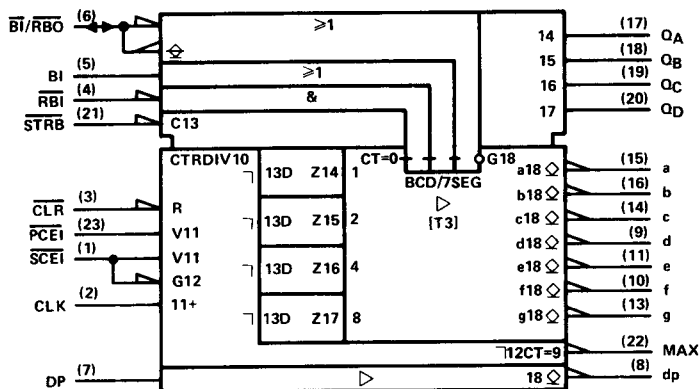
N PACKAGE  
(TOP VIEW)



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logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### description

This TTL MSI circuit contains the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input. The serial-count-enable, actually two internal emitters, is rated as one standard Series 54/74 load. The logic outputs, except  $\overline{RBO}$ , have active pull-ups.

The SN74143 driver output is designed specifically to maintain a relatively constant on-level sink current of approximately 15 milliamperes from output "a" through "g" and seven milliamperes from output "dp" over a voltage range from one to five volts. Any number of LED's in series may be driven as long as the output voltage rating is not exceeded.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 megahertz and power dissipation is typically 280 milliwatts. The SN74143 is characterized for operation from 0°C to 70°C.

**PRODUCTION DATA** documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS**  
**INSTRUMENTS**

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# SN74143 4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVER

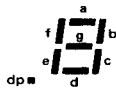
## description (continued)

Functions of the inputs and outputs of these devices are as follows:

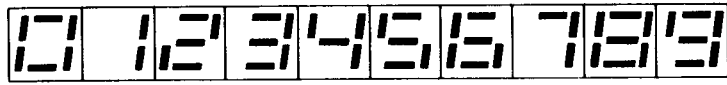
FUNCTION	PIN NO.	DESCRIPTION
CLEAR INPUT	3	When low, resets and holds counter at 0. Must be high for normal counting.
CLOCK INPUT	2	Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high).
PARALLEL COUNT ENABLE INPUT (PCEI)	23	Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low.
SERIAL COUNT ENABLE INPUT (SCEI)	1	Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low.
MAXIMUM COUNT OUTPUT	22	Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high.
LATCH STROBE INPUT	21	When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently.
LATCH OUTPUTS (QA, QB, QC, QD)	17, 18, 19, 20	The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: QA = 1, QB = 2, QC = 4, QD = 8.
DECIMAL POINT INPUT	7	Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked.
BLANKING INPUT (BI)	5	When high, will blank (turn off) the entire display and force $\overline{RBO}$ low. Must be low for normal display. May be pulsed to implement intensity control of the display.
RIPPLE-BLANKING INPUT (RBI)	4	When the data in the latches is BCD 0, a low input will blank the entire display and force the $\overline{RBO}$ low. This input has no effect if the data in the latches is other than 0.
RIPPLE-BLANKING OUTPUT (RBO)	6	Supplies ripple blanking information for the ripple blanking input of the next decade. Provides a low if BI is high, or if RBI is low and the data in the latches in BCD 0; otherwise, this output is high. This pin has a resistive pull-up circuit suitable for performing a wire-AND function with any open-collector output. Whenever this pin is low the entire display will be blanked; therefore, this pin may be used as an active-low blanking input.
LED/LAMP DRIVER OUTPUTS (a, b, c, d, e, f, g, dp)	15, 16, 14, 9 11, 10, 13, 8	Outputs for driving seven-segment LED's or lamps and their decimal points. See segment identification and resultant displays on following page.

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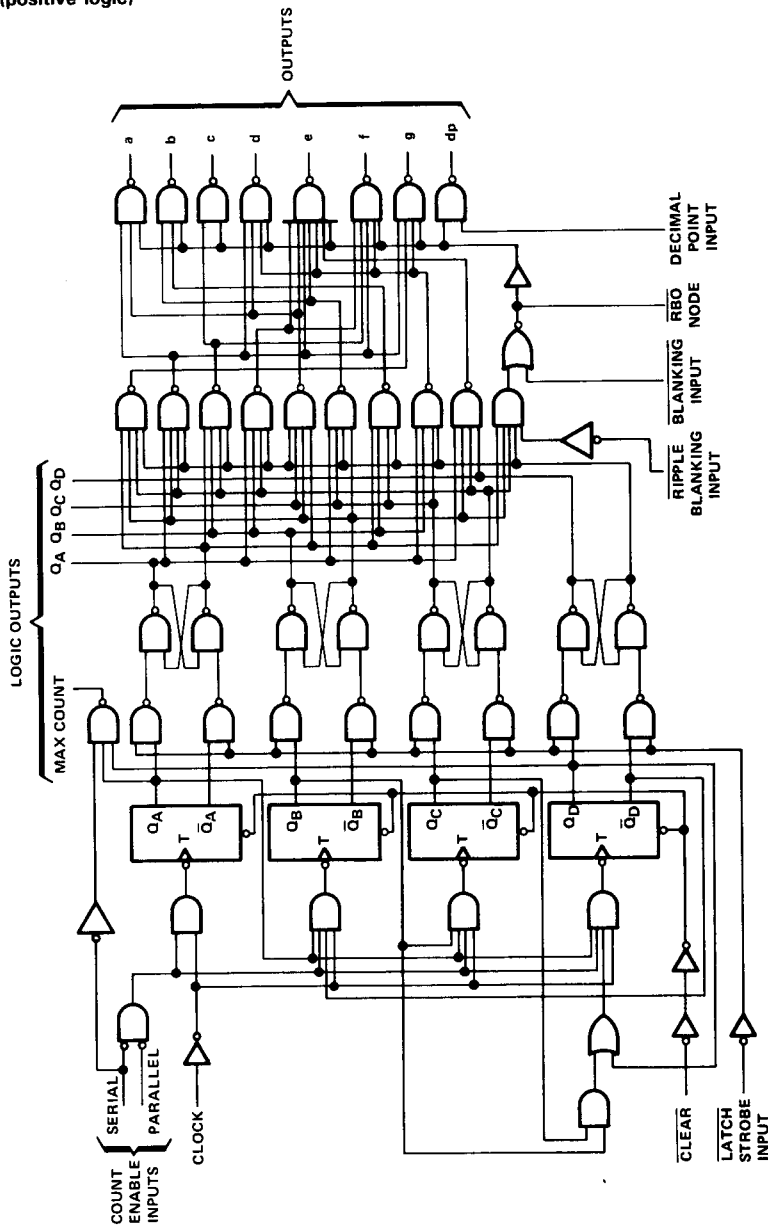


SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS—RESULTANT DISPLAYS

logic diagram (positive logic)

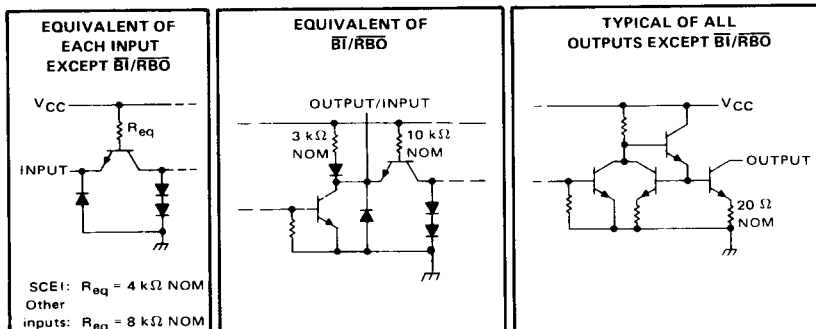


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# SN74143 4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVER

## schematics of inputs and outputs



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## TTL Devices

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Off-state current at outputs "a" thru "g" and "dp"	250 $\mu\text{A}$
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 2)	1.4 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
On-state voltage at outputs a thru g and dp ('143 only)	1		5	V
High-level output current, $I_{OH}$	$Q_A, Q_B, Q_C, Q_D$		-240	$\mu\text{A}$
	Maximum count		-560	
	$\overline{RBO}$		-120	
Low-level output current, $I_{OL}$	$Q_A, Q_B, Q_C, Q_D, \overline{RBO}$		4.8	mA
	Maximum count		11.2	
Clock pulse width, $t_w(\text{clock})$	High logic level	25		ns
	Low logic level	55		
Clear pulse width, $t_w(\text{clear})$		25		ns
Setup time, $t_{su}$	Serial and parallel carry	30 <sup>†</sup>		ns
	Clear inactive state	60 <sup>†</sup>		
Operating free-air temperature, $T_A$	0		70	°C

<sup>†</sup> The arrow indicates that the rising edge of the clock pulse is used for reference.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT	
V <sub>IH</sub>	High-level input voltage		2			V	
V <sub>IL</sub>	Low-level input voltage				0.8	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5	V	
V <sub>OH</sub>	High-level output voltage	R $\bar{B}\bar{O}$	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX	2.4		V	
		Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>					
		Maximum count					
V <sub>OL</sub>	Low-level output voltage	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , R $\bar{B}\bar{O}$	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = MAX		0.4	V	
		Maximum count					
V <sub>O(off)</sub>	Off-state output voltage	Outputs a thru g, dp	V <sub>CC</sub> = MAX, I <sub>OH</sub> = 250 $\mu$ A	7		V	
V <sub>O(on)</sub>	On-state output voltage	Outputs a thru g, dp	V <sub>CC</sub> = MIN			V	
I <sub>O(on)</sub>	On-state output current	Outputs a thru g	V <sub>CC</sub> = MIN, V <sub>O</sub> = 1 V	9	15	mA	
			V <sub>CC</sub> = 5 V, V <sub>O</sub> = 2 V		15		
			V <sub>CC</sub> = MAX, V <sub>O</sub> = 5 V		15		22
		Output dp	V <sub>CC</sub> = MIN, V <sub>O</sub> = 1 V	4.5	7		
			V <sub>CC</sub> = 5 V, V <sub>O</sub> = 2 V		7		
			V <sub>CC</sub> = MAX, V <sub>O</sub> = 5 V		7		12
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1	mA	
I <sub>IH</sub>	High-level input current	Serial carry *	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			40	$\mu$ A
		R $\bar{B}\bar{O}$ node		-0.12	-0.5		mA
		Other inputs				20	$\mu$ A
I <sub>IL</sub>	Low-level input current	Serial carry	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V, See Note 3			-1.6	mA
		R $\bar{B}\bar{O}$ node		-1.5	-2.4		
		Other inputs				-0.8	
I <sub>OS</sub>	Short-circuit output current	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>	V <sub>CC</sub> = MAX	-9	-27.5	mA	
		Maximum count		-15	-55		
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 4		56	93	mA	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTES: 3. I<sub>IL</sub> at R $\bar{B}\bar{O}$  node is tested with  $\bar{B}\bar{I}$  grounded and R $\bar{B}\bar{I}$  at 4.5 V.

4. I<sub>CC</sub> is measured after the following conditions are established:

- Strobe = R $\bar{B}\bar{I}$  = DP = 4.5 V
- Parallel count enable = serial count enable =  $\bar{B}\bar{I}$  = GND
- Clear ( ) then clock until all outputs are on ( )
- Outputs "a" through "g" and "dp" at 2.5 V, all other outputs open.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>				12	18		MHz
t <sub>PLH</sub>	Serial look-ahead	Maximum count	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 560 $\Omega$ , See Note 5		12	20	ns
t <sub>PHL</sub>					23	35	
t <sub>PLH</sub>	Clock	Maximum count			26	40	ns
t <sub>PHL</sub>					29	45	
t <sub>PLH</sub>	Clock	Q <sub>A</sub> , Q <sub>B</sub> , Q <sub>C</sub> , Q <sub>D</sub>	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1.2 k $\Omega$ ,		28	45	ns
t <sub>PHL</sub>							

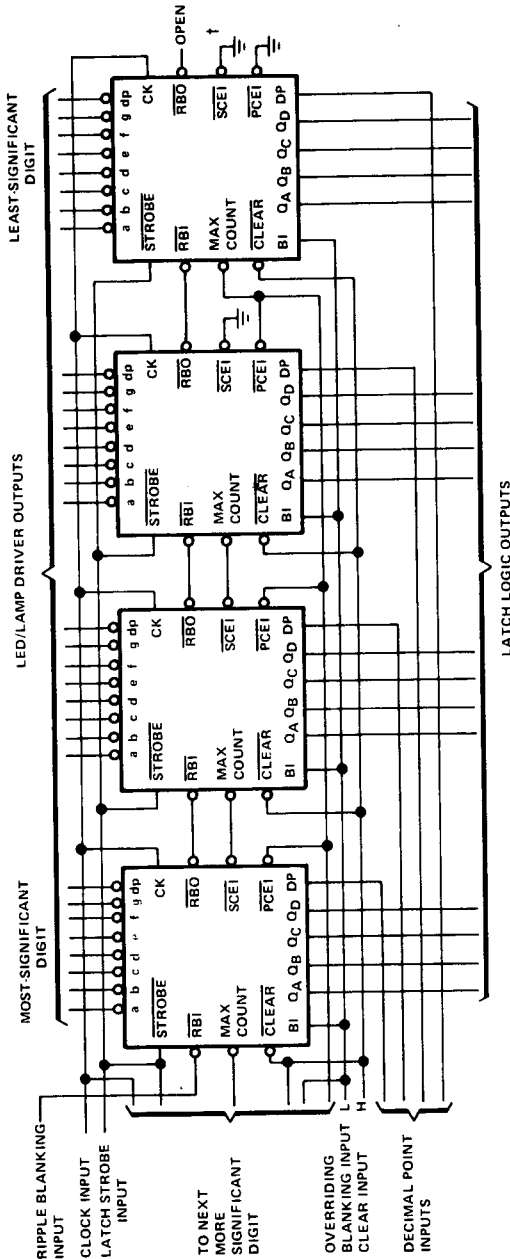
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TYPICAL APPLICATION DATA

This application demonstrates how the drivers may be cascaded for N-bit display applications. It features:

- Synchronous, look-ahead counting
- Ripple blanking of leading zeros; blanking of trailing zeros (not illustrated) can also be implemented
- Overriding blanking for total suppression or intensity modulation of display
- Direct parallel clear
- Latch strobe permits counter to acquire next display while viewing current display



† The serial count-enable input of the least-significant digit is normally grounded; however, it may be used as a count-enable control for the entire counter (high to disable, low to count) provided the logic level on this pin is not changed while the clock line is low or false counting may result.

