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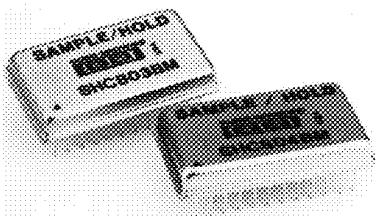


SHC803BM, CM
SHC804BM, CM

High Speed
SAMPLE/HOLD AMPLIFIER

FEATURES

- **350ns max ACQUISITION TIME**
- **±0.01% THROUGHPUT NONLINEARITY**
- **150ns max SAMPLE-TO-HOLD SETTLING TIME**
- **INPUT BUFFER (SHC803)**
- **24-PIN HERMETICALLY-SEALED METAL PACKAGE**

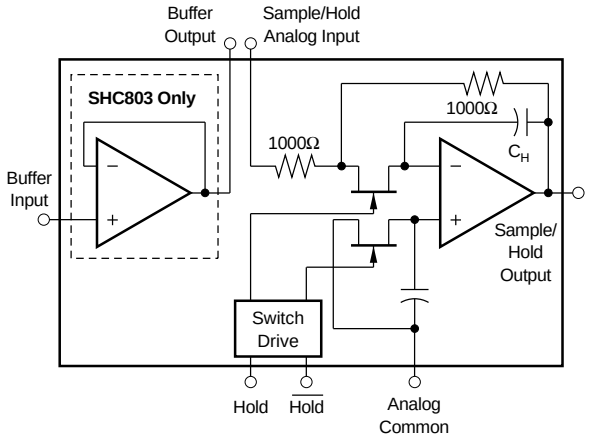
DESCRIPTION

The SHC803 and SHC804 are high speed sample/hold amplifiers designed for use in fast 12-bit data acquisition systems and signal processing systems. The SHC803 contains a fast-settling unity-gain amplifier for buffering high impedance sources or for use with CMOS multiplexers.

The SHC804 acquires a 10V signal change in less than 350ns to ±1/2LSB at 12 bits. Throughput nonlinearity error is guaranteed to be within ±1/2LSB for 12-bit systems. Stability over temperature is excellent, with only ±5ppm/°C of gain drift and ±4ppm of FSR/°C of charge offset drift over the –25 to +85°C temperature range.

The ±25ps maximum aperture uncertainty of SHC803 and SHC804 permits sampling (to ±0.01% of Full Scale Range) of signals with rates of change of up to 100V/µs. These sample/holds have been optimized for use with Burr-Brown's high speed 12-bit analog-to-digital converter, model ADC803. Together these components are capable of accurately digitizing fast changing signals at sample rates as high as 500k samples per second.

The digital inputs (HOLD and $\overline{\text{HOLD}}$) are TTL-compatible. Power supply requirements are ±15V and +5V and the specification temperature range is –25°C to +85°C. The SHC803 and SHC804 are packaged in a 24-pin dual-in-line hermetic metal package. SHC804 is pin-compatible with other sample/holds on the market with similar performance characteristics.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

PARAMETER	SHC803/SHC804BM MIN	SHC803/SHC804BM TYP	SHC803/SHC804BM MAX	SHC803/SHC804CM MIN	SHC803/SHC804CM TYP	SHC803/SHC804CM MAX	UNITS
SAMPLE/HOLD INPUTS (without Input Buffer)							
ANALOG							
Voltage Range	±10.25	±11		*	*		V
R_{IN}		1.00			*		kΩ
DIGITAL (HOLD, $\overline{HOLD}$)							
V_{IH}	+2.0			*			V
V_{IL}			+0.8			*	V
I_{IH}, V_{IN} = +2.7V			+60			*	µA
I_{IL}, V_{IN} = +0.4V			–1.2			*	mA
SAMPLE/HOLD TRANSFER CHARACTERISTICS (without Input Buffer)							
ACCURACY							
Sample Mode							
Gain		–1			*		V/V
Gain Error			±0.1			*	%
Temperature Coefficient		±3	±10		±1	±5	ppm/°C
Linearity Error		±0.001	±0.005		*	*	% of FSR[1]
Zero Offset		±1	±5		±0.5	±3	mV
Temperature Coefficient		±1	±2.5		±0.5	±1.5	ppm of FSR/°C
Hold Mode							
Charge Offset		±2	±10		±1	±5	mV
Temperature Coefficient		±3	±10		±2	±4	ppm of FSR/°C
Droop Rate: at +25°C		±0.5	±5		*	*	µV/µs
+85°C			±0.5			±0.1	mV/µs
Throughput Nonlinearity			±0.01			*	% of FSR
Power Supply Sensitivity[2]: ±V_{CC}			±0.002			*	% of FSR/%V_{CC}
V_{DD}			±0.003			*	% of FSR/%V_{DD}
DYNAMIC CHARACTERISTICS							
Acquisition Time (with 10V Step)							
to within: ±0.1% (±10mV)		220			*		ns
±0.01% (±1mV)		250	350		*	*	ns
Sample-to-Hold Settling Time							
to within ±0.01% (±1mV)		100	150		*	*	ns
Sample-to-Hold Transient Amplitude		60	150		*	*	mV_{PEAK}
Aperture Delay TIme[3]		15	25		*	*	ns
Aperture Uncertainty		±10	±25		*	*	ps
Sample Mode: Output Slew Rate		160			*		V/µs
Full Power Bandwidth		1			*		MHz
Small Signal Bandwidth		16			*		MHz
Hold Mode Feedthrough Rejection							
(10V Square Wave Input)	±0.03	±0.005			*		%
SAMPLE/HOLD OUTPUT							
Voltage Range	±10.25	±11		*	*		V
Output Current	±50			*			mA
Short Circuit Protection		Indefinite to Common			*		
Output Impedance (at DC)		0.01	0.1		*	*	Ω
INPUT BUFFER CHARACTERISTICS (SHC803 only)							
INPUT							
Offset Voltage		±1/2	±5		*	*	mV
vs Temperature		±1.5	±2.5		*	*	ppm of FSR/°C
Bias Current			±25			*	nA
Impedance		10^8 || 5			*		Ω || pF
V_{IN} Range	±10.25	±11		*	*		V
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth		320			*		kHz
Slew Rate[4]		10			*		V/µs
Settling Time[4] to ±2mV for 10V Step		2.5			*		µs
OUTPUT							
V_{OUT} Range	±10.25			*			V
Output Current	±10.25			*			mA

SPECIFICATIONS (CONT)

ELECTRICAL

At +25°C, rated power supplies and a 1kΩ output load, unless otherwise specified.

PARAMETER	SHC803/SHC804BM			SHC803/SHC804CM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Rated Voltage: $\pm V_{CC}$	±13.5	±15	±16.5	*	*	*	V
V_{DD}	+4.75	+5.00	+5.25	*	*	*	V
Quiescent Current (No Load)							
SHC804: $+V_{CC}$		30	35		*	*	mA
$-V_{CC}$		15	20		*	*	mA
V_{DD}		5	10		*	*	mA
SHC803: $+V_{CC}$		33	40		*	*	mA
$-V_{CC}$		18	25		*	*	mA
V_{DD}		5	10		*	*	mA
Power Dissipation: SHC804		700	875		*	*	mW
SHC803		790	1100		*	*	mW
TEMPERATURE RANGE							
Specification	–25		+85	*		*	°C
Storage	–55		+125	*		*	°C

* Specification same as SHC803/SHC804BM.

NOTES: (1) FSR means Full Scale Range and is 20V for SHC803 and SHC804. (2) Sensitivity of offset plus charge offset. (3) With respect to HOLD. For $\overline{HOLD}$ add 5ns typical. (4) With buffer connected to the sample/hold amplifier.

ABSOLUTE MAXIMUM RATINGS

Input Overvoltage ..... ±15V
$+V_{CC}$ to V_{CC} COMMON ..... 0 to +18V
$-V_{CC}$ to V_{CC} COMMON ..... 0 to –18V
Voltage on Digital Inputs (pins 11 and 12) ..... –0.5V to +7V
Power Dissipation 1500mW
V_{DD} to DCOM ..... –0.5V
Analog Output ..... Indefinite Short to V_{CC} COM

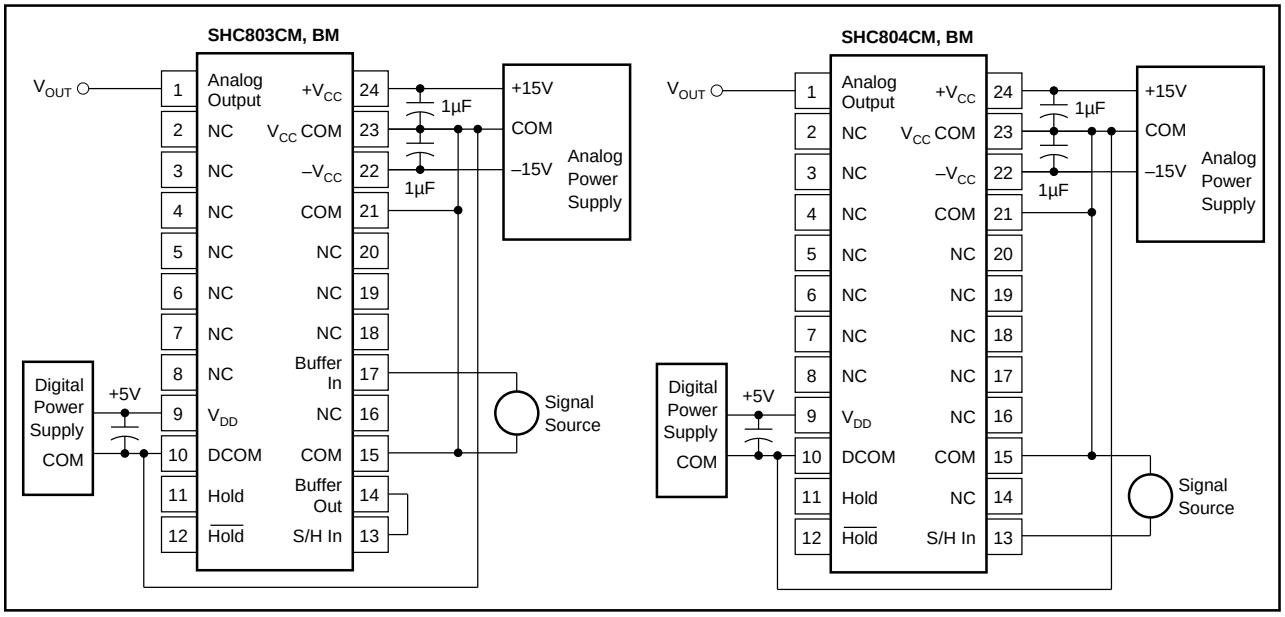
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliablility.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
SCH803/804CM, BM	24-Pin Metal	113
SCH803/804BM	24-Pin Metal	113

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

CONNECTION DIAGRAMS



PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	Sample/Hold Output	Analog voltage output
2	NC	Not connected
3	NC	Not connected
4	NC	Not connected
5	NC	Not connected
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V_{DD}	Logic supply
10	DCOM	Logic supply common
11	HOLD	Logic "1" = HOLD
12	$\overline{HOLD}$	Logic "0" = HOLD
13	S/H In	SHC804 input; for SHC803 connect pin 13 to pin14
14	Buffer Out, SHC803 only	Not connected for SHC804
15	COM	Signal common
16	NC	Not connected
17	Buffer In, SHC803 only	Not connected for SHC804
18	NC	Not connected
19	NC	Not connected
20	NC	Not connected
21	COM	Signal common
22	$-V_{CC}$	–15V supply
23	V_{CC} COM	Analog to power common, connected to case
24	$+V_{CC}$	+15V supply

DISCUSSION OF SPECIFICATIONS

Throughput Nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by Offset and Gain adjustments.

Gain Error is the difference between the input and output voltage magnitude (in the Sample mode) due to the amplifier gain errors.

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor and FET switch leakage current and the input bias current of the output amplifier.

Feedthrough is the amount of output voltage change caused by an input voltage change when the sample/hold is in the Hold mode.

Aperture Delay Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the Hold mode control transition to the time at which the output stops tracking the input.

Aperture Uncertainty Time is the nonrepeatibility of aperture delay time.

Acquisition Time is the time required for the sample/hold output to settle to within a given error band of its final value when the sample/hold is switched from Hold to Sample.

Charge Offset (Pedestal) is the output voltage change that results from charge coupled into the Hold capacitor through the gate capacitance of the switching field effect transistor. This charge appears as an offset at the output.

Sample-to-Hold Switching Transient is the switching transient which appears on the output when the sample/hold is switched from Sample to Hold. Both the magnitude and the settling time of the transient are specified.

OPERATION

A simplified circuit diagram of SHC803/804 is shown on page 1. The SHC803 includes a noninverting unity-gain op amp to serve as a source-impedance buffer when the sample/hold is used with CMOS analog multiplexers. The SHC804 and SHC803 are identical except for this buffer.

In the Sample (track) mode the circuit acts as a unity-gain inverting amplifier. In the Hold mode, the capacitor, C_H, holds the value of the output at the time the unit was switched to the Hold mode. Additional circuits compensate for switching transients and provide switch leakage current

cancellation. The amplifier provides high current drive and low output impedance to external loads.

GAIN, OFFSET, CHARGE OFFSET

SCH803 and SCH804 have been internally-trimmed to eliminate the need for external trim potentiometers for Gain, Offset (in Sample mode) and Charge Offset (Pedestal). System Gain and Offset errors can be adjusted elsewhere in the system, at an input amplifier preceding the sample/hold, or at an analog-to-digital converter following the sample/hold.

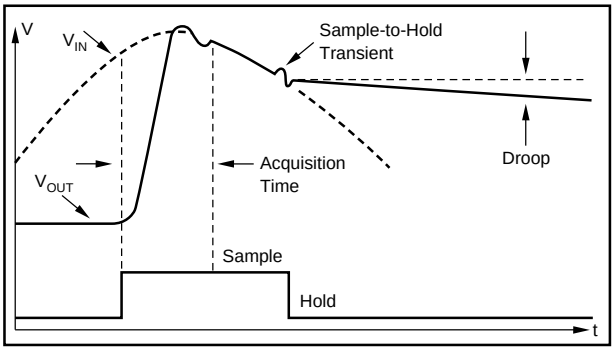


FIGURE 1. Definition of Acquisition Time, Droop and Sample-to-Hold Transient.

INSTALLATION

GROUNDING AND BYPASSING

SHC803 and SHC804 have four COMMON pins (pins 10, 15, 21 and 23) and all must be tied together and connected to the system analog common (V_{CC} COM) as close to the package as possible. It is preferable to have a large ground plane surrounding the sample/hold and have all four common pins soldered directly to it. Note that the metal case is internally connected to pin 23; therefore, care must be taken to avoid a ground loop if the case is allowed to contact the ground plane.

Most digital return currents pass through pin 10. Noise from the switch-drive circuit may couple directly into the main op amp summing junction, a very noise-sensitive node. Care must be taken to insure that no voltage differences occur between pin 10 and the other common pins. This is the reason pin 10 must be connected directly to the ground plane.

For the same reason, the logic supply should be kept as free of noise as possible. $\pm V_{CC}$ supply lines (pins 24 and 22) are internally bypassed to common with 0.01µF capacitors. It is recommended that the user install additional external 0.1µF to 1µF tantalum bypass capacitors at each supply pin.

SAMPLE/HOLD CONTROL

A TTL logic "0" at pin 11 (or a logic "1" at pin 12) switches the SHC803/804 into the Sample (track) mode. In this mode, the device acts as a unity-gain inverting amplifier, the output following the inverse of the input. A logic "1" at pin 11 (or a logic "0" at pin 12) will switch the SHC803/804 into the Hold mode. The output voltages will be held constant at the value present when the Hold command is given.

If pin 11 is used, pin 12 must be connected to the DCOM (pin 10). If pin 12 is used, pin 11 must be tied to V_{DD}. Using the HOLD and $\overline{\text{HOLD}}$ inputs as logic function may adversely affect the charge offset (pedestal). A clean digital signal (no overshoot) at the HOLD of $\overline{\text{HOLD}}$ inputs will also reduce charge offset errors. Pins 11 and 12 present less than one standard TTL load (two LSTTL loads) to the digital drive circuit.

OUTPUT LOADING

Care must be taken when loading the output of the SHC803/804 to avoid possible oscillations, current limiting and performance variations over temperature.

The maximum capacitive load to avoid oscillations is about 300pF. Recommended resistive load is 500Ω or more, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω in parallel with capacitive loads up to 100pF. Higher capacitances will affect acquisition and settling times.

ANALOG SIGNAL SOURCE CONSIDERATIONS

The output impedance of the signal source driving the SHC804 will affect the accuracy of the sample and hold operation both statically (at DC) and dynamically. The output impedance of the signal source should be low and remain low over a wide bandwidth. A small capacitor at the driving source may help to improve the charge offset errors that are affected by dynamic source impedance.

SHC803 BUFFER AMPLIFIER

The buffer amplifier incorporated in the SHC803 provides appropriate drive characteristics to the sample/hold amplifier. Again a 20pF to 50pF capacitor added to the output of the buffer amplifier may improve charge offset performance.

The buffer amplifier is optimized for fast settling with 10Vp-p signals. However, for step input signals greater than 10V, a protection network (Figure 2) is required to prevent the buffer from overload, resulting in excessive settling time.

The data sheet for the Burr-Brown model ADC803 analog-to-digital converter contains a sample printed circuit board layout incorporating many of the above considerations.

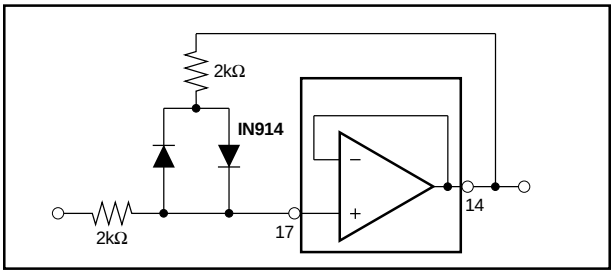


FIGURE 2. SHC803 Buffer Amplifier Protection For Input Steps Greater Than 10V.

APPLICATIONS

SIGNAL DIGITIZATION

Sample/hold amplifiers are commonly used to hold input voltages to an A/D converter constant during conversion. Digitizing errors result if the analog signal being digitized varies excessively during conversion.

For example, the Burr-Brown ADC803 is a 12-bit successive-approximation converter with a 1.5µs conversion time. To insure the accuracy of the output data, the analog input signal to the A/D converter must not change more than 1/2LSB during the conversion.

The maximum rate of change for sine wave inputs is dv/dt (max) = $2\pi Af$ (V/s). If one allows a 1/2LSB change (2.44mV) for a ±10V input swing to the A/D converter, the allowable input rate-of-change limit would be 2.44mV/1.5µs = 1.63mV/µs. Thus the sampled sinusoidal signal frequency limit is

$$f = (1.63 \times 10^3)/2\pi A = 259/A(Hz)$$

where A is the amplitude of the sine wave. For a ±10V sine wave this corresponds to a frequency of 26Hz.

A sample/hold in front of the A/D converter "freezes" the converter's input signal whenever it is necessary to make a conversion. The rate-of-change limitation calculated above no longer exists. If a sample/hold has acquired an input signal and is tracking it, the sample/hold can be commanded to hold at any instant. There is a short delay between the time the hold command is asserted and the time the circuit actually holds. This delay is called aperture delay. The hold command signal can usually be advanced in time to cause the amplifier to hold when one wants it to hold.

The uncertainty in aperture delay, called aperture jitter, is a key consideration. For the SHC803/804 there is a 25ps maximum period during which the input signal should not change, for example, more than 1/2LSB for 12-bit systems. For a ±10V input range (1/2LSB = 2.44mV), the input signal rate of change limitation is 2.44mV/25ps = 97.6V/µs. The equivalent input sine wave frequency is

$$f = 97.6 \times 10^6/2\pi A = 15.5/A(MHz),$$

60,000 times higher than using the A/D alone.

However, there are other considerations. The resampling rate of an ADC803 is 1.5µs (A/D conversion time) + 0.3µs (sample/hold acquisition time) = 1.8µs. If one samples a sine wave at the Nyquist rate this permits sampling a frequency of 278kHz. The above analysis assumed that the droop rate of the sample/hold is negligible—less than 1/2LSB during the conversion time—and that the large signal bandwidth response of the sample/hold causes negligible waveform distortion.

USING THE SHC804 WITH THE ADC803

ADC803 is a 1.5µs, 12-bit successive approximation A/D converter. Its input circuitry has been designed to minimize high frequency current transients that appear at the input of successive approximation A/D converters. The SHC803 and SHC804 have been designed with a fast-settling, low output-impedance amplifier to further minimize the effects of high frequency transient currents present in an output load.

A typical SHC804/ADC803 connection for high-speed digitization is illustrated in Figure 3. A short delay must occur before the A/D start command is asserted since the ADC803 makes its first conversion decision 100ns after the start command is asserted. Because the SHC804 sample-to-hold settling time is 150ns (maximum) the additional delay required is about 50ns. This can be achieved using a one-shot or by using the delay provided by the six inverters of a hex inverter integrated circuit. This combination can be triggered at rates of over 500k samples per second.

Using the input buffer of the SHC803 provides a high input impedance sample/hold for CMOS analog multiplexers such as the high speed Burr-Brown MPC800. The high input impedance of the SHC803 buffer minimizes DC errors caused by the ON resistance of the multiplexer switches and/or relatively high impedance signal sources (Figure 4). The multiplexer can be switched to a new channel as soon as the SHC803 is switched to the Hold mode. The multiplexer/buffer combination settles to the new input value during the sample/hold acquisition time and A/D conversion time. This "overlap" technique results in little or no loss in throughput rate.

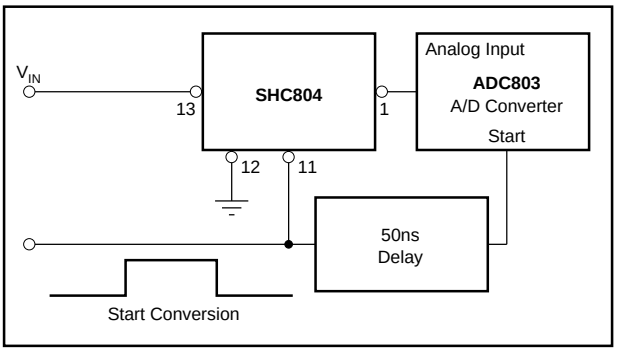


FIGURE 3. SHC804 and ADC803 Provide Sampling Rates Over 500k Samples Per Second.

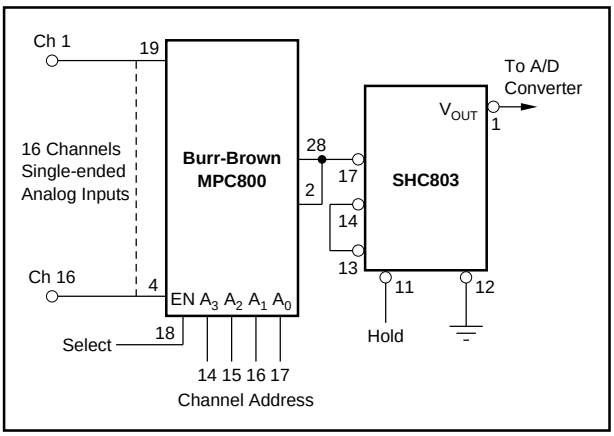
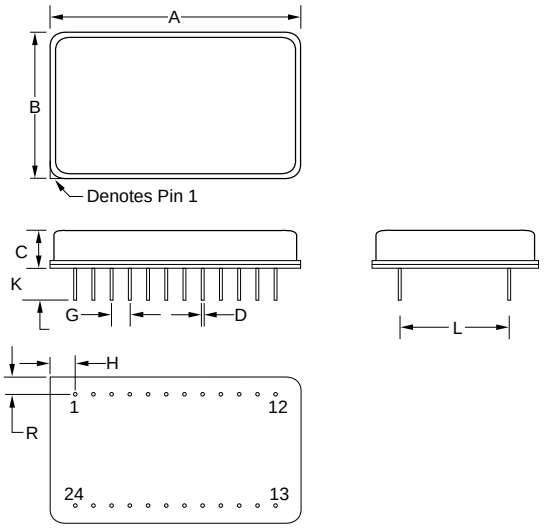


FIGURE 4. Using SHC803 With The MPC800 Analog Multiplexer.

PACKAGE DRAWING

Package Drawing Number 113 — 24-Pin Metal



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.365	1.385	34.67	35.18
B	.790	.810	20.07	20.57
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.125	.150	3.18	3.81
K	.150	.300	3.81	7.62
L	.600 BASIC		15.24 BASIC	
R	.080	.110	2.03	2.79

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.
Pin numbers shown for reference only.