BURR - BROWN®

SHC615

Wide-Bandwidth, DC RESTORATION CIRCUIT

FEATURES

- PROPAGATION DELAY: 2.2ns
- BANDWIDTH: OTA: 750MHz
  Comparator: 280MHz
- LOW INPUT BIAS CURRENT: –0.3μA
- SAMPLE/HOLD SWITCHING TRANSIENTS: +1/–7mV
- SAMPLE/HOLD FEEDTHROUGH REJECTION: 100dB
- CHARGE INJECTION: 40fC
- HOLD COMMAND DELAY TIME: 3.8ns
- TTL/CMOS HOLD CONTROL

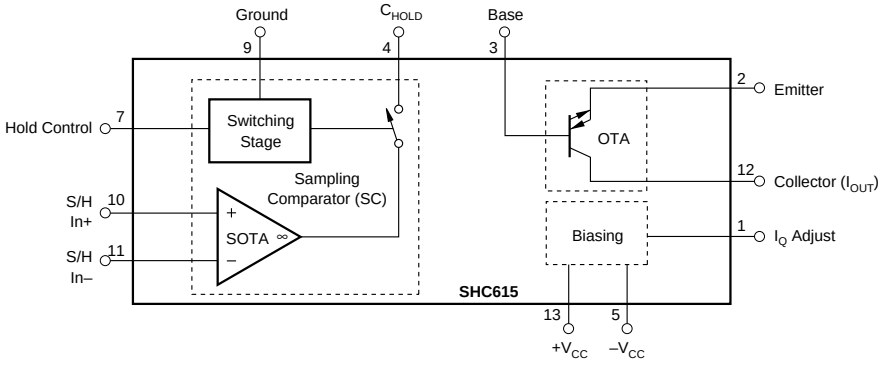
APPLICATIONS

- BROADCAST/HDTV EQUIPMENT
- TELECOMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- CAD MONITORS/CCD IMAGE PROCESSING
- NANO SECOND PULSE INTEGRATOR/ PEAK DETECTORS
- PULSE CODE MODULATOR/ DEMODULATOR
- COMPLETE VIDEO DC LEVEL RESTORATION
- SAMPLE/HOLD AMPLIFIER

DESCRIPTION

The SHC615 is a complete subsystem for very fast and precise DC restoration, offset clamping, and low frequency hum suppression of wideband amplifiers or buffers. Designed to stabilize the performance of video signals, it can also be used as a sample/hold amplifier, high-speed integrator, or peak detector for nanosecond pulses. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and fast sampling comparator set a new standard for high-speed applications. Both can be used as stand-alone circuits or combined to form a more complex signal processing stage. The self-biased, bipolar OTA can be viewed as an ideal voltage-controlled current source and is optimized for low input bias current. The sampling comparator has two identical high-impedance inputs and a current source output optimized for low output bias current and offset voltage; it can be controlled by a TTL-compatible switching stage within a few nanoseconds. The transconductance of the OTA and sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

The SHC615 is available in SO-14 surface mount and 14-pin plastic DIPs, and is specified over the extended temperature range of –40°C to +85°C.



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DC SPECIFICATIONS

At V_{CC} = ±5V, R_{LOAD} = 100Ω, R_Q = 300Ω, R_{IN} = 150Ω and T_A = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU MIN	SHC615AP, AU TYP	SHC615AP, AU MAX	UNITS
OFFSET VOLTAGE, V_E at V_B = 0					
Initial			8	±40	mV
vs Temperature			40		µV/°C
vs Supply (tracking)	V_{CC} = ±4.5V to ±5.5V	50	55		dB
B-INPUT BIAS CURRENT					
Initial			–0.3	±0.9	µA
vs Temperature			1		nA/°C
C-OUTPUT BIAS CURRENT, I_C at V_B = 0					
Initial		–200	–77	+100	µA
B-INPUT IMPEDANCE			4.4		MΩ
INPUT NOISE					
Voltage Noise Density, B-to-E	f_{OUT} = 100kHz to 100MHz		2.2		$nV/\sqrt{Hz}$
Voltage Noise Density, B-to-C	f_{OUT} = 100kHz to 100MHz		4.5		$nV/\sqrt{Hz}$
INPUT VOLTAGE RANGE			±3.4		V
OUTPUT					
Output Voltage Compliance			±3.2		V
C-Current Output		±18	±20		mA
E-Current Output		±18	±20		mA
C-Output Impedance			0.5		MΩ
E-Output Impedance			12		Ω
Open-Loop Gain			96		dB
TRANSCONDUCTANCE	Small Signal, <200mV		70		mA/V

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

DC SPECIFICATIONS (CONT)

At V_{CC} = ±5V, R_{LOAD} = 1kΩ, R_Q = 300Ω, and T_A = +25°C, unless otherwise specified.

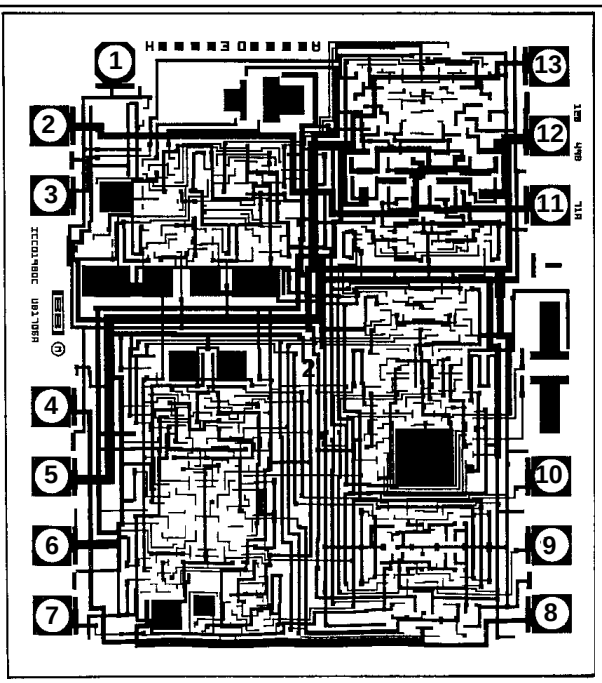
PARAMETER	CONDITIONS	SHC615AP, AU			UNITS
		MIN	TYP	MAX	
COMPARATOR					
INPUT BIAS CURRENT					
Initial			1.0	±5	µA
vs Temperature			–2.3		nA/°C
C-OUTPUT BIAS CURRENT					
Initial			±10	±50	µA
vs Temperature			±13		nA/°C
INPUT IMPEDANCE					
Input Impedance			0.2		MΩ
INPUT NOISE					
Voltage Noise Density	f_{OUT} = 100kHz to 100MHz		5		nV/√Hz
INPUT VOLTAGE RANGE					
Input Voltage Range			±3.0		V
Common-Mode Input Range			±3.2		V
OUTPUT					
Output Voltage Compliance			±3.5		V
C-Current Output		±2.5	±3.2		mA
C-Output Impedance			620 || 2		kΩ || pF
Open-Loop Gain			83		dB
TRANSCONDUCTANCE					
Transconductance			22		mA/V
HOLD CONTROL					
Logic 1 Voltage		+2		$+V_{CC}$ +0.6	V
Logic 0 Voltage		0		0.8	V
Logic 1 Current	V Hold Control = 5.0V		1		µA
Logic 0 Current	V Hold Control = 0.8V		0.05		µA
TRANSFER CHARACTERISTICS					
Charge Injection	Track-To-Hold		40		fC
Feedthrough Rejection	Hold Mode		–100		dB
COMPLETE SHC615					
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	R_Q = 300Ω	±12	±15	±18	mA
Quiescent Current Range	Programmable (Useful Range)		±3 to ±36		mA
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–40		+125	°C

AC SPECIFICATIONS

At V_{CC} = ±5V, R_{LOAD} = 100Ω, R_{SOURCE} = 50Ω, R_Q = 300Ω, and T_A = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	SHC615AP, AU MIN	SHC615AP, AU TYP	SHC615AP, AU MAX	UNITS
FREQUENCY DOMAIN					
OTA					
LARGE-SIGNAL BANDWIDTH (–3dB), (B-to-E)	V_{OUT} = 5.0Vp-p V_{OUT} = 2.8Vp-p V_{OUT} = 1.4Vp-p		430 540 620		MHz MHz MHz
SMALL-SIGNAL BANDWIDTH B-TO-E	V_{OUT} = 0.2Vp-p		520		MHz
DIFFERENTIAL GAIN (B-TO-E)	f = 4.43MHz, V_{OUT} = 0.7Vp-p, R_L = 150Ω R_L = 500Ω		 1.8 0.1		 % %
DIFFERENTIAL PHASE (B-TO-E)	f = 4.43MHz, V_{OUT} = 0.7Vp-p, R_L = 150Ω R_L = 500Ω		 0.07 0.01		 ° °
HARMONIC DISTORTION (B-TO-E) Second Harmonic Third Harmonic	f = 30MHz, V_{OUT} = 1.4Vp-p		 –50 –46		 dBc dBc
LARGE SIGNAL BANDWIDTH (–3dB), (B-to-C)	V_{OUT} = 5.0Vp-p V_{OUT} = 2.8Vp-p V_{OUT} = 1.4Vp-p		250 580 750		MHz MHz MHz
SMALL SIGNAL BANDWIDTH B-to-C	V_{OUT} = 0.2Vp-p		680		MHz
COMPARATOR	Sample Mode				
BANDWIDTH (–3dB)	I_{OUT} = 4mAp-p I_{OUT} = 2mAp-p I_{OUT} = 1mAp-p		240 270 280		MHz MHz MHz
TIME DOMAIN					
OTA					
RISE TIME	2Vp-p Step, 10% to 90% B-to-E B-to-C		 1.1 1.2		 ns ns
SLEW RATE	2Vp-p, B-to-E B-to-C 5Vp-p, B-to-E B-to-C		1800 1700 3300 3000		V/µs V/µs V/µs V/µs
COMPARATOR					
RISE TIME (Sample Mode)	10% to 90%, R_L = 50Ω, I_{OUT} = ±2mA C_{LOAD} = 1pF		2.5		ns
SLEW RATE (Sample Mode)	10% to 90%, R_L = 50Ω, I_{OUT} = ±2mA C_{LOAD} = 1pF		0.95		mA/ns
DYNAMIC CHARACTERISTICS Propagation Delay Time Propagation Delay Time Delay Time	 t_{PDH}, V_{OD} = 200mV t_{PDL}, V_{OD} = 200mV Sample-to-Hold Hold-to-Sample		 2.2 2.15 3.8 3.0		 ns ns ns ns

DICE INFORMATION



SHC615 DIE TOPOGRAPHY

DIE PAD	FUNCTION
1	I_Q Adjust
2	OTA-Emitter
3	OTA-Base
4	C_{HOLD}
5	–5V Supply, Analog
6	–5V Supply, Digital
7	Hold Control
8	Ground
9	S/H In+
10	S/H In–
11	I_{OUT}, OTA-Collector
12	+5V Supply, Analog
13	+5V Supply, Digital

Substrate Bias: Negative Supply.
Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	73 x 81, ±5	1.86 x 2.06, ±0.13
Die Thickness	14, ±1	0.55, ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, –0.0	0.0005, +0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	±6V
Input Voltage[1]	$\pm V_{CC}$ ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Hold Control	–0.5V to $+V_{CC}$ +0.7V

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

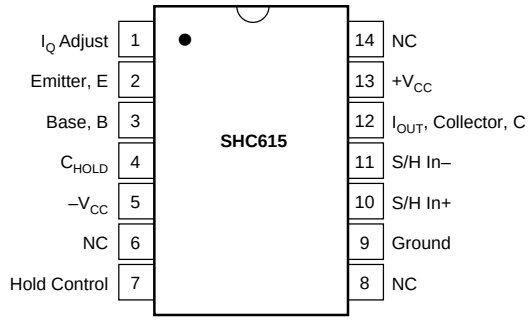
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC615AP	Plastic 14-Pin DIP	010
SHC615AU	SO 14-Pin Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATION

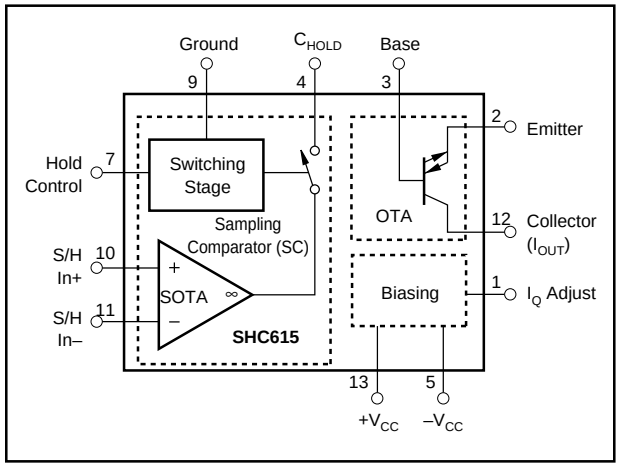
Top View **DIP SO-14**



ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE
SHC615AP	Plastic 14-Pin DIP	–40°C to +85°C
SHC615AU	SO 14-Pin Surface Mount	–40°C to +85°C

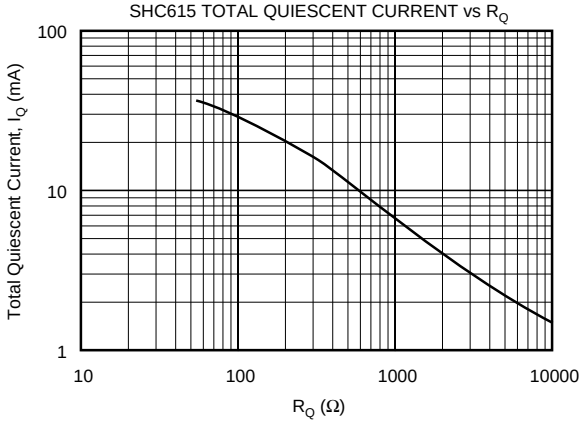
BLOCK DIAGRAM



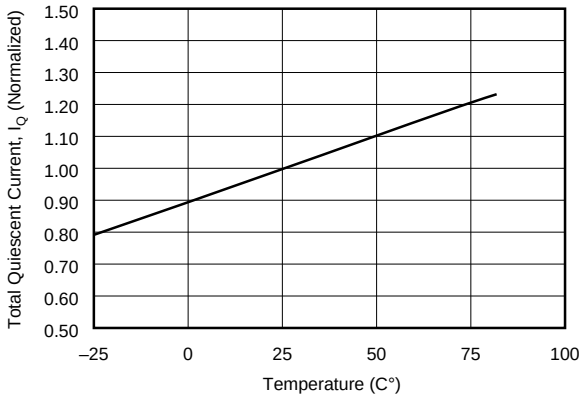
TYPICAL PERFORMANCE CURVES

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

SHC615 TOTAL QUIESCENT CURRENT vs R_Q

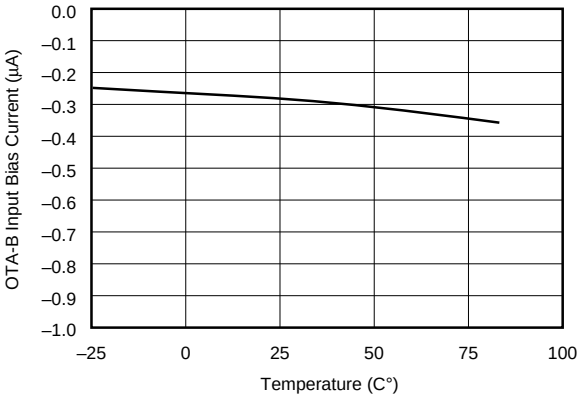


TOTAL QUIESCENT CURRENT vs TEMPERATURE

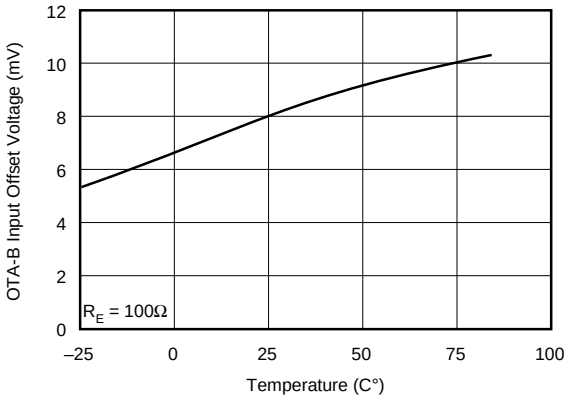


OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

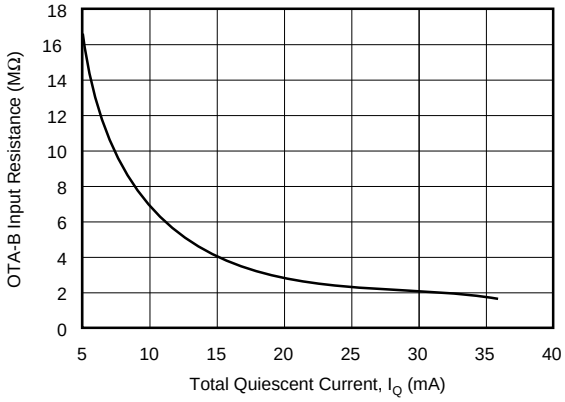
OTA B-INPUT BIAS CURRENT vs TEMPERATURE



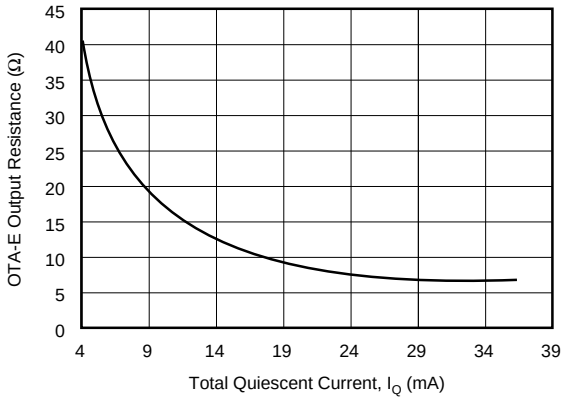
OTA-B INPUT OFFSET VOLTAGE vs TEMPERATURE



OTA-B INPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



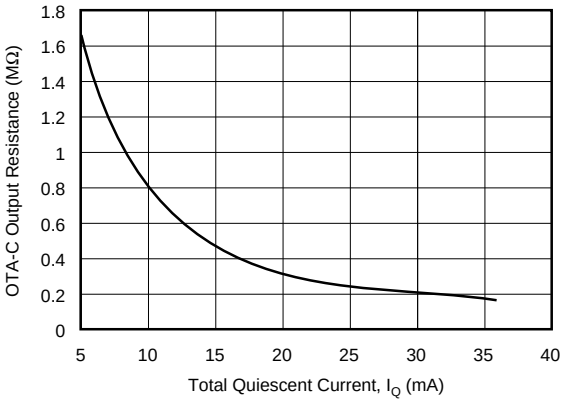
OTA-E OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



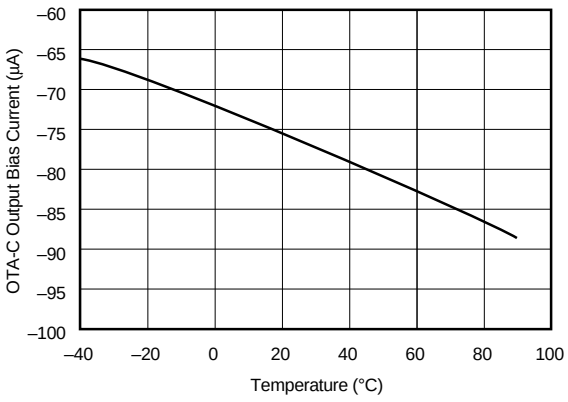
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

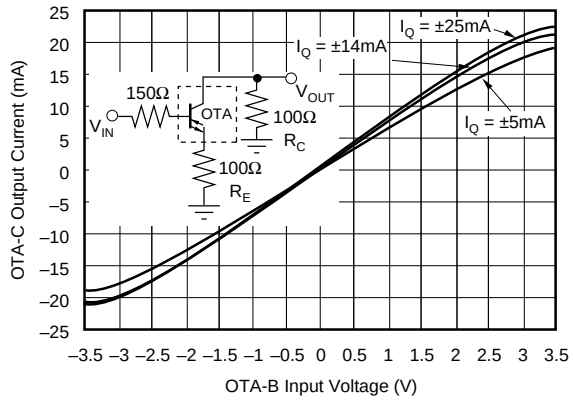
OTA-C OUTPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



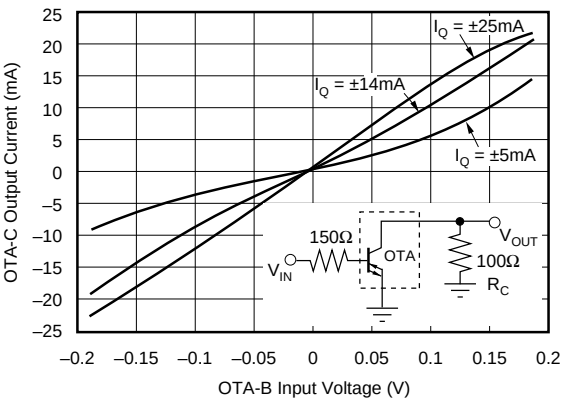
OTA-C OUTPUT BIAS CURRENT vs TEMPERATURE



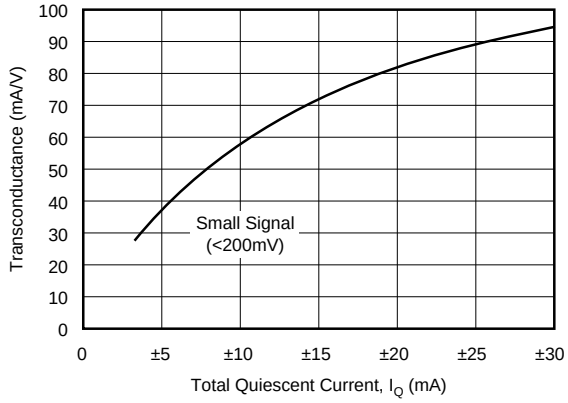
OTA TRANSFER CHARACTERISTICS vs INPUT VOLTAGE



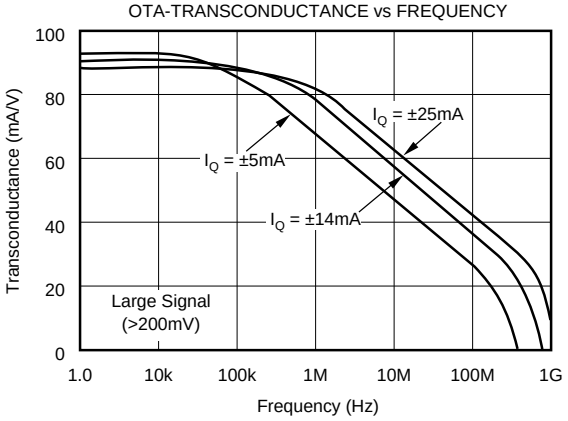
OTA TRANSFER CHARACTERISTIC vs INPUT VOLTAGE



OTA TRANSCONDUCTANCE vs TOTAL QUIESCENT CURRENT



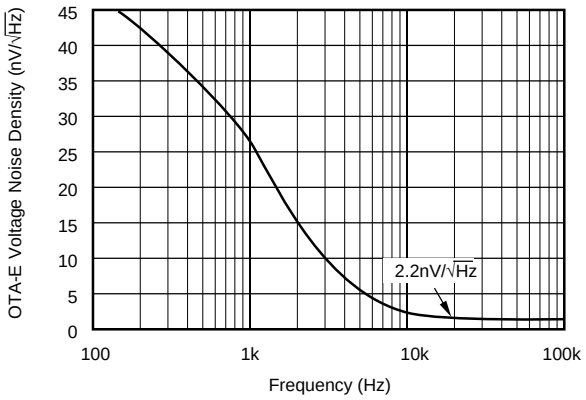
OTA-TRANSCONDUCTANCE vs FREQUENCY



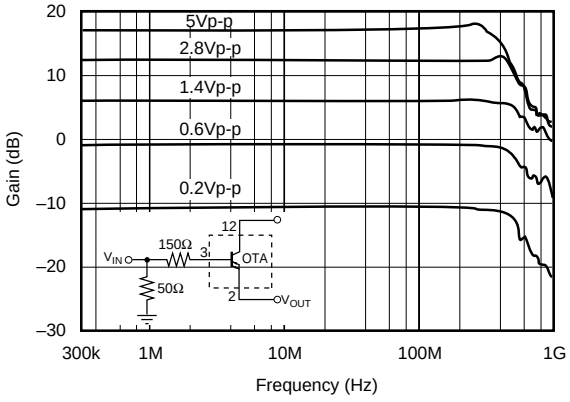
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

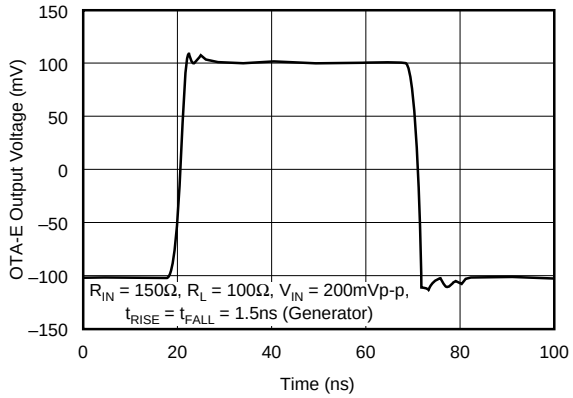
OTA-E VOLTAGE NOISE SPECTRAL DENSITY



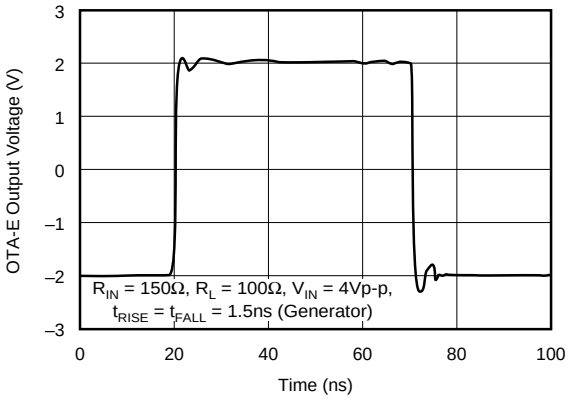
OTA-E FREQUENCY RESPONSE



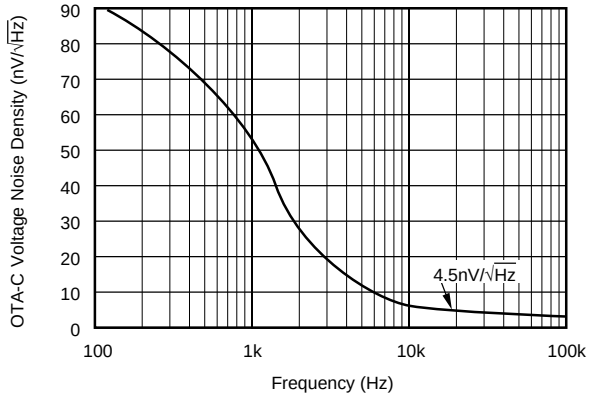
OTA-E SMALL SIGNAL PULSE RESPONSE



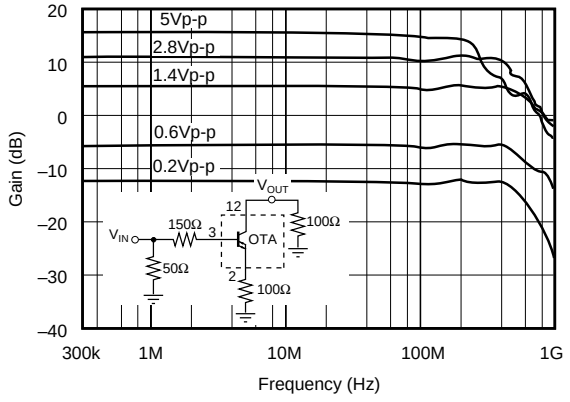
OTA-E LARGE SIGNAL PULSE RESPONSE



OTA-C VOLTAGE NOISE SPECTRAL DENSITY



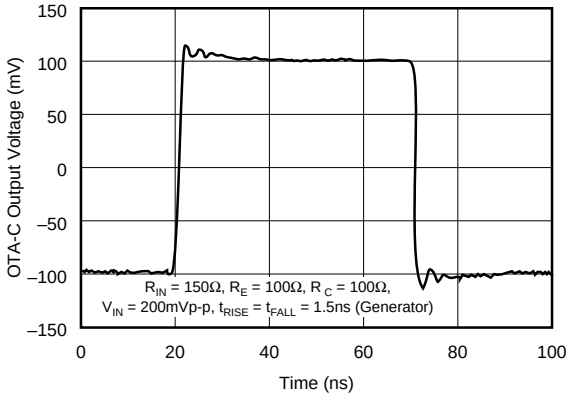
OTA-C FREQUENCY RESPONSE



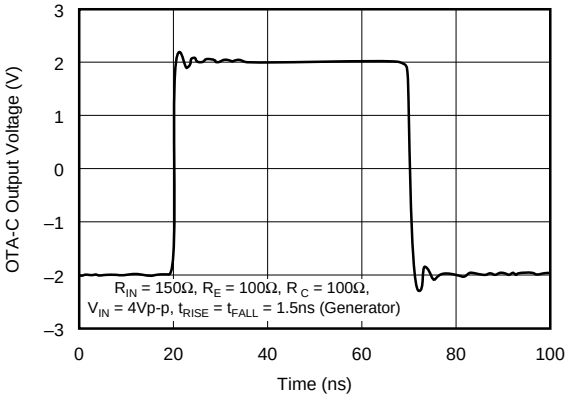
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

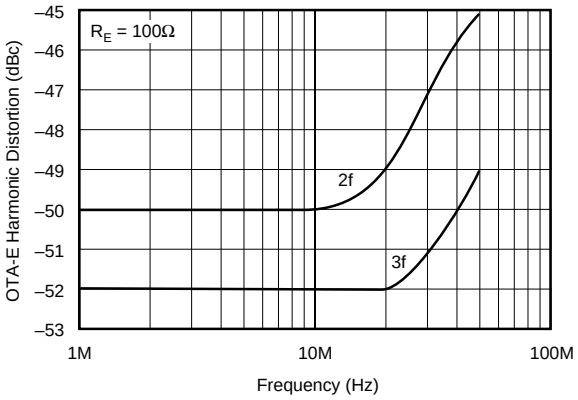
OTA-C SMALL SIGNAL PULSE RESPONSE



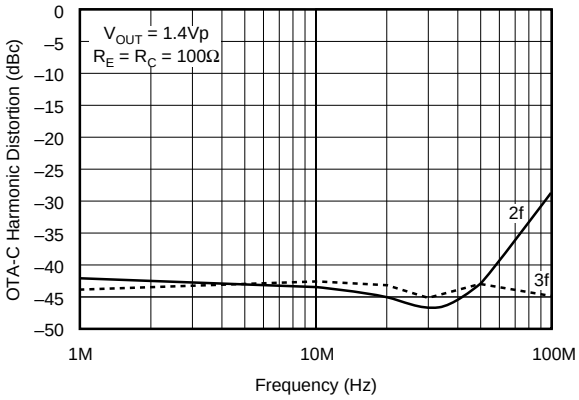
OTA-C LARGE SIGNAL PULSE RESPONSE



OTA-E HARMONIC DISTORTION vs FREQUENCY

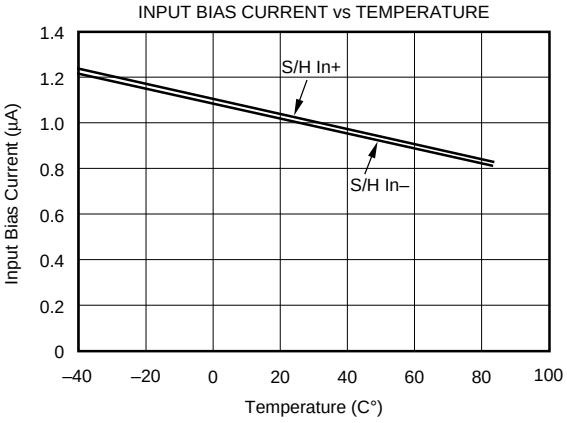


OTA-C HARMONIC DISTORTION vs FREQUENCY

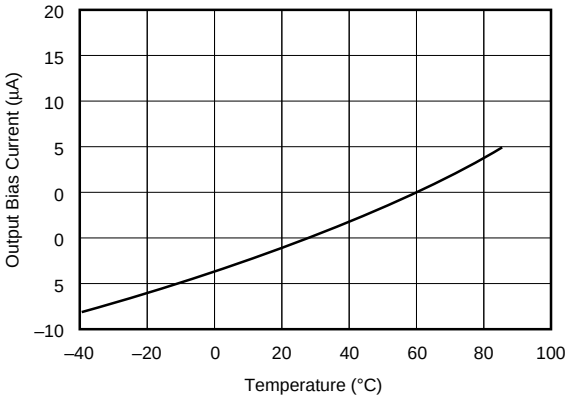


SAMPLING COMPARATOR

INPUT BIAS CURRENT vs TEMPERATURE



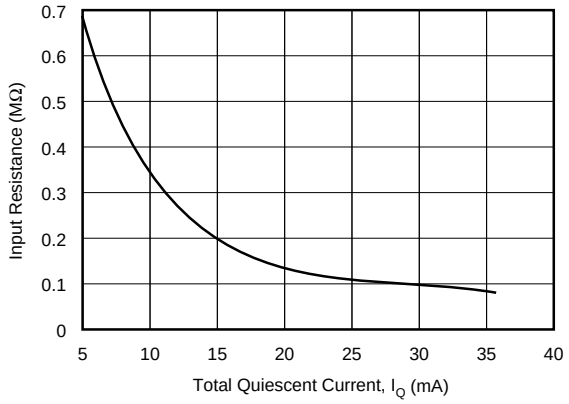
OUTPUT BIAS CURRENT vs TEMPERATURE



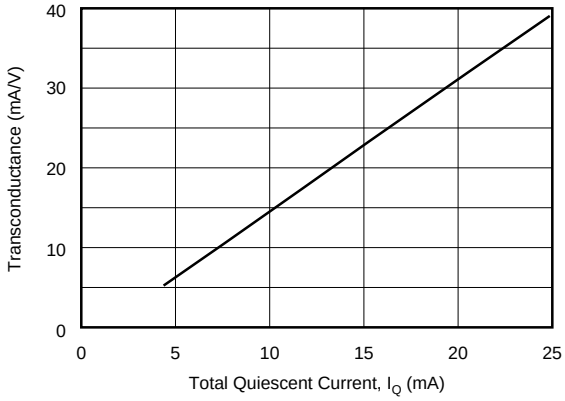
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

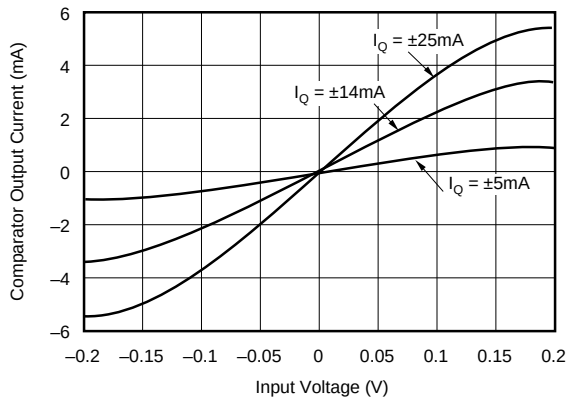
INPUT RESISTANCE vs TOTAL QUIESCENT CURRENT



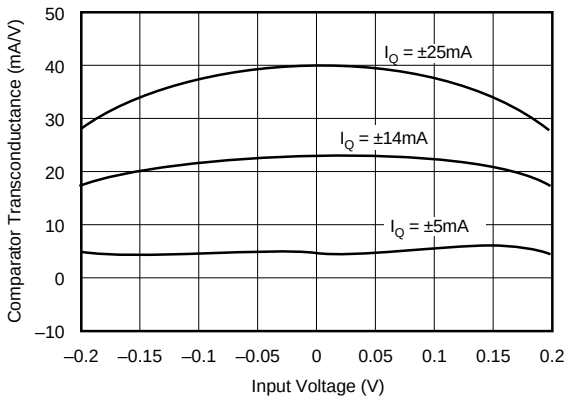
TRANSCONDUCTANCE vs TOTAL QUIESCENT CURRENT



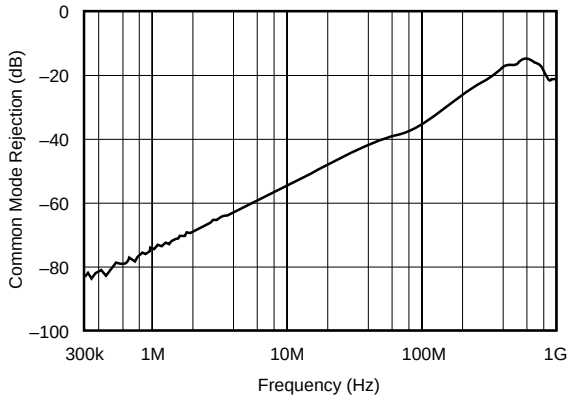
TRANSFER CHARACTERISTICS



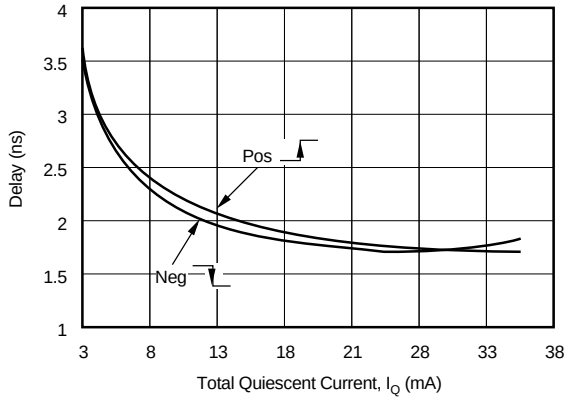
TRANSCONDUCTANCE vs INPUT VOLTAGE



COMMON MODE REJECTION vs FREQUENCY



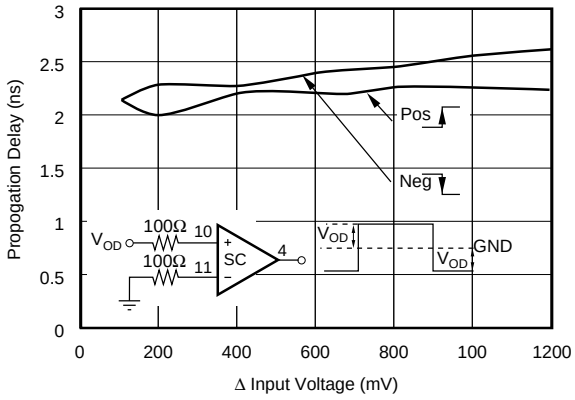
PROPAGATION DELAY vs TOTAL QUIESCENT CURRENT



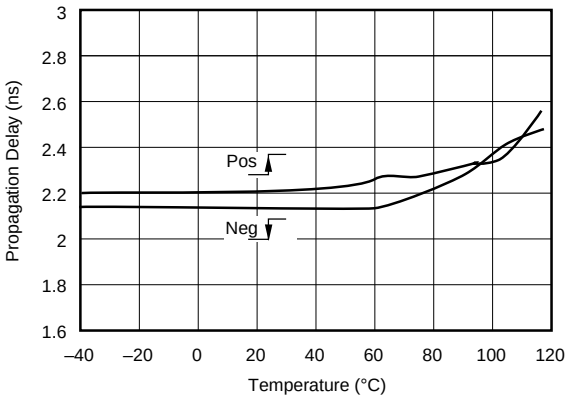
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

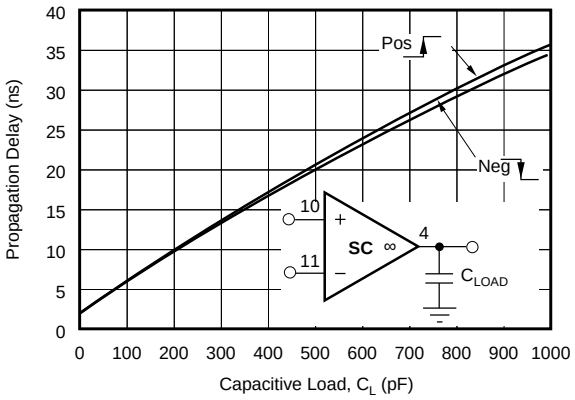
PROPAGATION DELAY vs OVERDRIVE



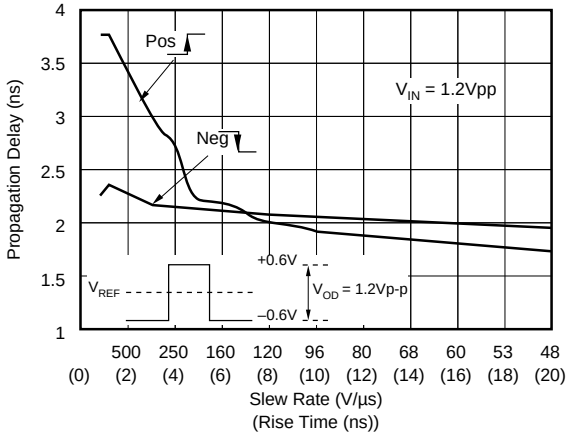
PROPAGATION DELAY TIME vs TEMPERATURE



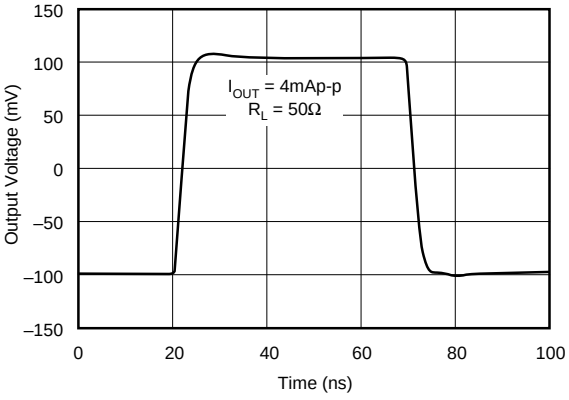
PROPAGATION DELAY vs LOAD CAPACITANCE



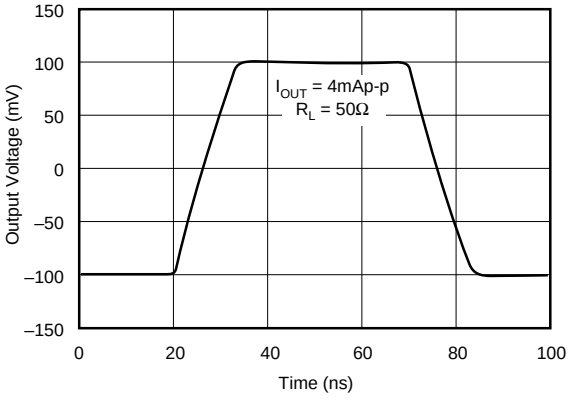
PROPAGATION DELAY vs SLEW RATE



COMPARATOR RESPONSE TO A
2ns ANALOG INPUT PULSE



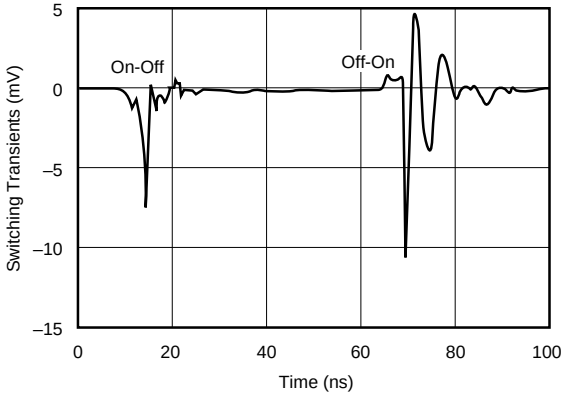
COMPARATOR RESPONSE TO A
10ns ANALOG INPUT PULSE



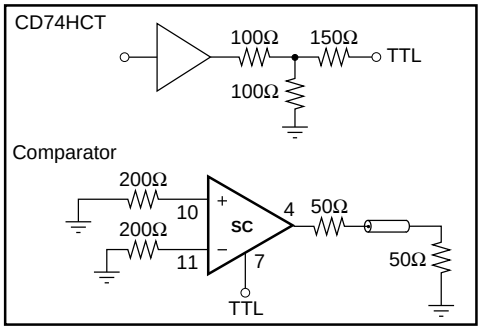
TYPICAL PERFORMANCE CURVES (CONT)

R_Q = 300Ω, T_A = +25°C, V_{CC} = ±5V unless otherwise noted.

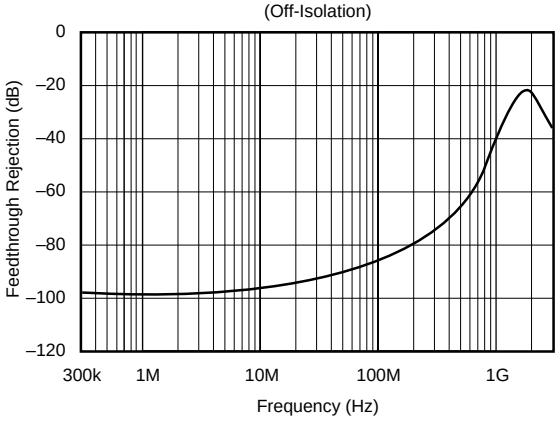
SWITCHING TRANSIENTS



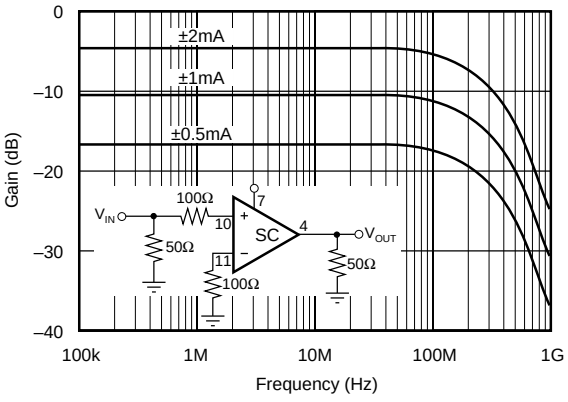
SWITCHING TRANSIENTS TEST CIRCUITS



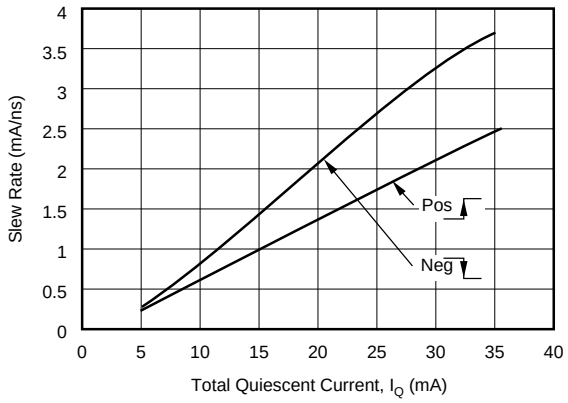
FEEDTHROUGH REJECTION vs FREQUENCY
(Off-Isolation)



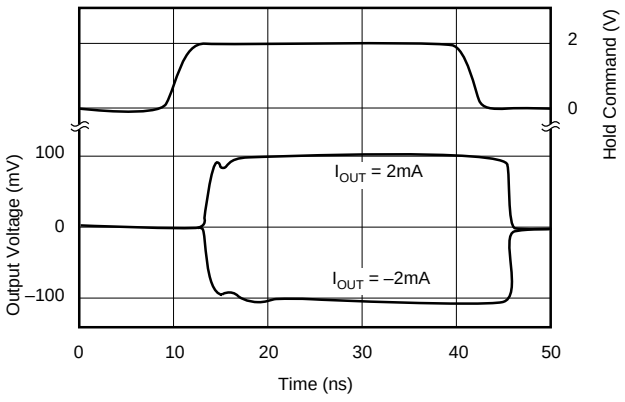
BANDWIDTH vs OUTPUT CURRENT SWING



SLEW RATE vs TOTAL QUIESCENT CURRENT



HOLD COMMAND DELAY TIME



DISCUSSION OF PERFORMANCE

The SHC615, which contains a wideband Operational Transconductance Amplifier and a fast sampling comparator, represents a complete subsystem for very fast and precise DC restoration, offset clamping and correction to GND or to an adjustable reference voltage, and low frequency hum suppression of wideband operational or buffer amplifiers.

Although the IC was designed to improve or stabilize the performance of complex, wideband video signals, it can also be used as a sample and hold amplifier, high-speed integrator, peak detector for nanosecond pulses, or demodulator or modulator for pulse code transmission systems. A wideband Operational Transconductance Amplifier (OTA) with a high-impedance cascode current source output and a fast and precise sampling comparator set a new standard for high-speed sampling applications.

Both can be used as stand-alone circuits or combined to create more complex signal processing stages like sample and hold amplifiers. The SHC615 simplifies the design of input amplifiers with high hum suppression, clamping or DC-restoration stages in professional broadcast equipment, high-resolution CAD monitors and information terminals, signal processing stages for the energy and peak value of small and fast nanoseconds pulses, and eases the design of high-speed data acquisition systems behind a CCD sensor or in front of an analog-to-digital converter.

An external resistor, R_Q, allows the user to set the quiescent current. R_Q is connected from Pin 1 (I_Q adjust) to $-V_{CC}$. It determines the operating currents of both the OTA and comparator sections and controls the bandwidth and AC behavior as well as the transconductance of both sections. Besides the quiescent current setting feature, the Proportional-to-Absolute-Temperature (PTAT) supply increases the quiescent current vs temperature and keeps it constant over a wide range of input voltages. This variation holds the transconductance g_m of the OTA and comparator relatively constant vs temperature. The circuit parameters listed in the specification table are measured with R_Q set to 300Ω, giving a nominal quiescent current at ±15mA. The circuit can be totally switched-off with a current flowing into Pin 1.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

SECTION AND OVERVIEW

The symbol for the OTA section is similar to that of a bipolar transistor, and the self-based OTA can be viewed as a quasi-ideal transistor or as a voltage-controlled current source. Application circuits for the OTA look and operate much like transistor circuits—the bipolar transistor, also, is a voltage-controlled current source. Like a transistor, it has three terminals: a high-impedance input (base) optimized for a low input bias current of 0.3µA, a low-impedance input/output (emitter), and the high-impedance current output (collector).

The OTA consists of a complementary buffer amplifier and a subsequent complementary current mirror. The buffer amplifier features a Darlington output stage and the current mirror has a cascoded output. The addition of this cascode circuitry increases the current source output resistance to 1MΩ and the open-loop gain to typically 96dB. Both features improve the OTAs linearity and drive capabilities. Any bipolar input voltage at the high impedance base has the same polarity and signal level at the low impedance buffer or emitter output. For the open-loop diagrams the emitter is connected to GND and then the collector current is determined by the product voltage between base and emitter times the transconductance. In application circuits (Figure 2b.), a resistor R_E between emitter and GND is used to set the OTA transfer characteristics. The following formulas describe the most important relationships. r_E is the output impedance of the buffer amplifier (emitter) or the reciprocal of the OTA transconductance. Above ±5mA, collector current, I_C, will be slightly less than indicated by the formula.

$$I_C = \frac{V_{IN}}{r_E + R_E} \qquad R_E = \frac{V_{IN}}{I_C} - r_E$$

The R_E resistor may be bypassed by a relatively large capacitor to maintain high AC gain. The parallel combination of R_E and this large capacitor form a high pass filter enhancing the high frequency gain. Other cases may require a RC compensation network parallel to R_E to optimize the high-frequency response. The full power bandwidth measured at the emitter achieves 620MHz. The frequency response of the collector is directly related to the resistor's value between collector and GND; it decreases with increasing resistor values, because it forms a low-pass network with the OTA C-output capacitance.

Figure 1 shows a simplified block and circuit diagram of the SHC615 OTA. Both the emitter and the collector outputs offer a drive capability of ±20mA for driving low impedance lines or inputs. Connecting the collector to the emitter in a direct-feedback buffer configuration increases the drive capability to ±40mA. The emitter output is not current-limited or protected. Momentary shorts to GND should be avoided, but are unlikely to cause permanent damage.

While the OTA's function and labeling looks similar to that of transistors, it offers essential distinctive differences and improvements: 1) The collector current flows out of the C terminal for a positive B-to-E input voltage and into it for negative voltages; 2) A common emitter amplifier operates in non-inverting mode while the common base operates in inverting mode; 3) The OTA is far more linear than a bipolar transistor; 4) The transconductance can be adjusted with an external resistor; 5) Due to the PTAT biasing characteristic the quiescent current increases as shown in the typical performance curve vs temperature and keeps the AC performance constant; 6) The OTA is self-biased and bipolar; and, 7) The output current is zero for zero differential input voltages. AC inputs centered at zero produce an output current centered at zero.

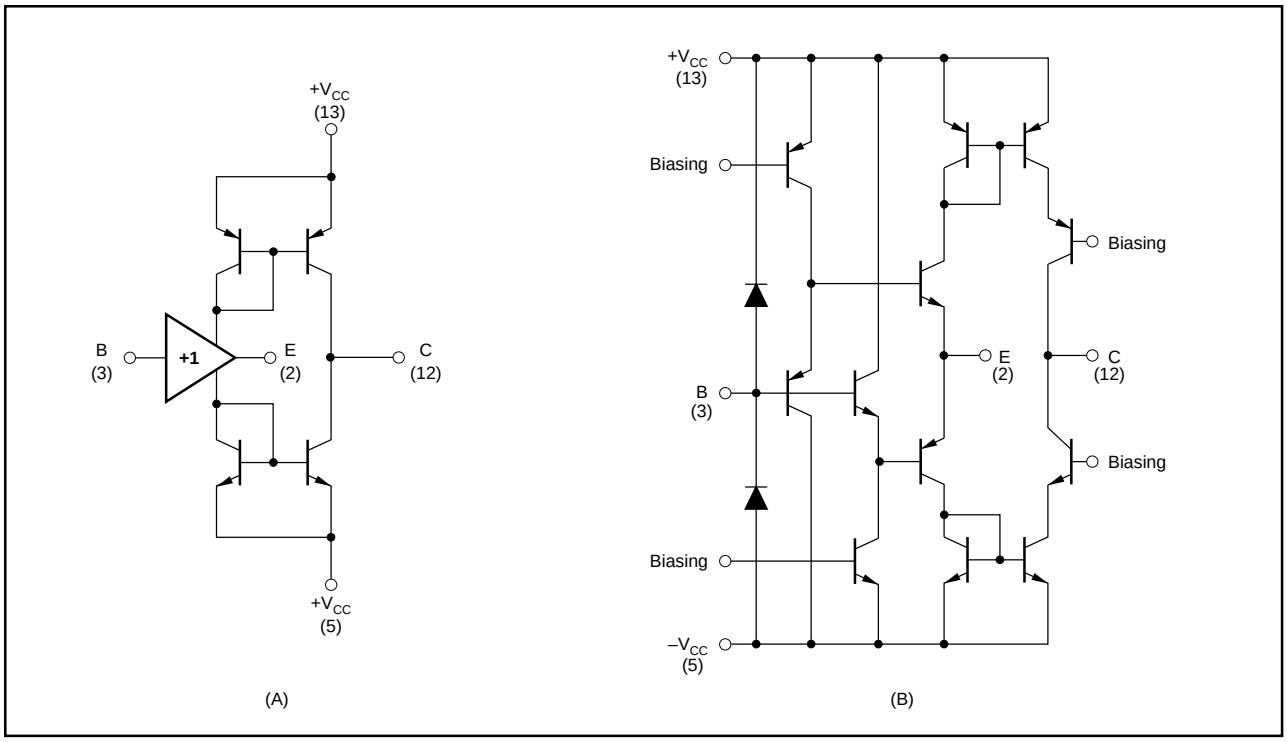


FIGURE 1. a) Simplified Block; and, b) Circuit Diagram of the OTA Section.

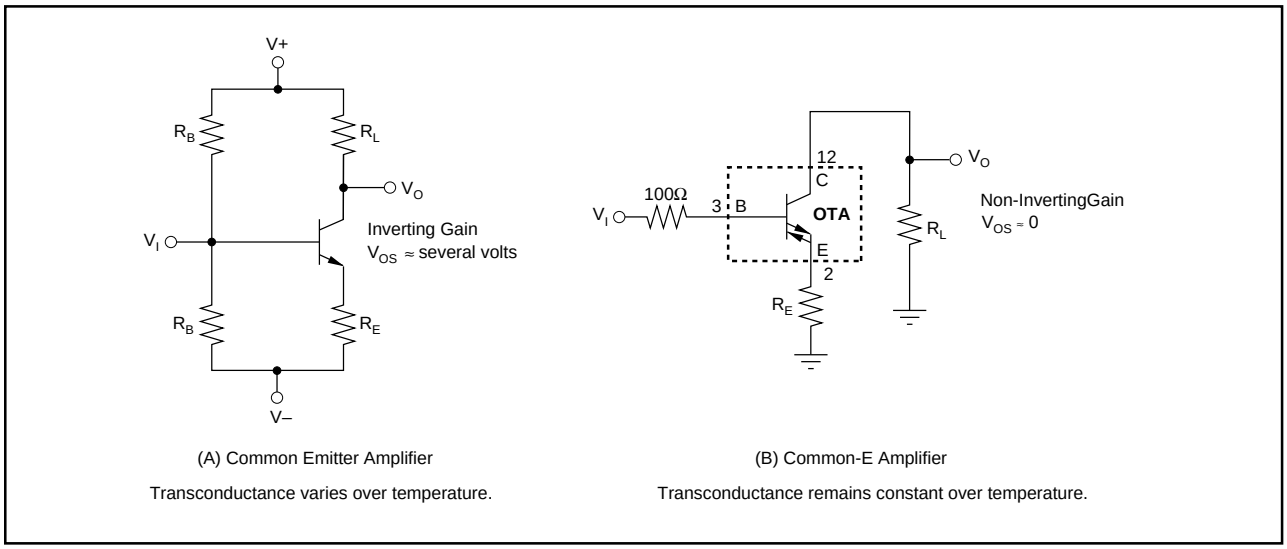


FIGURE 2. a) Common Emitter Amplifier Using a Discrete Transistor; b) Common-E Amplifier Using the OTA Portion of the SHC615.

BASIC APPLICATIONS CIRCUITS

Most application circuits for the OTA section consist of a few basic types which are best understood by analogy to discrete transistor circuits. Just as the transistor has three basic operating modes—common emitter, common base, and common collector—the OTA has three equivalent operating modes common-E, common-B, and common-C (See Figures 2, 3 and 4). Figure 2 shows the OTA connected as a Common-E amplifier which is equivalent to a common emitter transistor amplifier. Input and output can be ground referenced without any biasing. Due to the sense of the output current, the amplifier is non-inverting.

Figure 4 shows the common-B amplifier. This configuration produces an inverting gain, and the input is low-impedance. When a high impedance input is needed, it can be created by inserting a buffer amplifier like BUF600 in series.

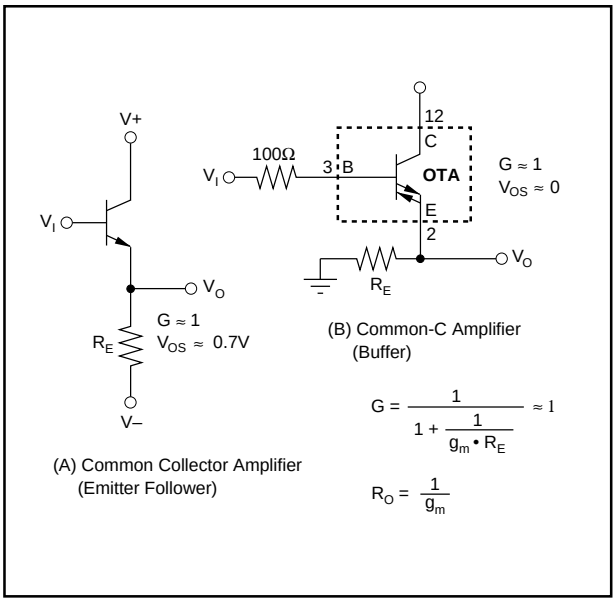


FIGURE 3. a) Common Collector Amplifier Using a Discrete Transistor; b) Common-C Amplifier Using the OTA Portion of the SHC615.

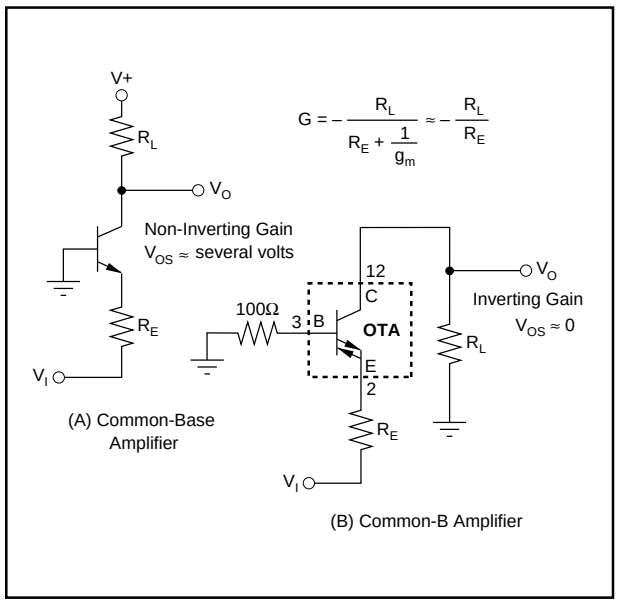


FIGURE 4. a) Common Base Amplifier Using a Discrete Transistor; b) Common-B Amplifier Using the OTA Portion of the SHC615.

SAMPLING COMPARATOR

The SHC615 sampling comparator features a very short 2.2ns propagation delay and utilizes a new switching circuit architecture to achieve excellent speed and precision.

It provides high impedance inverting and non-inverting inputs, a high-impedance current source output and a TTL-CMOS-compatible Hold Control Input.

The sampling comparator consists of an operational transconductance amplifier (OTA), a buffer amplifier, and a subsequent switching circuit. The OTA and buffer amplifier are directly tied together at the buffer outputs to provide the two identical high-impedance inputs and high open-loop transconductance. Even a small differential input voltage multiplied with the high transconductance results in an output current—positive or negative—depending upon the input polarity. This is similar to the low or high status of a conventional comparator. The current source output features high output impedance, output bias compensation, and is optimized for charging a capacitor in DC restoration, nanosecond integrators, peak detectors and S/H circuits. The typical comparator output current is ±3.2mA and the output bias current is minimized to typically ±10µA in the sampling mode.

This innovative circuit achieves the slew rate representatives of an open-loop design. In addition, the acquisition slew current for a hold or storage capacitor is higher than standard diode bridge and switch configurations, removing a main contributor to the limits of maximum sampling rate and input frequency.

The switching circuits in the SHC615 use current steering (versus voltage switching) to provide improved isolation between the switch and analog sections. This results in low aperture time sensitivity to the analog input signal, reduced power supply and analog switching noise. Sample-to-hold peak switching is 40fC.

The additional offset voltage or switching transient induced on a capacitor at the current source output by the switching charge can be determined by the following formula:

$$\text{Offset(V)} = \frac{\text{Charge(pC)}}{\text{C}_\text{H}\ \text{Total(pF)}}$$

The switching stage input is insensitive to the low slew rate performance of the hold control command and compatible with TTL/CMOS logic levels. With a TTL logic high, the comparator is active, comparing the two input voltages and varying the output current accordingly. With a TTL logic low, the comparator output is switched off.

APPLICATION INFORMATION

The SHC615 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur.

Inputs of the SHC615 are protected with internal diode clamps as shown in Figure 1. These protection diodes can safely conduct 10mA continuously (30mA peak). If input voltages can exceed the power supply voltages by 0.7V, the input signal current must be limited.

BASIC CONNECTIONS

Figure 6 shows the basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See “Circuit Layout” at the end of the applications discussion for further suggestions on layout.

If the high speed TTL-hold command signal goes negative due to reflections for AC-coupling, the hold control input must be protected by an external reverse bias diode to ground as shown in Figure 6.

CIRCUIT LAYOUT

The high-frequency performance of the SHC615 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions, not as absolute requirements. Oscillations, ringing, poor bandwidth, poor settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF); parallel 470pF and/or 10nF ceramic chip capacitors may be added if desired. Surface mount types are recommended because of their low lead inductance. Supply bypassing is extremely critical at high frequencies and when driving high current loads.
- PC board traces for power lines should be wide to reduce impedance.

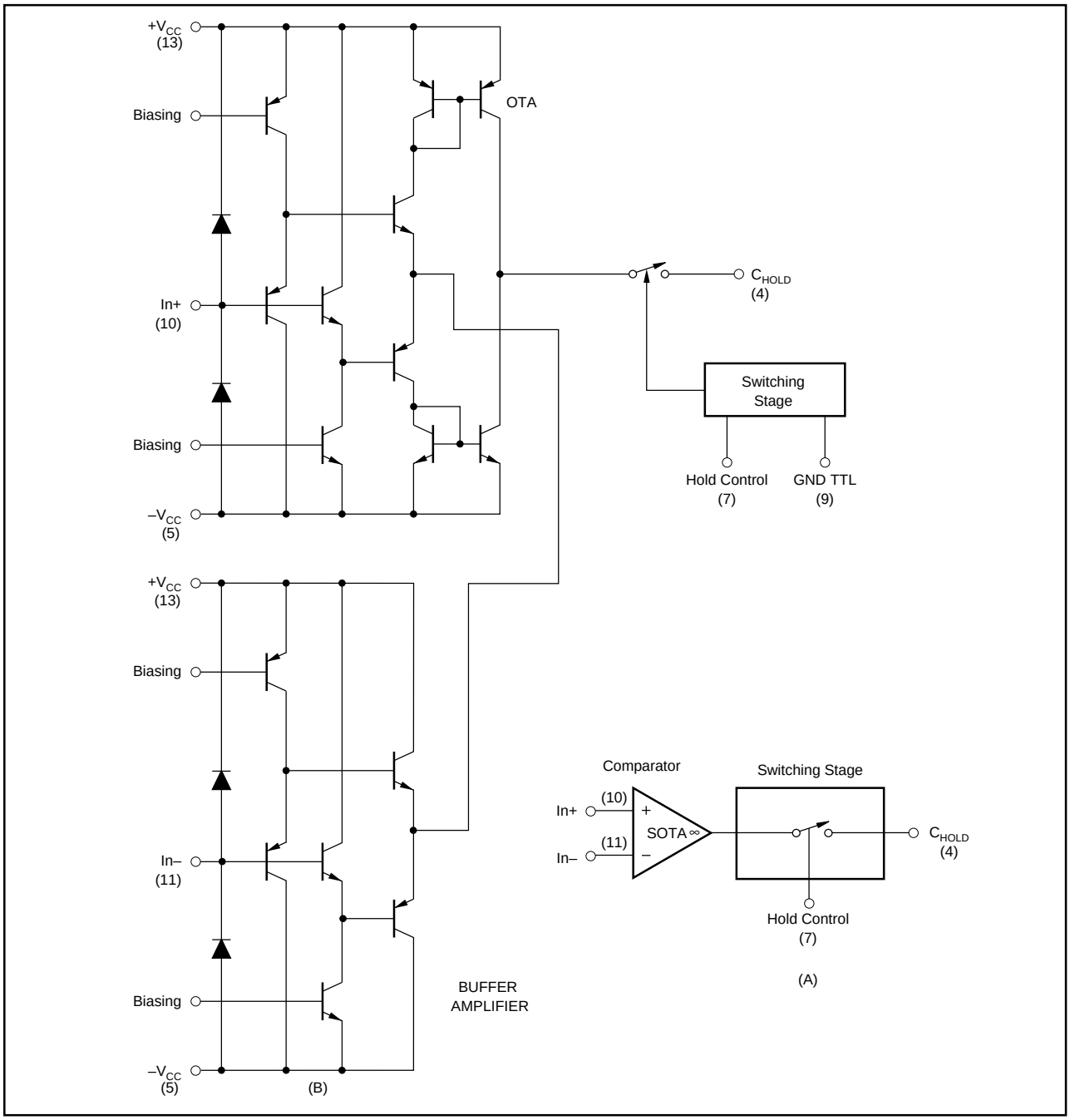


FIGURE 5. a) Simplified Block Diagram; and, b) Circuit Diagram of the Sampling Comparator which Includes the Sampling Operational Transconductance Amplifier (SOTA) and the Switching Stage.

- Make short, low-inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that a low-impedance ground is available throughout the layout.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances such as the amplifier's input terminals.
- Sockets are not recommended since they add significant inductance and parasitic capacitance. If sockets are required, use zero-profile sockets.
- Use low-inductance, surface-mount components. Surface-mount components offer the best AC performance.
- A resistor of 100 to 250Ω in series with the high-impedance inputs is recommended to reduce peaking.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.
- Terminate transmission line loads. Unterminated lines, such as box cables, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.
- Protect the hold control input with an external diode if necessary.

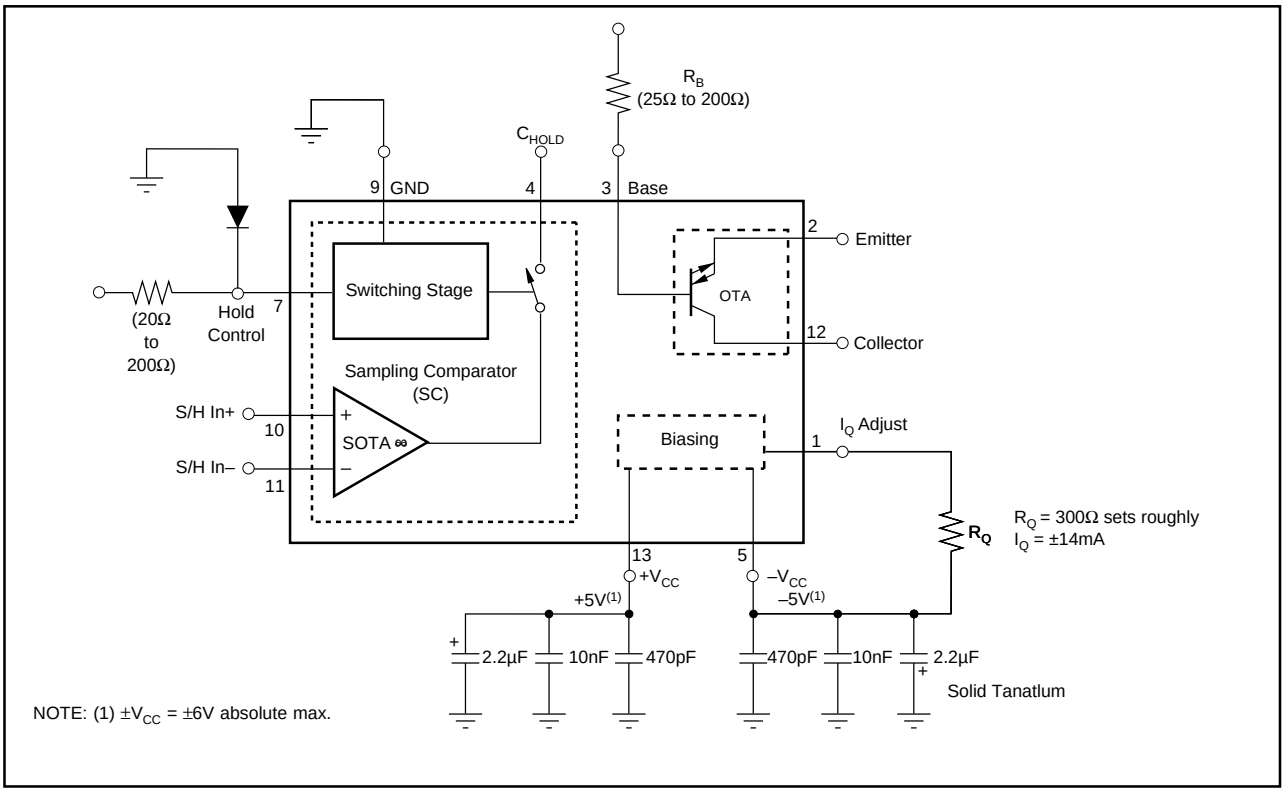


FIGURE 6. Basic Connections

TYPICAL APPLICATIONS

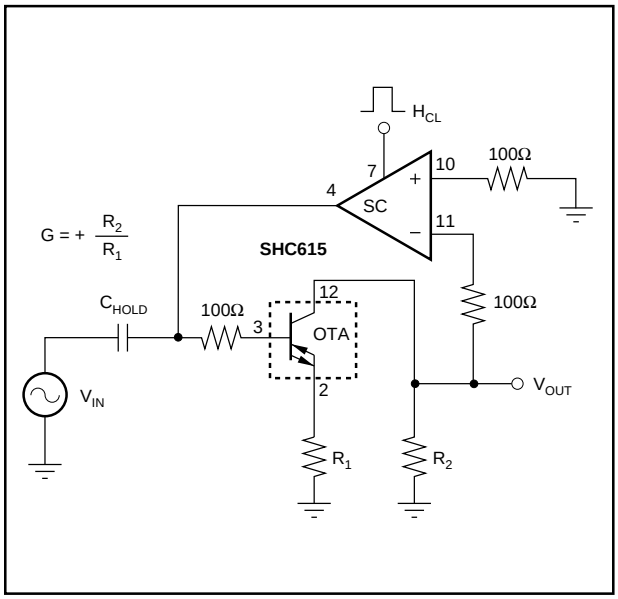


FIGURE 7. Complete DC Restoration System.

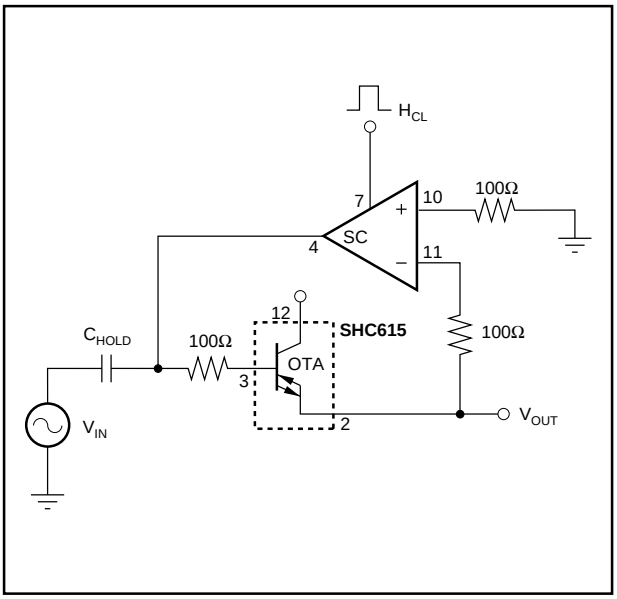


FIGURE 8. DC Restoration of a Buffer Amplifier.

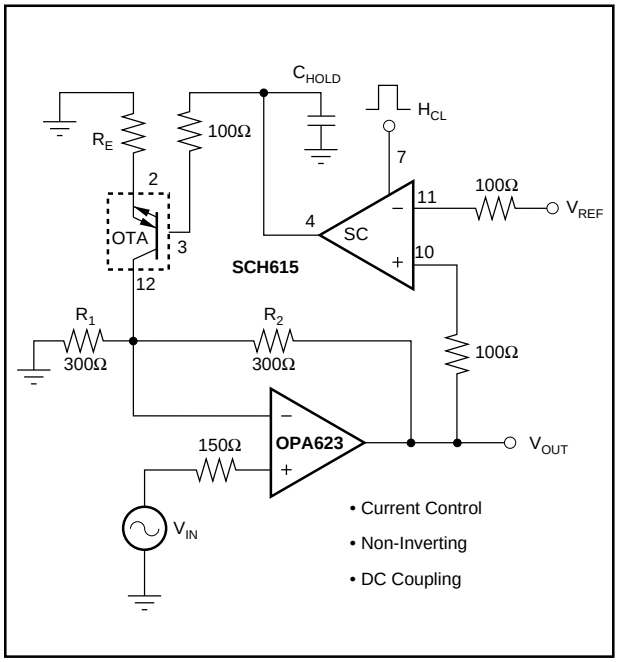


FIGURE 9. Clamped Video/RF Amplifier.

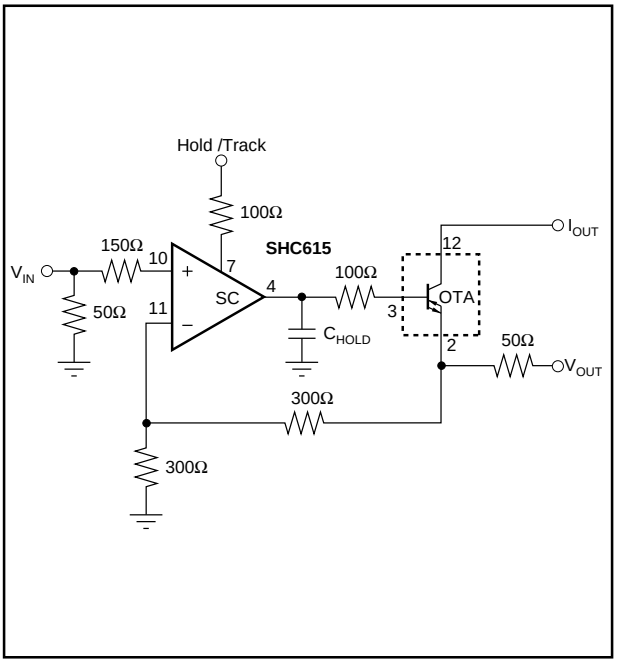


FIGURE 10. Sample/Hold Amplifier.

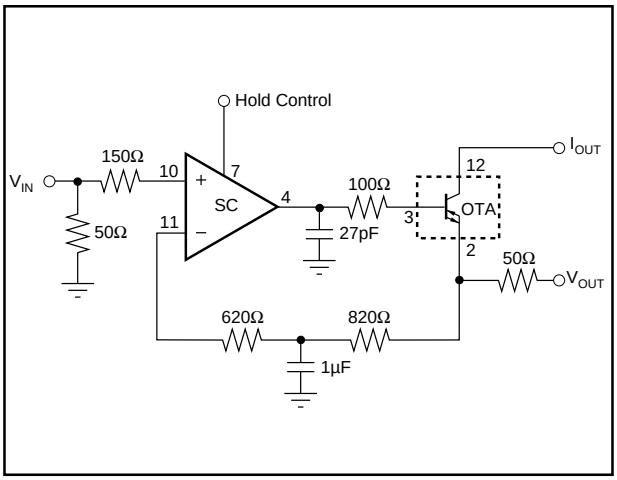


FIGURE 11. Integrator for ns-Pulses.

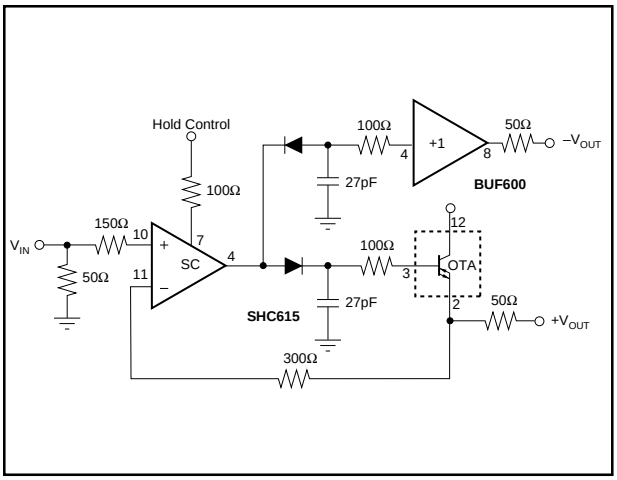


FIGURE 12. Fast Pulse Peak Detector.

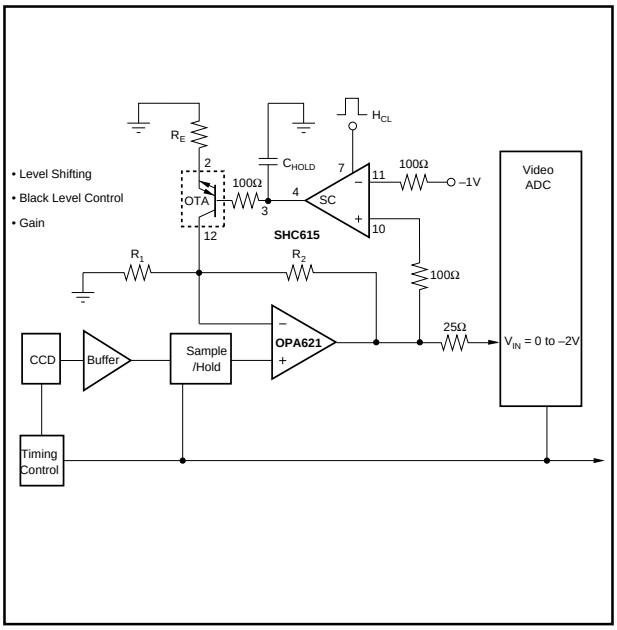


FIGURE 13. CCD Analog Front-End.

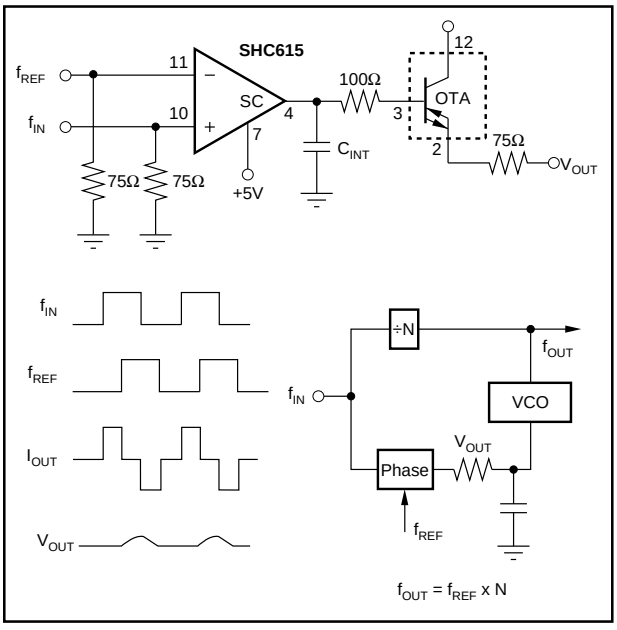
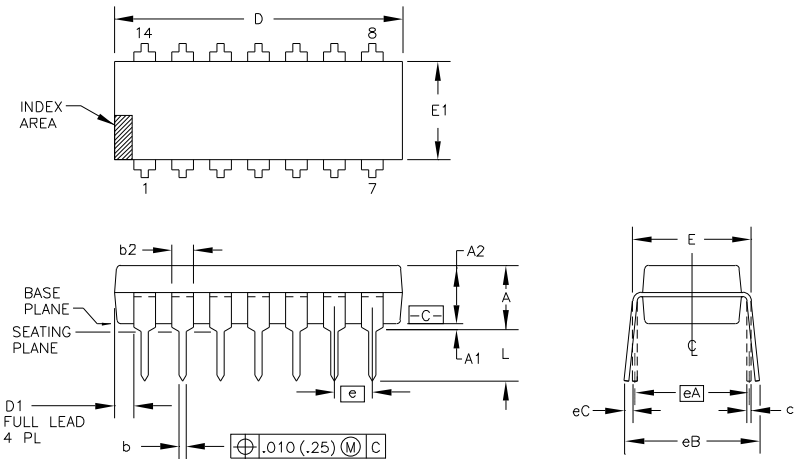


FIGURE 14. Phase Detector For Fast PLL-Systems.

PACKAGE DRAWINGS

Package Number 010 - 14-Pin Plastic, Single-Wide DIP



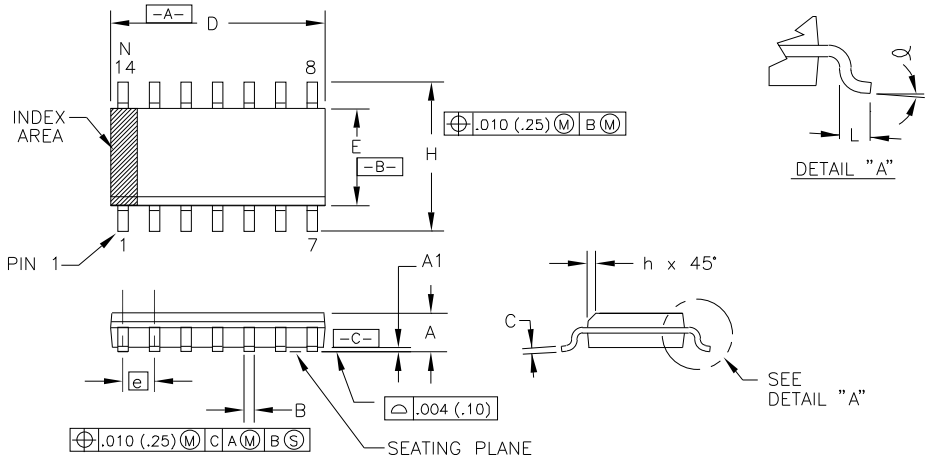
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
c	.008	.014	0.20	0.36	
D	.735	.775	18.67	19.69	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
L	.115	.150	2.92	3.81	3
N	14		14		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ010	REV.: G
JEDEC NUMBER: MS-001-AA	

Package Number 235 - 14-Lead SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.25	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.19	0.25	
D	.3367	.3444	8.55	8.75	2
E	.1497	.1574	3.80	4.00	3
e	.050 BASIC		1.27 BASIC		
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	4
L	.016	.050	0.40	1.27	5
N	14		14		6
α	0°	8°	0°	8°	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ235	REV.: D
JEDEC NUMBER: MS-012-AB	