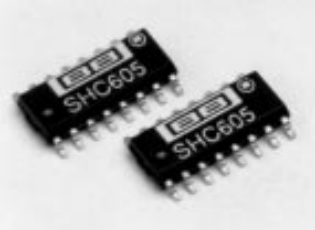
BURR - BROWN®



SHC605

High-Speed Operational TRACK-AND-HOLD AMPLIFIER

FEATURES

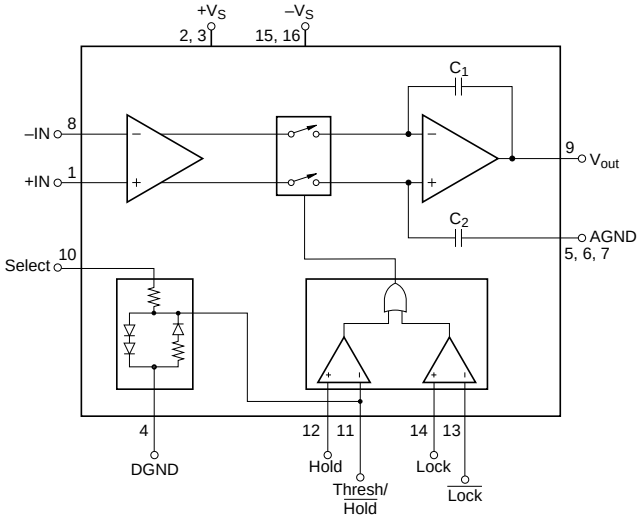
- **VERY GOOD SPURIOUS FREE DYNAMIC RANGE:**
  90dB at 1MHz F_{IN} and 20MSPS
  86dB at 2MHz F_{IN} and 20MSPS
  77dB at 5MHz F_{IN} and 20MSPS
- **LOW ACQUISITION TIME: 30ns to 0.01%**
- **LOW DROOP RATE: 8mV/μs max T_{MIN} to T_{MAX}**
- **LOW POWER CONSUMPTION: 335mW**
- **EXTREMELY VERSATILE ARCHITECTURE: Noninverting, Inverting, and Differential Gains**
- **LOGIC FLEXIBILITY: TTL and ECL Compatible**
- **SMALL PACKAGE: 16-Lead SOIC**
- **EXTENDED TEMPERATURE SPECS: –40°C to +85°C**

APPLICATIONS

- **A/D CONVERTER FRONT ENDS**
- **MULTIPLE CHANNEL SIMULTANEOUS SAMPLING**
- **IMPROVING FLASH ADC PERFORMANCE**
- **PEAK DETECTORS**
- **DAC DEGLITCHING**

DESCRIPTION

The SHC605 is a monolithic high-speed, high accuracy track-and-hold amplifier. It combines fast acquisition and low distortion to provide a complete solution for a wide range of sampling applications. Its new proprietary closed-loop architecture provides a single-chip solution to many data acquisition problems formerly requiring more than one device. Noninverting, inverting, and differential gain configurations are easy to apply with the SHC605. An on-board logic reference circuit makes the SHC605 compatible with both single-ended and differential ECL or TTL clock inputs. An internal track-mode lockout circuit allows edge-triggered operation in data acquisition systems. The SHC605 is available in a 16-lead SOIC package specified for the –40C to +85C industrial temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

PARAMETER	CONDITION	TEMP RANGE	SHC605AU MIN	SHC605AU TYP	SHC605AU MAX	UNITS
DC INPUT PARAMETERS						
Offset Voltage		Full		±1	±7.5	mV
Power Supply Rejection	V_S = ±4.5 to ±5.5V	+25°C	60	85		dB
Input Bias Current	V_{CM} = 0V	Full		15	50	µA
Input Offset Current	V_{CM} = 0V	Full		±0.2	±5	µA
Common-Mode Input Range		Full	±2.0	±2.5		V
Common-Mode Rejection	V_{CM} = ±2VDC	Full		80		dB
Differential Input Impedance		Full		13||1		kΩ||pF
Common-Mode Input Impedance		Full		2||1		MΩ||pF
Open-loop Voltage Gain	V_O = ±2V, R_L = 100Ω	+25°C		100		dB
OUTPUT						
Voltage Output	R_L = 50Ω	Full	±2.0	±2.5		V
Current Output		+25°C	±40	±80		mA
		Full	±40	±60		mA
Short Circuit Current		Full		±140		mA
Output Resistance,						
Closed-Loop: Track-Mode	DC	Full		0.0001		Ω
Hold-Mode	DC	Full		0.01		Ω
DIGITAL INPUTS/OUTPUTS						
TTL Input Levels [1]	Hold Input Only					
V_{IL}	Logic "LO"	Full	0		+1.0	V
V_{IH}	Logic "HI"	Full	+2.0		+5.0	V
Single-Ended ECL Input Levels [2]	Hold/$\overline{\text{Hold}}$ and Lock/$\overline{\text{Lock}}$ Inputs					
V_{IL}	Logic "LO"	Full	–1.80		–1.45	V
V_{IH}	Logic "HI"	Full	–1.05		–0.80	V
Common-Mode Input Voltages	Hold/$\overline{\text{Hold}}$	Full	–3		+5	V
	Lock/$\overline{\text{Lock}}$	Full	$-V_S$		+3	V
Differential Input Voltages	Hold/$\overline{\text{Hold}}$ and Lock/$\overline{\text{Lock}}$ Inputs	Full	0.2		5.0	V
Digital Input Currents						
I_{IL}, Lock/$\overline{\text{Lock}}$ Inputs Only	ECL Logic "LO", V_{IL} = –1.60V	Full			5	µA
I_{IL}, Hold/$\overline{\text{Hold}}$ Inputs Only	ECL or TTL Logic "LO"	Full			–100	µA
I_{IH}, Lock/$\overline{\text{Lock}}$ Inputs Only	Logic "HI", V_{IH} = –1.0V	Full			50	µA
I_{IH}, Hold/$\overline{\text{Hold}}$ Inputs Only		Full			–10	µA
Threshold Voltage Output[3]						
TTL[4]		Full	1.1	1.5	1.9	V
ECL[5]	$-V_S$ = –5.2V	Full	–1.40		–1.10	V
TRACK-MODE RESPONSE						
Closed-Loop Bandwidth	Gain = +1V/V	+25°C	100	200		MHz
	Gain = +2V/V	+25°C		75		MHz
	Gain = +5V/V	+25°C		20		MHz
	Gain = +10V/V	+25°C		10		MHz
Full Power Response	±1V Input, –3dB Output	Full		32		MHz
Slew Rate [6]	G = +1, 2V Step	+25°C	140	200		V/µs
		Full	120	200		V/µs
Acquisition Time to 1%[7]	2V Step	Full		15	25	ns
0.1%	2V Step	Full		23	35	ns
0.012%	2V Step	Full		30	45	ns
0.012%	4V Step	Full		40	60	ns
Input Voltage Noise	1MHz to 100MHz			2.5		nV/√Hz
Input Bias Current Noise	1MHz to 100MHz			2.5		pA/√Hz
Differential Gain	3.58MHz, V_O = 0 to 0.7Vp–p			0.005		%
Differential Phase	3.58MHz, V_O = 0 to 0.7Vp–p			0.005		degrees
Spurious Free Dynamic Range						
(5MHz)	V_O = ±1V			83		dBc
(10MHz)	V_O = ±1V			73		dBc

NOTE: (1) Select (Pin 10) connected to $+V_S$ for TTL threshold voltage on Pin 11. (2) Select (Pin 10) connected to $-V_S$ for ECL threshold voltage on Pin 11. (3) Output voltage on pin 11. (4) Pin 10 (Select) connected to $+V_S$. (5) Pin 10 (Select) connected to $-V_S$. (6) Slew rate is rate of change from 10% to 90% of a 2V output step. (7) Acquisition time includes hold-to-track delay switch time. (8) Hold noise is proportional to the time in the hold mode. For example, if the hold time is 25ns, the accumulated noise is 10µVrms(9) This is the maximum length of time the SHC605 can remain in the hold mode and still maintain a linear droop rate. (10) Select (Pin 10) connected to $+V_S$.

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

PARAMETER	CONDITION	TEMP RANGE	SHC605AU MIN	SHC605AU TYP	SHC605AU MAX	UNITS
TRACK-TO-HOLD SWITCHING	V_{IN} = 0V					
Aperture Delay		Full		1.7		ns
Aperture Jitter		Full		2.4		ps rms
Pedestal Offset		+25°C		±5	±20	mV
over Temperature		Full		±5	±25	mV
Transient Amplitude		Full		±5		mV
Settling Time to 1mV		Full		8	15	ns
100µV		Full		15		ns
HOLD-MODE RESPONSE						
Spurious Free Dynamic Range						
(1MHz, 20MSPS)	V_O = ±1V	Full	78	90		dBc
(2MHz, 20MSPS)	V_O = ±1V	Full	74	86		dBc
(5MHz, 20MSPS)	V_O = ±1V	Full	65	77		dBc
(10MHz, 20MSPS)	V_O = ±1V	+25°C		60		dBc
(10MHz, 20MSPS)	V_O = ±0.5	+25°C		72		dBc
Hold Noise[8]				$400xt_H$		V/s rms
Droop Rate		Full		±1	±8	mV/µs
Hold Time[9]		Full			2	µs
Feedthrough Rejection (20MHz)		+25°C		85		dB
POWER SUPPLY						
Specified Operating Voltage		Full	±4.50	±5	±5.50	V
Positive Supply Current[10]		Full		34	39	mA
Negative Supply Current[10]		Full		33	39	mA
Total Power Dissipation		Full		335	390	mW
TEMPERATURE RANGE						
Specification	Ambient	Full	–40		+85	°C
Storage			–55		+150	°C
Thermal Resistance, θ_{JA}		Full		100		°C/W

NOTE: (1) Select (Pin 10) connected to $+V_S$ for TTL threshold voltage on Pin 11. (2) Select (Pin 10) connected to $-V_S$ for ECL threshold voltage on Pin 11. (3) Output voltage on pin 11. (4) Pin 10 (Select) connected to $+V_S$. (5) Pin 10 (Select) connected to $-V_S$. (6) Slew rate is rate of change from 10% to 90% of a 2V output step. (7) Acquisition time includes hold-to-track delay switch time. (8) Hold noise is proportional to the time in the hold mode. For example, if the hold time is 25ns, the accumulated noise is 10µVrms. (9) This is the maximum length of time the SHC605 can remain in the hold mode and still maintain a linear droop rate. (10) Select (Pin 10) connected to $+V_S$.

ABSOLUTE MAXIMUM RATINGS

Supply ..... ±7VDC
Input Voltage Range ..... ±5V
Differential Input Voltage ..... ±5.5V (between +In and –In inputs)
Storage Temperature Range ..... –40°C to +125°C
Lead Temperature (soldering, SOIC 3s) ..... +260°C
Output Short Circuit to Ground (+25°C) ..... Continuous to Ground
Junction Temperture (T_j) ..... +175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
SHC605AU	16-Pin SOIC	265

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

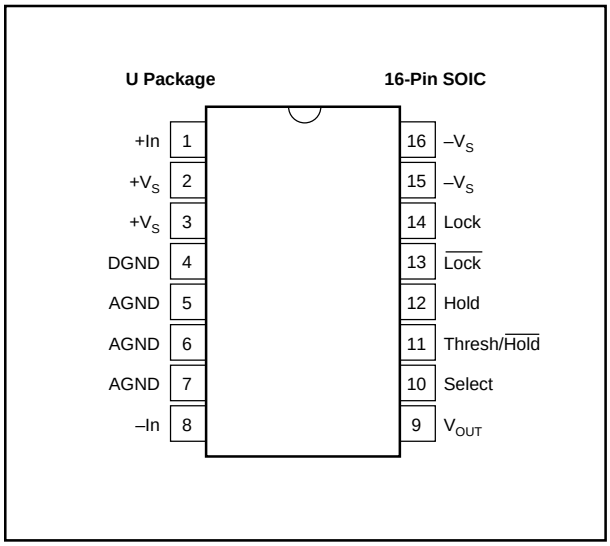
MODEL	PACKAGE	TEMPERATURE
SHC605AU	16-Pin SOIC	–40°C to +85°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

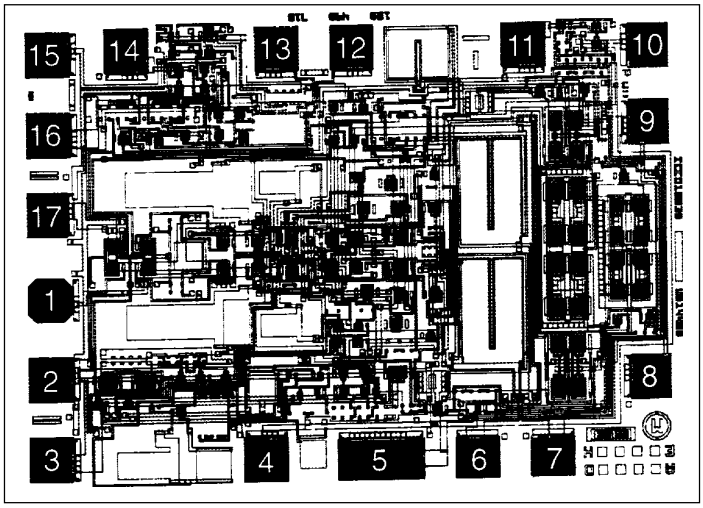
PIN CONFIGURATION



PIN DESCRIPTION

PIN #	SYMBOL	DESCRIPTION
1	+In	Non-Inverting Input
2	$+V_S$	+5V Supply
3	$+V_S$	+5V Supply
4	DGND	Digital Ground
5	AGND	Analog Ground
6	AGND	Analog Ground
7	AGND	Analog Ground
8	–In	Inverting Input
9	V_{OUT}	Output Voltage
10	Select	+5V Selects TTL; –5V Selects ECL
11	Thresh/$\overline{\text{Hold}}$	Logic threshold for single-ended operation or complement Hold input for differential operation
12	Hold	True Hold input
13	$\overline{\text{Lock}}$	Complement Lock Input
14	Lock	True Lock input; Locks SHC605 in Hold-mode regardless of Hold/$\overline{\text{Hold}}$ Inputs
15	$–V_S$	–5V Supply
16	$–V_S$	–5V Supply

DICE INFORMATION



SHC605 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	+In	10	Select
2	$+V_S$	11	Comp
3	$+V_S$	12	Thresh/$\overline{\text{Hold}}$
4	DGND	13	Hold
5	AGND	14	$\overline{\text{Lock}}$
6	C_2	15	Lock
7	C_1	16	$–V_S$
8	–In	17	$–V_S$
9	V_{OUT}		

Substrate Bias: Negative supply ($–V_S$).

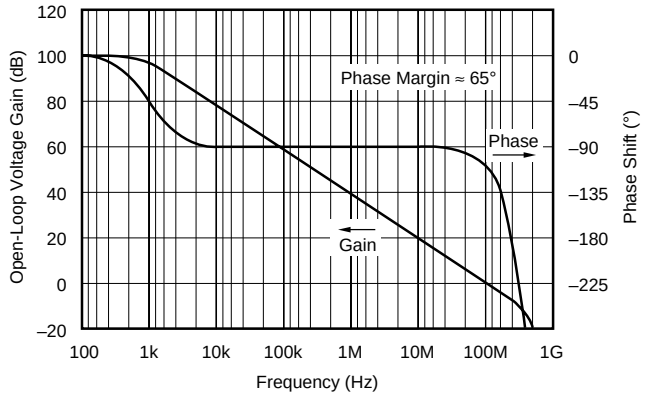
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	58 x 80	
Die Thickness	14 ±1	
Min. Pad Size	4 x 4	0.1 x 0.1
Backing	Gold	
Metallization	Gold	

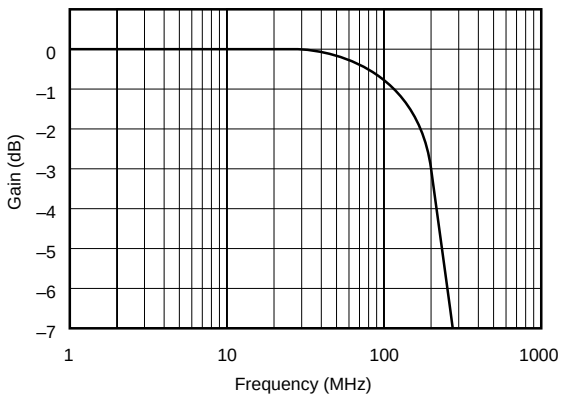
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

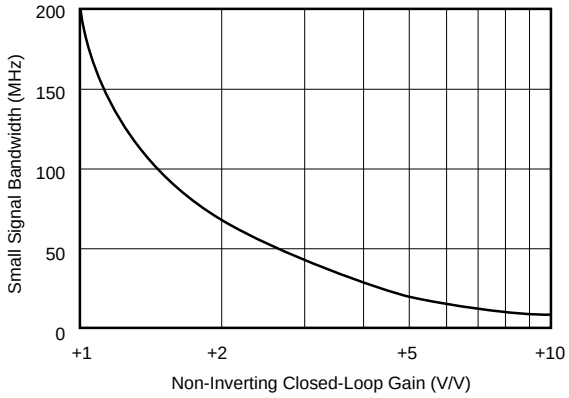
OPEN-LOOP FREQUENCY RESPONSE (Track Mode)



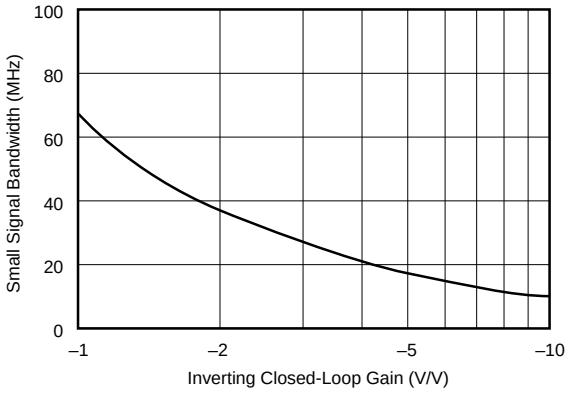
CLOSED-LOOP GAIN = +1V/V
vs FREQUENCY (Track Mode)



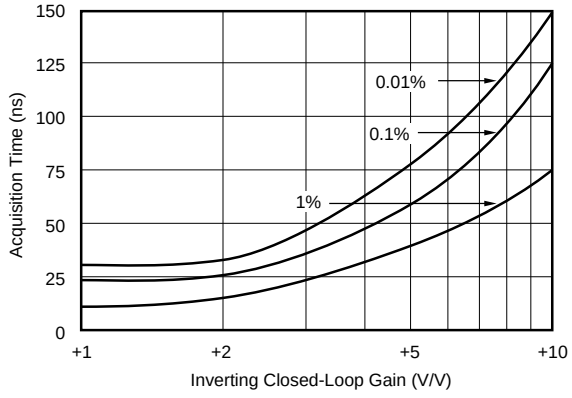
NON-INVERTING CLOSED-LOOP GAIN
vs SMALL SIGNAL BANDWIDTH



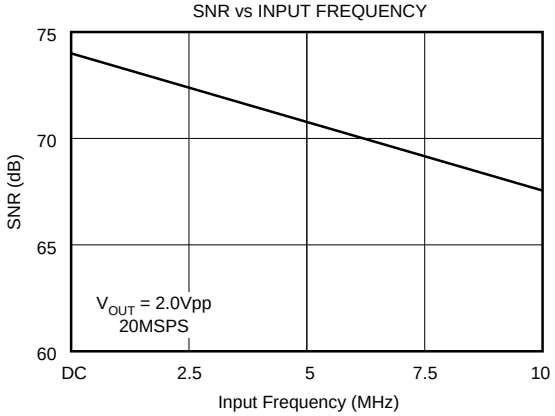
INVERTING CLOSED-LOOP GAIN
vs SMALL SIGNAL BANDWIDTH



ACQUISITION TIME
vs NON-INVERTING CLOSED-LOOP GAIN



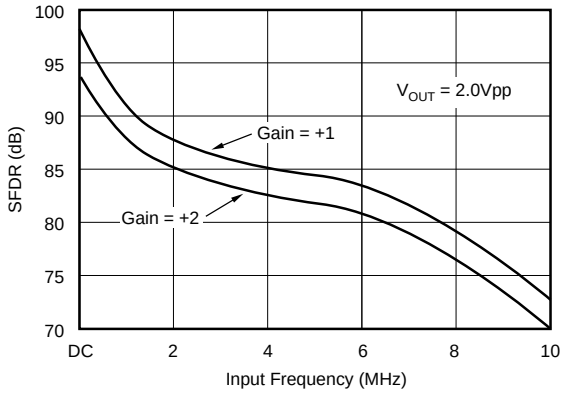
SNR vs INPUT FREQUENCY



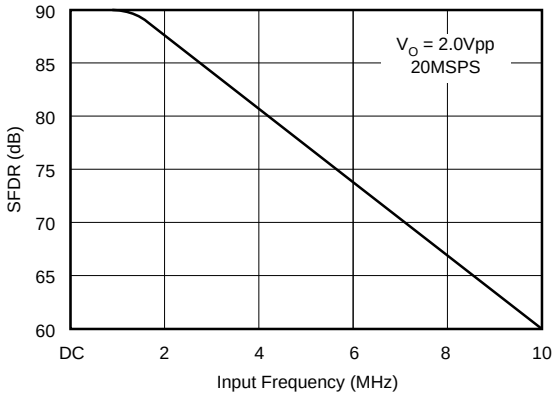
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

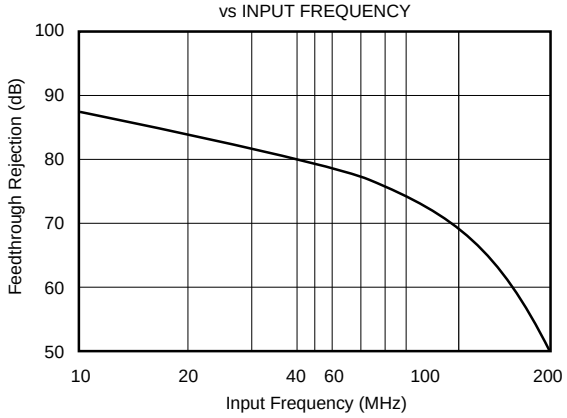
LARGEST HARMONIC
vs INPUT FREQUENCY (Track Mode)



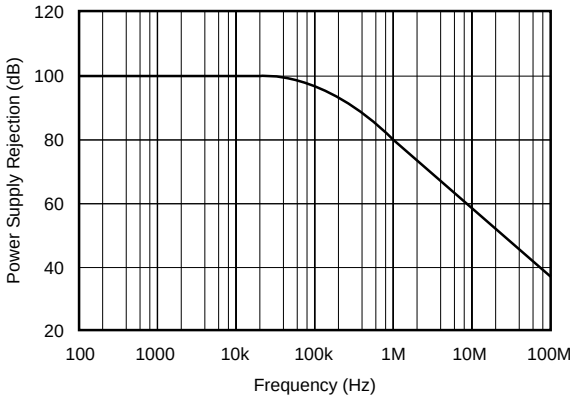
LARGEST HARMONIC
vs INPUT FREQUENCY (Hold Mode)



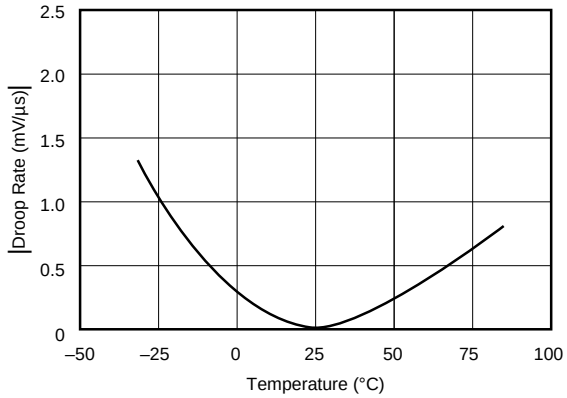
FEEDTHROUGH REJECTION
vs INPUT FREQUENCY



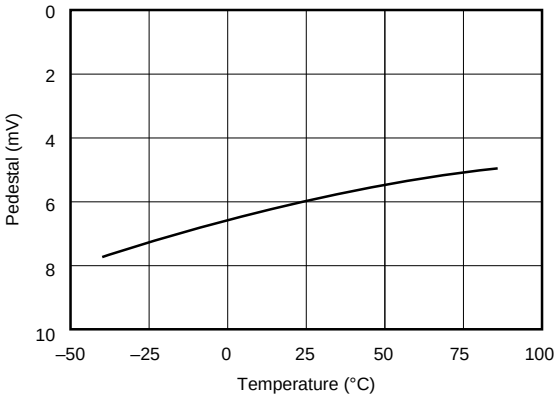
POWER SUPPLY REJECTION
vs SUPPLY RIPPLE FREQUENCY (Track Mode)



DROOP RATE vs TEMPERATURE



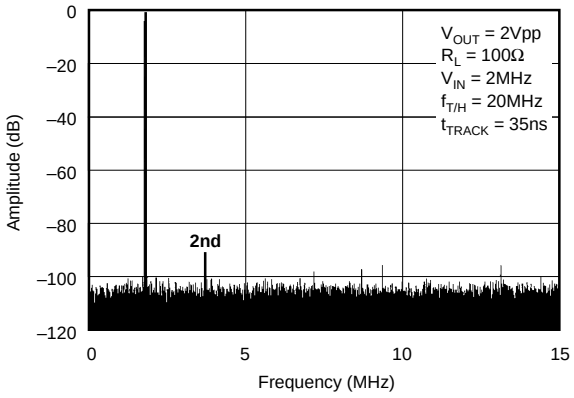
PEDESTAL vs TEMPERATURE



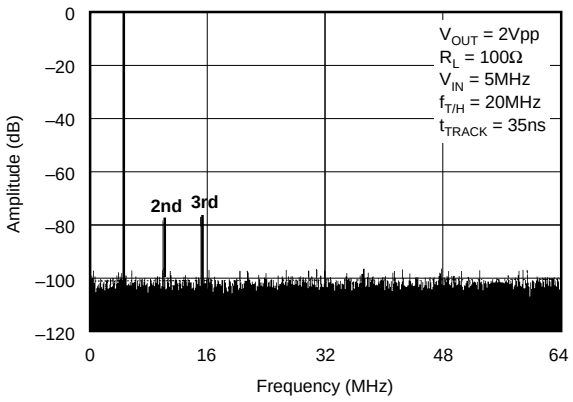
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, $\pm V_S$ = ±5V, G = +1V/V, R_L = 100Ω, C_L = 5pF, and ECL Hold/$\overline{\text{Hold}}$ Inputs, unless otherwise noted.

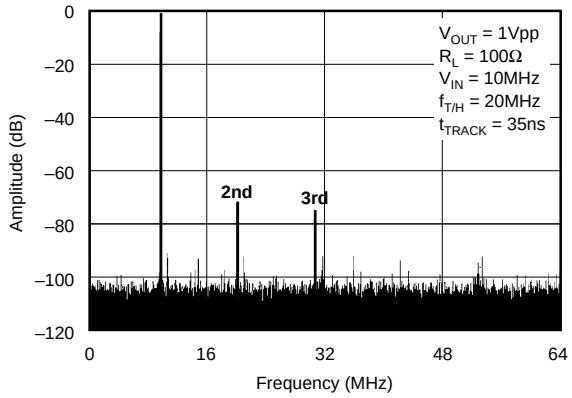
HOLD-MODE DISTORTION
AT 20MSPS, V_{IN} = 2MHz



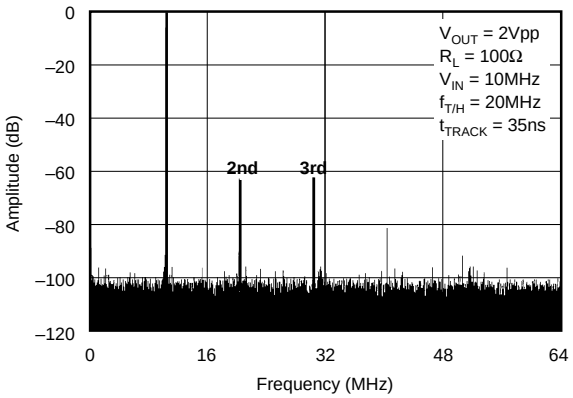
HOLD-MODE DISTORTION
AT 20MSPS, V_{IN} = 5MHz



HOLD-MODE DISTORTION
AT 20MSPS, V_{IN} = 10MHz



HOLD-MODE DISTORTION
AT 20MSPS, V_{IN} = 10MHz



TIMING DEFINITIONS

Acquisition Time is the time it takes to reacquire the input signal when switching from the hold to track mode. This time interval starts at 50% of the clock transition and ends when the input signal is reacquired to within a specified accuracy at the output. This specification does not include the track-to-hold settling time.

Aperture Delay is a measure of the track-to-hold switch delay time. It is the difference between the analog input amplifier's signal path delay and the digital track-to-hold switch delay. A positive delay indicates the digital switch delay is larger than the analog amplifier delay.

Aperture Jitter is random variation in the aperture delay. This specification is measured in ps-rms and results in phase noise on the held signal. A large aperture jitter value can manifest itself by degrading the SNR of a sampling ADC.

Droop Rate is the change of the held output voltage as a function of time. The measurement starts immediately after the device switches from the track to hold mode.

Feedthrough Rejection is a measure of the amount of the input signal that "feeds through" to the output while the device is in the hold mode. This specification is usually a function of frequency, with degradation at higher frequencies.

Hold-to-Track Delay is the time from the track command to the point when the output begins changing to acquire a new signal. This delay is included in the SHC605's specified acquisition time.

Pedestal Offset is the error voltage step incurred at the output when the device is switched from the track to hold mode.

Track-to-Hold Settling Time is the time for the track to hold transient to settle to within a specified accuracy.

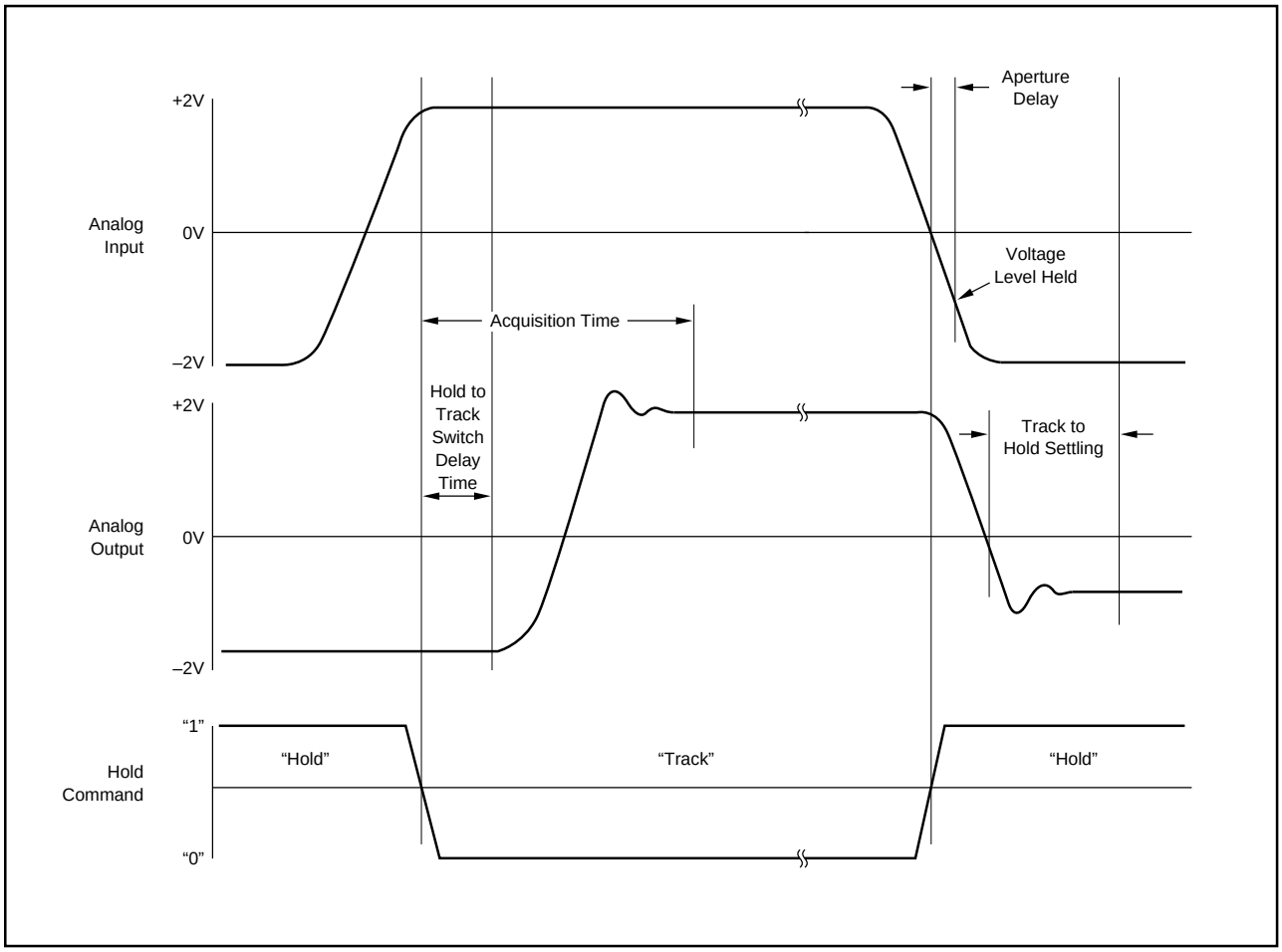


FIGURE 1. SHC605 Timing Diagram.

THEORY OF OPERATION

The SHC605 is a monolithic track-and-hold circuit fabricated on an extremely fast complementary bipolar process. Figure 2 provides a simplified circuit diagram of the SHC605. A conventional two-stage operational amplifier is shown with a standard differential phase compensation scheme sometimes referred to as "doublet compensation." Capacitors C_1 and C_2 compensate the amplifier in the track-mode and hold the analog output signal in the hold-mode. Switching from track to hold is achieved by turning off the amplifier's input stage and isolating C_1 and C_2 from the input signal.

The differential two-stage amplifier architecture of the SHC605 provides many performance advantages over traditional open-loop designs. The use of differential hold capacitors provides a first-order correction for many errors including distortion, pedestal, and droop. A dominant cause of distortion in high-speed amplifiers is the nonlinear transistor junction capacitance connected to the hold capacitor(s). This parasitic capacitance varies as the voltage across it changes. Most open-loop track-and-hold circuits have a fixed gain of +1V/V, which means the hold capacitor(s) and parasitic junction capacitance sees the full output signal swing. In the SHC605 the second gain stage attenuates the signal across the capacitors and greatly reduces the nonlinear capacitance. The SHC605's second stage has a unity-gain bandwidth of approximately 250MHz and its open-loop gain rolls off at –20dB/decade. With a 2.5MHz signal, the voltage across the hold capacitors is 100 times less than the output signal, and therefore, the nonlinear capacitance is greatly reduced.

The SHC605's patented architecture provides users with an extremely accurate high-speed *operational* track-and-hold amplifier. All common operational amplifier transfer functions can be realized with the SHC605; i.e. unity-gain, noninverting gain, inverting gain, and differential gain. These configurations are shown in Figures 3 through 6. In many instances, the SHC605 provides a superior single-chip solution to applications previously requiring two or more devices. As with any conventional voltage feedback op amp, it is important to consider tradeoffs between noise, bandwidth, and settling time for these applications. Refer to Discussion of Performance and Typical Performance Curves for more details.

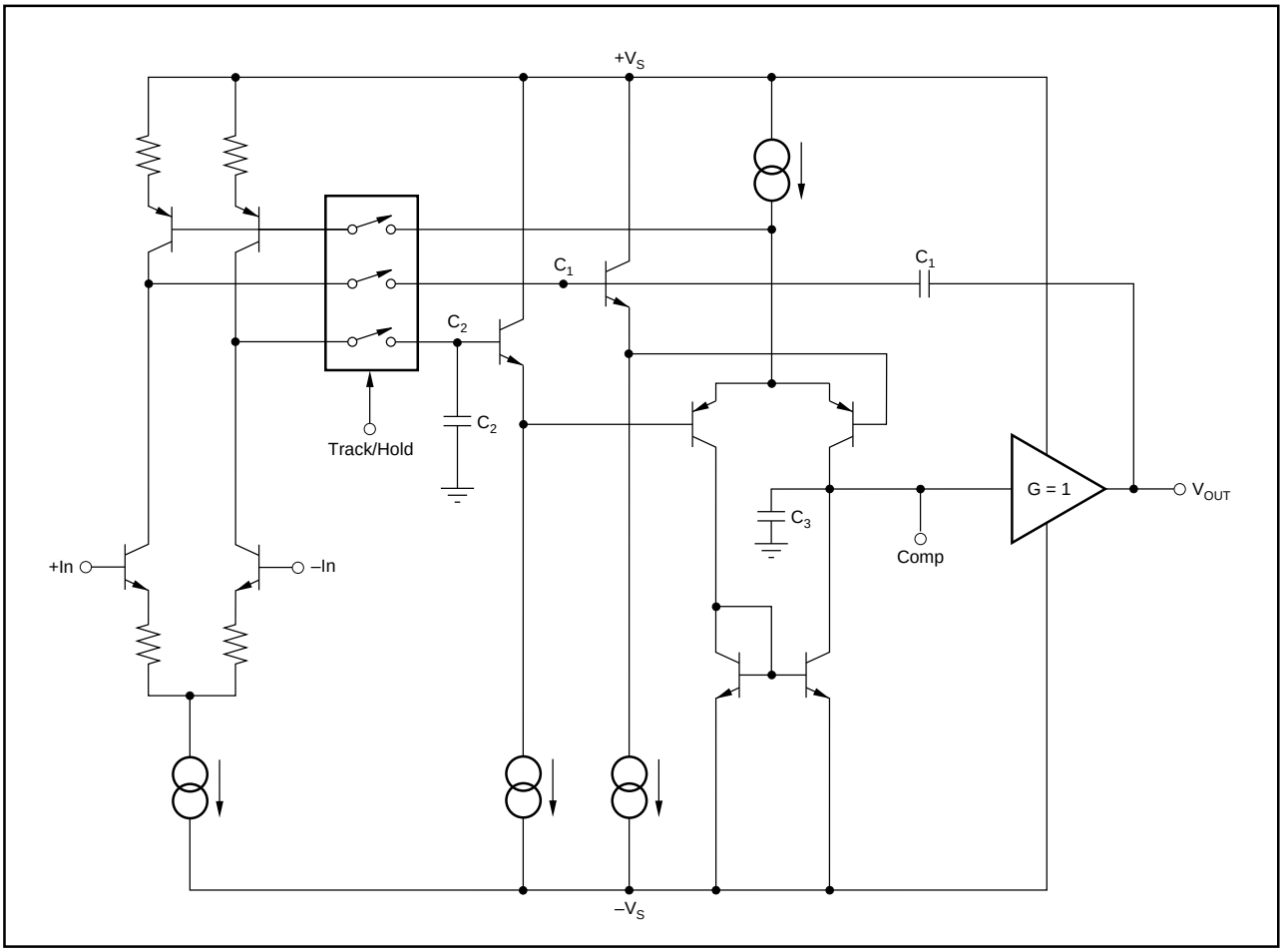


FIGURE 2. SHC605 Simplified Circuit Diagram.

DISCUSSION OF PERFORMANCE

DISTORTION

Hold-mode distortion is an important specification for a track-and-hold amplifier. This is a measure of the accuracy of the amplifier's held output while sampling a sinusoidal input signal. It includes errors from both the switching network and the amplifier's signal path. Hold-mode distortion depends on the input signal's amplitude and frequency as well as the sampling rate. The biggest cause of distortion in the SHC605 is slew-induced nonlinearity; the higher the amplitude of a high frequency input, the higher the distortion. Hold-mode distortion can also result from sampling too fast or not allowing enough acquisition time or track-to-hold settling time. The SHC605 has a typical 0.01% acquisition time of 30ns for a 2V step, and a typical 100µV track-to-hold settling time of 15ns. Thus, for 12-bit accuracy the clock rate should not exceed 22MHz (refer to Typical Performance Curves for details).

NOISE

The SHC605's noise performance is almost completely determined by track-mode noise. This is the noise sampled by the differential hold capacitors during track-mode, which is greater than the noise measured directly at the output. The input referred noise of the SHC605 is 2.5nV/√Hz. For unity-gain this corresponds to an output noise of approximately 35µVrms; which is much lower than the typical 150µVrms noise sampled by the hold capacitors. The track-mode noise sampled by the hold capacitors is independent of closed-loop gain, and therefore, the SHC605 can be used with higher closed-loop gain without degrading the overall noise performance.

The SHC605's noise performance is also affected by hold-mode noise and aperture jitter. Hold-mode noise is the result of current noise reacting with the hold capacitors. This noise accumulates on the capacitors at a rate which is proportional to the square root of the hold time. For sample rates above 1MHz this noise is usually insignificant. Aperture jitter describes the random variation in track-to-hold aperture delay, and causes increased hold-mode noise when high slew rate signals are sampled. A differential ECL clock input will provide lower aperture jitter than a single-ended ECL or TTL clock.

CHOOSING THE BEST ARCHITECTURE

The SHC605 is basically a high-speed operational amplifier which can hold its output on command. Unlike traditional high-speed track-and-hold amplifiers, which have fixed gains of +1V/V, the SHC605 can be used with non-inverting, inverting, or differential gains. In many applications, a single SHC605 can be used to solve a problem that previously required two or more devices.

Figures 3 through 6 show the SHC605 connected for non-inverting, inverting, and differential gains. As with any op amp, it is important to consider performance tradeoffs for all of these configurations. For gains less than ±10, the SHC605's track-to-hold settling, pedestal offset, droop, and total hold-mode noise remains constant. However, small-signal bandwidth and acquisition time will be compromised as the closed-loop gain is increased (refer to the Typical Performance Curves for details).

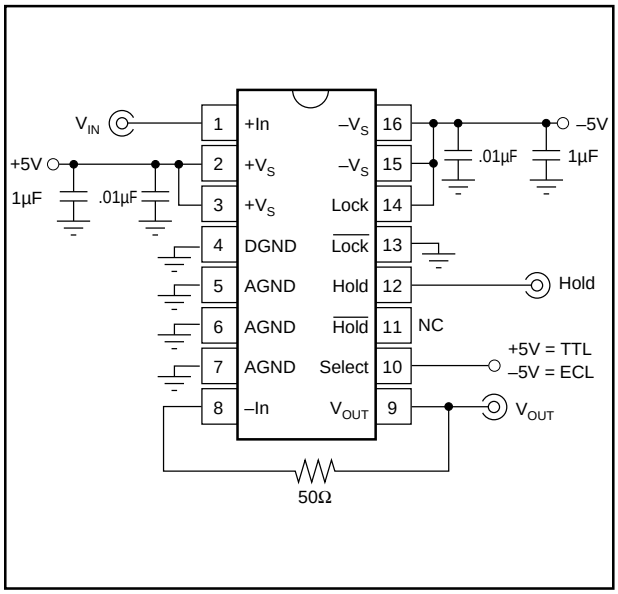


FIGURE 3. Gain of +1 Track-and-Hold Amplifier.

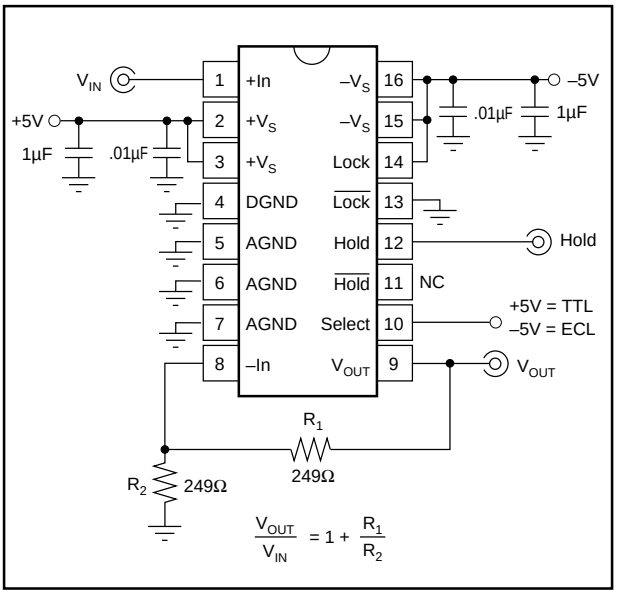


FIGURE 4. Gain of +2 Track-and-Hold Amplifier.

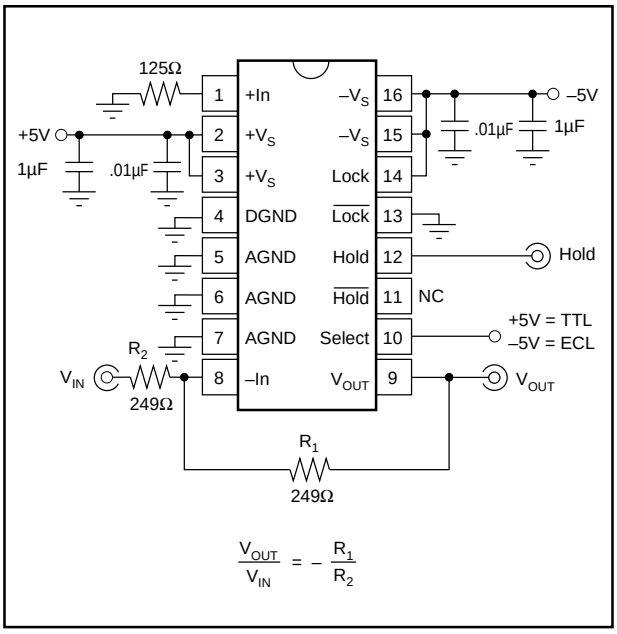


FIGURE 5. Gain of –1 Track-and-Hold Amplifier.

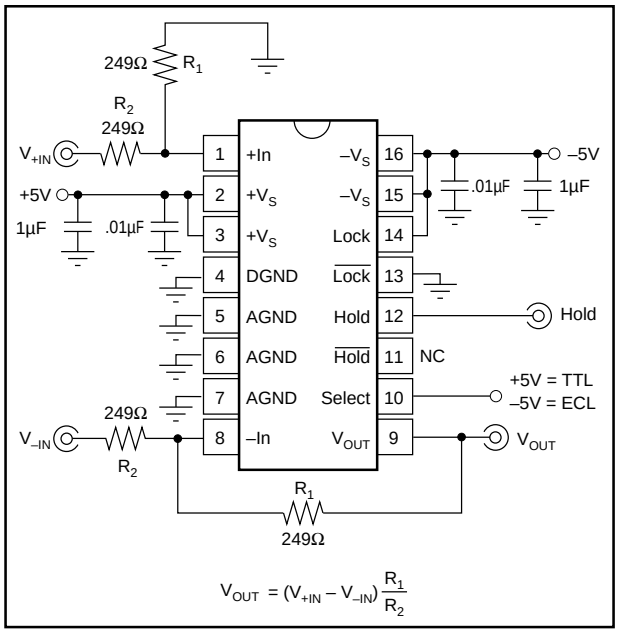


FIGURE 6. Differential Gain of 1 Track-and-Hold Amplifier.

APPLICATIONS INFORMATION

LOGIC COMPATIBILITY/TRACK-TO-HOLD SWITCHING

The SHC605 contains an internal reference circuit which produces either an ECL or TTL logic threshold voltage for single-ended track-to-hold switching. Differential ECL switching is also possible with the SHC605. Table I provides the proper pin connections for all of the possible switching options and the Performance Specifications Table gives the logic levels and input bias currents.

LOGIC TYPE	DGND (Pin 4)	SELECT (Pin 10)	THRESH/$\overline{\text{HOLD}}$ (Pin 11)	HOLD (Pin 12)
Single-ended TTL	GND	+5V	NC	Clock
Single-ended ECL	GND	–5V	NC	Clock
Differential ECL	NC	NC	$\overline{\text{Clock}}$	Clock

TABLE I. Track-to-Hold Switching Options.

LOCKOUT CIRCUITRY

The SHC605 includes additional logic circuitry which allows edge-triggered operation for sampling ADCs. The lockout comparator and Track/Hold comparator form a wired-or mode control circuit as shown in the block diagram on page one. When the Lock input, pin 14, is high with respect to the $\overline{\text{Lock}}$ input, pin 13, the SHC605 is in the Hold-mode regardless of the Hold/$\overline{\text{Hold}}$ inputs. This feature provides more flexibility in the convert command duty cycle and reduces noise resulting from aperture jitter.

Figure 7 shows how the SHC605 lockout circuit can be used with an ECL one-shot to provide an edge-triggered sampling ADC. An ECL threshold voltage is generated on Thresh/$\overline{\text{Hold}}$ (Pin 11), which is connected to $\overline{\text{Lock}}$ (Pin 13), to allow a single-ended lockout input on Lock (Pin 14). The ECL convert command is applied directly to the SHC605. The 10ns delay on the ADCs convert signal is to allow for SHC605 track-to-hold settling. The one-shot's duty cycle

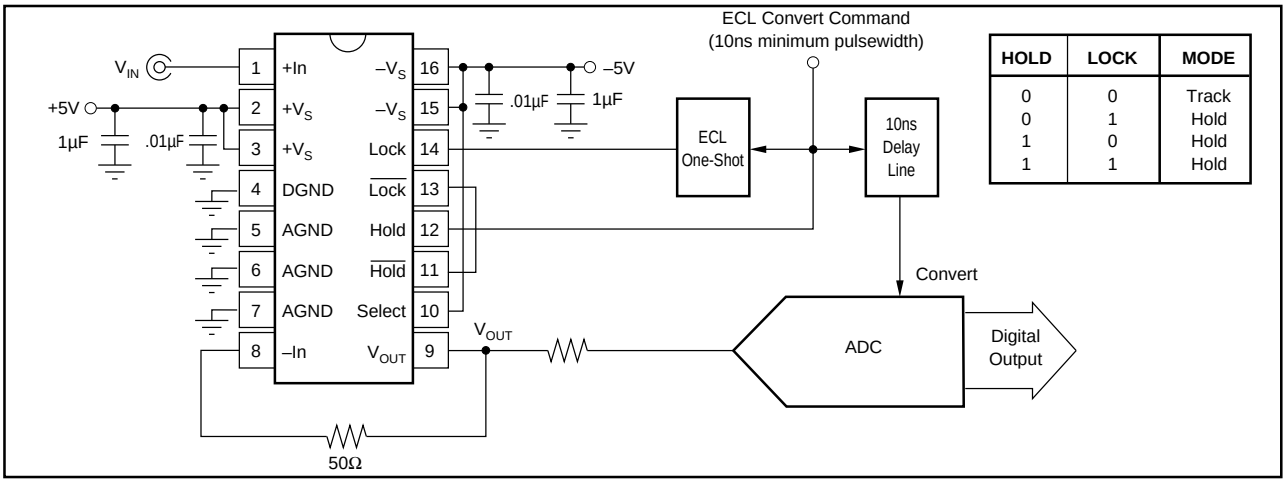


FIGURE 7. Edge-Triggered ADC.

will depend on the ADC conversion time. In this application the one-shot is used to set the critical ADC timing which means the user has more freedom in selecting the convert command duty cycle. Since the convert command is applied directly to the SHC605—instead of after additional logic and clock conditioning—aperture jitter noise is minimized.

OFFSET VOLTAGE ADJUSTMENT

The SHC605's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 8 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input offset voltage errors due to the amplifier's input offset current, which is typically only 0.2µA.

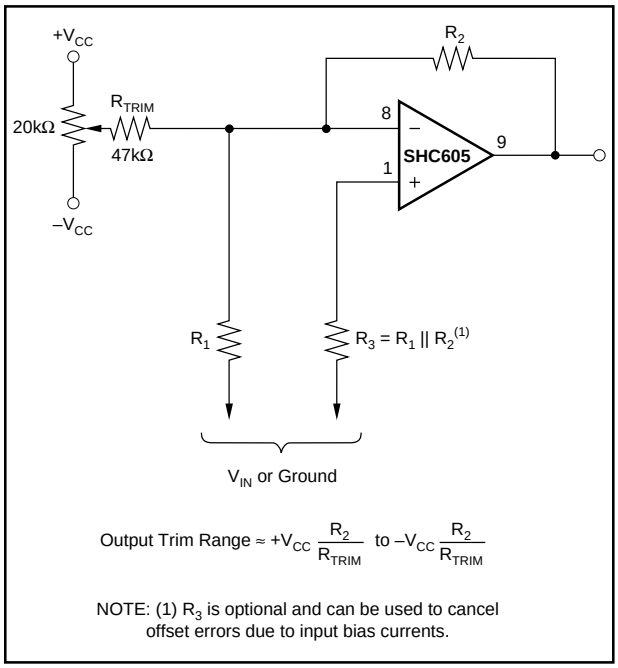


FIGURE 8. Offset Voltage Trim.

INPUT PROTECTION

The SHC605 incorporates on-chip ESD protection diodes as shown in Figure 9. All pins on the SHC605 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability diode current should be externally limited to 10mA or so whenever possible. Static damage can cause subtle changes in SHC605 input characteristics without necessarily destroying the device. In precision track-and-hold amplifiers, this may cause a noticeable degradation in performance. Therefore, static protection is recommended when handling the SHC605.

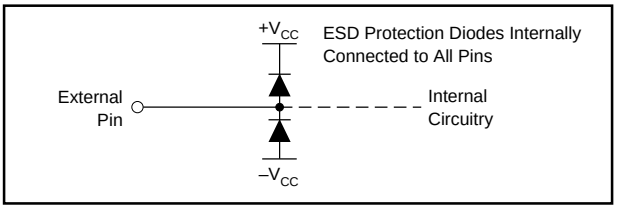


FIGURE 9. Internal ESD Protection.

LAYOUT AND BYPASSING

For best performance, good high speed design techniques must be applied. The component (top) side ground plane should be as large as possible and continuous (not fragmented). Two ounce copper cladding is recommended.

All traces should be as short as possible, especially the output. As much of the ground plane as possible should be removed from around the +In, –In, and V_{OUT} pins to reduce parasitic capacitance and minimize coupling onto the analog signal path.

Power supply decoupling capacitors must be used as shown in Figures 3 through 6. The 0.01µF capacitors should be low inductance surface mount devices and should be connected as close to the SHC605 ±Vs leads as possible (within 30 mils). The 1µF low frequency bypass capacitors should be tantalum capacitors (preferably surface mount) and should be located within one inch of the SHC605. Surface mount resistors are also recommended and should be placed as close to the SHC605 as possible to minimize inductance.

CAPACITIVE LOADS

The SHC605's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be buffered by connecting a small resistance, usually 20Ω to 50Ω, in series with the output as shown in

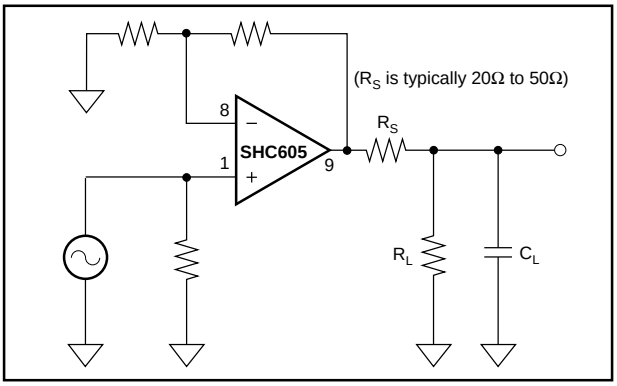


FIGURE 10. Driving Capacitance Load.

Figure 10. This is particularly important when driving high capacitance loads such as flash A/D converters.

The series resistor, R_S, should be connected as close to the SHC605 as possible. If R_S causes excessive output attenuation, add closed-loop gain to the SHC605 as shown in Figures 4 through 6.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coaxial cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

APPLICATIONS

The SHC605's combination of high speed and accuracy, small size, and low price makes it ideally suited for many data acquisition applications. Its versatile operational amplifier architecture and switching flexibility provides users with an extremely reliable single-chip solution to problems that previously required several components. Figures 11 through 16 show many application circuits using the SHC605. These include high-speed flash and sub-ranging ADC driving, multi-channel simultaneous sampling, DAC deglitching, and peak detecting.

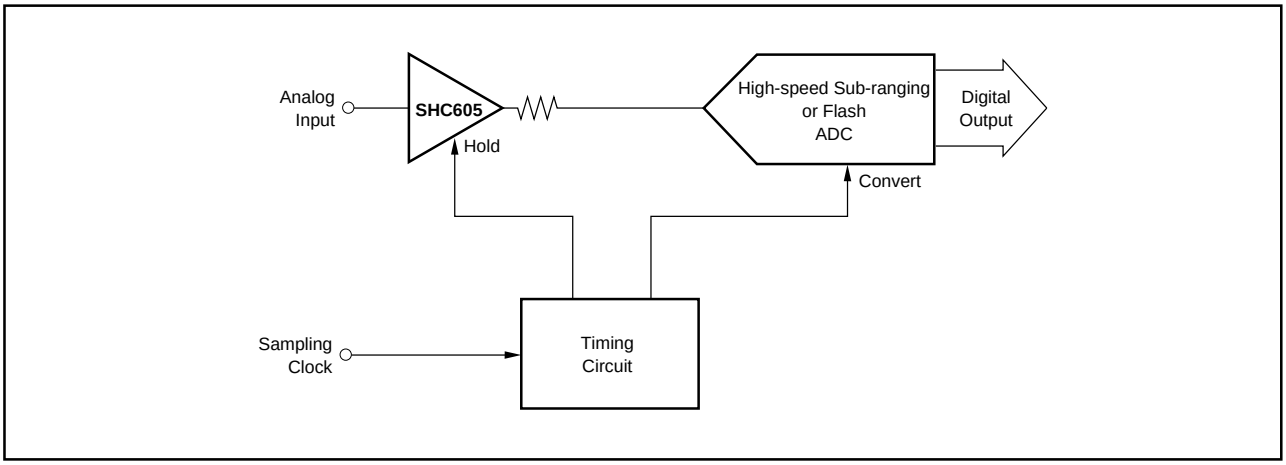


FIGURE 11. Sampling ADC.

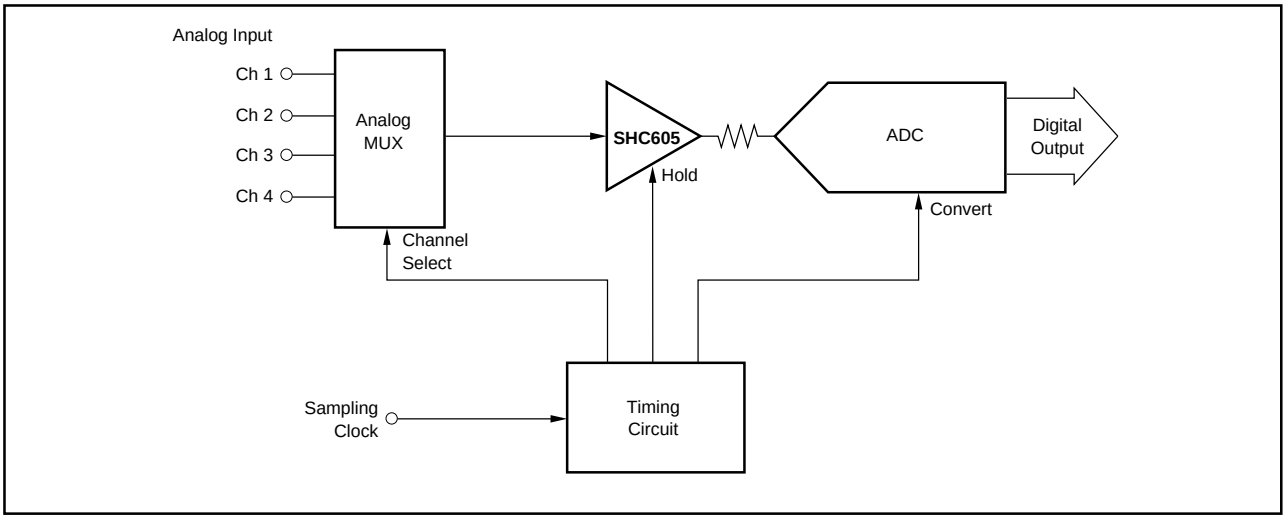


FIGURE 12. Traditional Data Acquisition System.

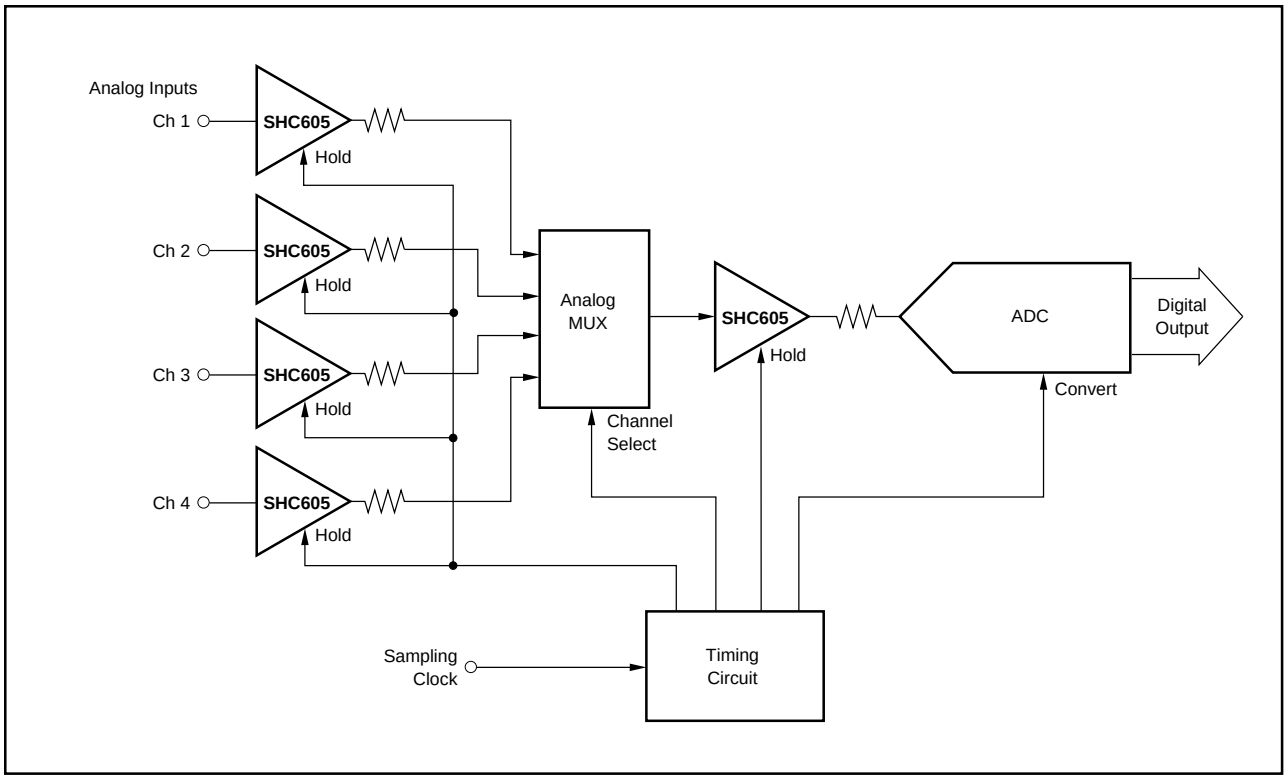


FIGURE 13. Multi-Channel Simultaneous Sampling System.

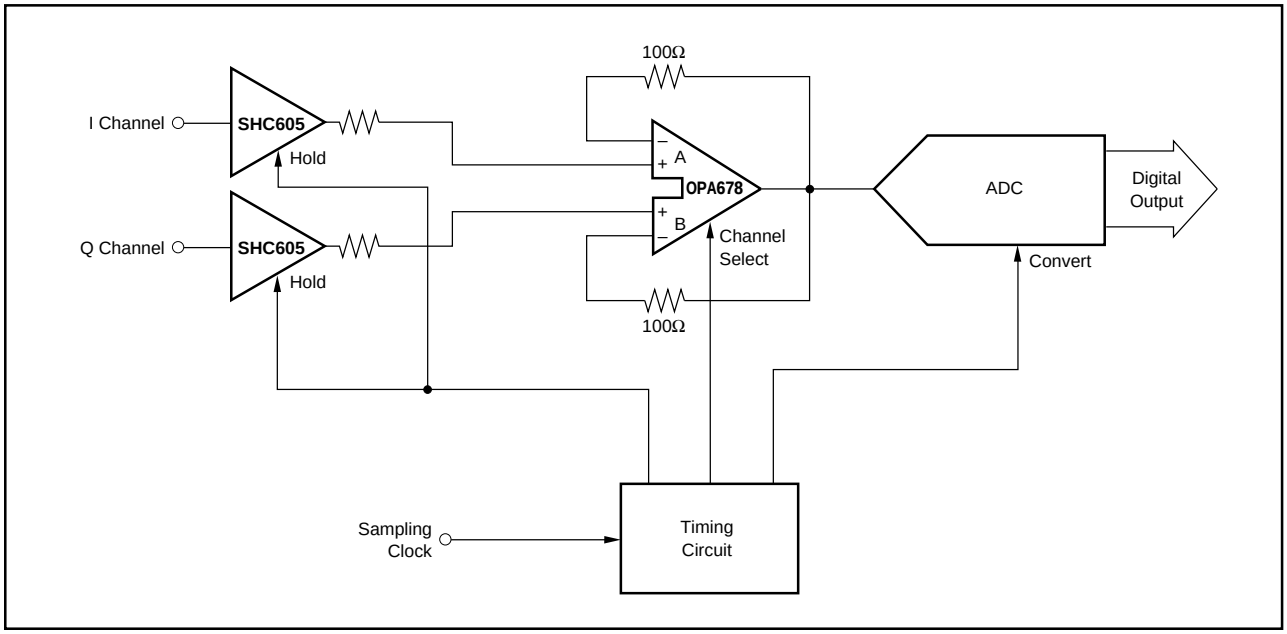


FIGURE 14. I/Q Channel Simultaneous Sampling.

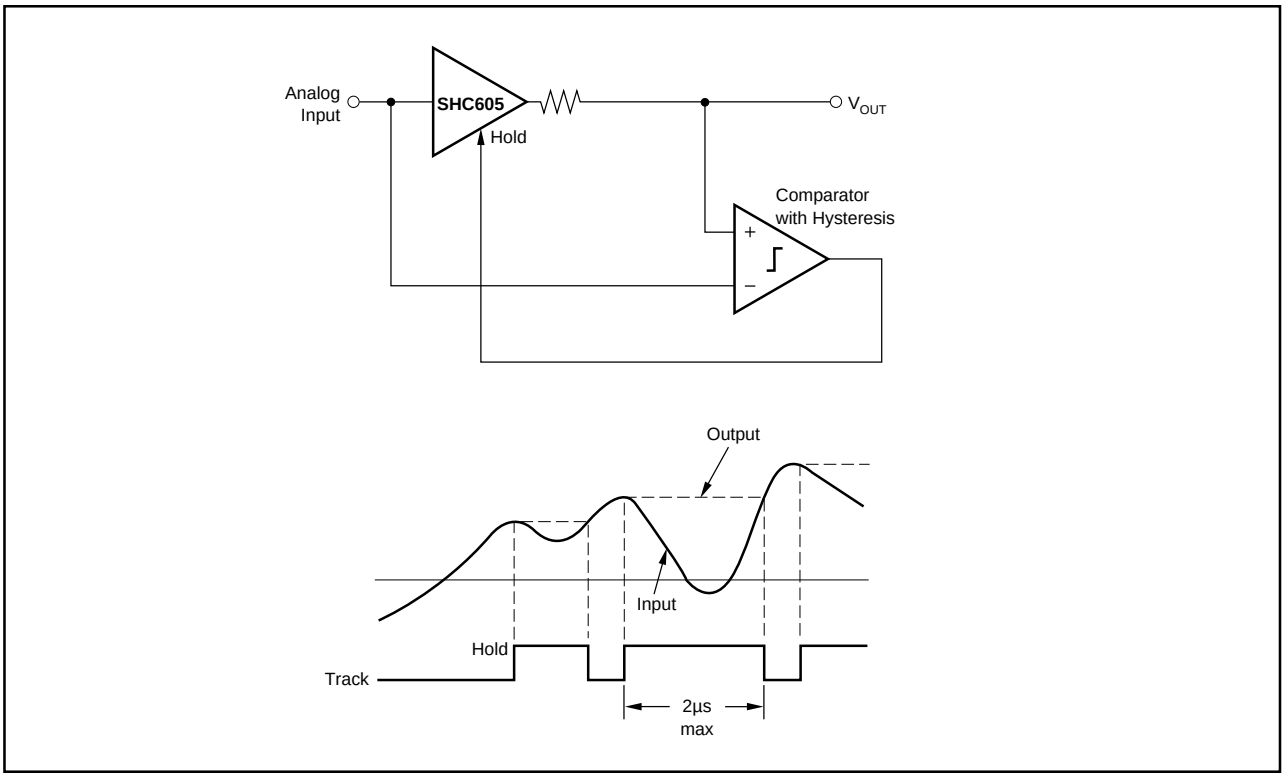


FIGURE 15. High-Speed Peak Detector.

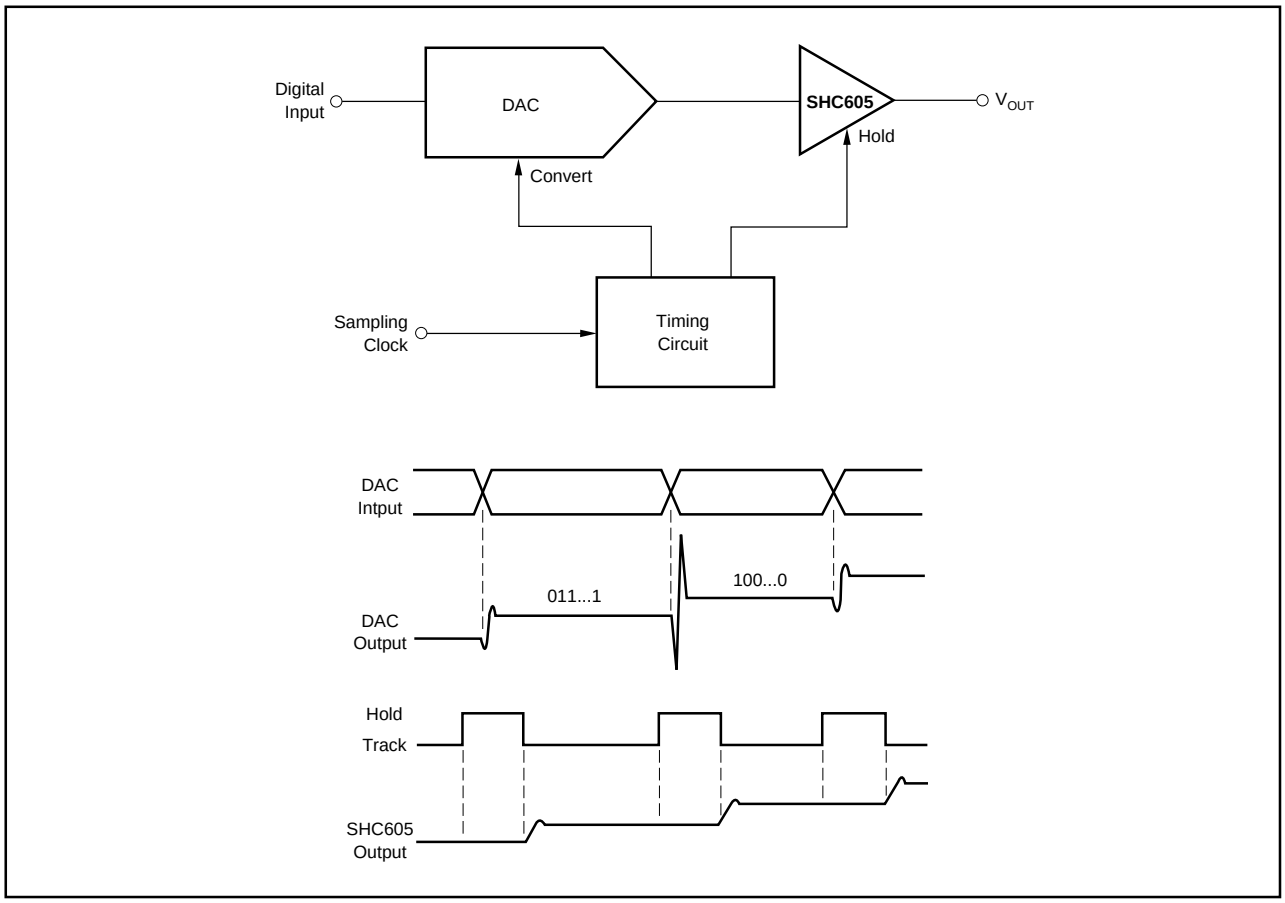
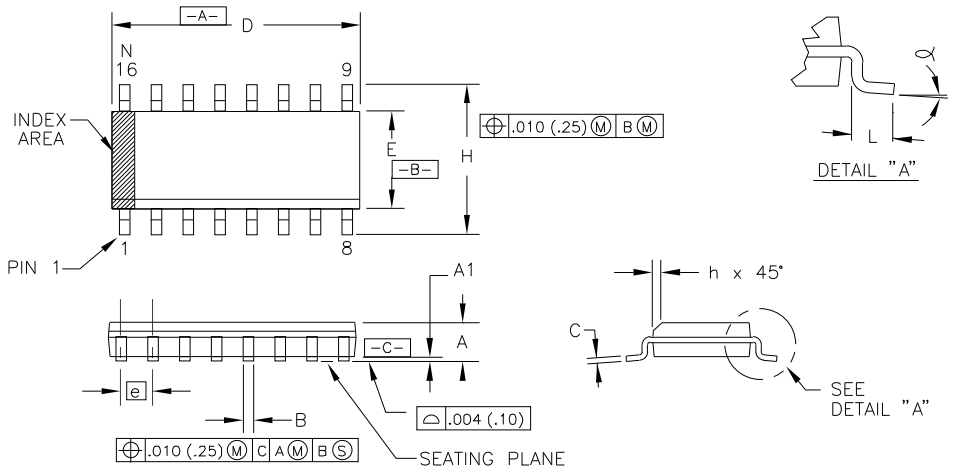


FIGURE 16. DAC Deglitcher.

PACKAGE DRAWING

Package Number 265 - 16-Lead SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.25	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.19	0.25	
D	.3859	.3937	9.80	10.00	2
E	.1497	.1574	3.80	4.00	3
e	.050 BASIC		1.27 BASIC		
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	4
L	.016	.050	0.40	1.27	5
N	16		16		6
∝	0°	8°	0°	8°	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS–HATCHED AREA.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ265	REV.: C
JEDEC NUMBER: MS–012–AC	