ITT SEMICONDUCTORS

SEVEN STAGE FREQUENCY DIVIDER

Monolithic integrated circuit in bipolar technique, designed primarily for use in electronic organs. The device incorporates seven flip-flops with externally accessible inputs and outputs.

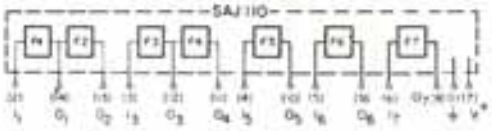
Each flip-flop changes state on application of a positive-going input pulse. The individual flip-flops can be interconnected to form a divider chain. Two flip-flop pairs are already internally series-connected as shown in Fig. 2.

An emitter-follower is interposed between each flip-flop and the associated output terminal to ensure that the output voltage is largely independent of load. Because no internal emitter resistors are provided, the emitter-follower delivers undirectional output currents.

When used in electronic organs the frequency divider SAJ110 may be driven by sine-wave as well as square-wave signals. The shape of the square-wave output signal can be modified by connection of RC filters.

If, by means of an appropriate circuit, all inputs and outputs are brought to a potential below 1.5 volts for a short time, all outputs remain in the low state.

Fig. 2: Block Diagram



The figures in brackets correspond to the pin numbers.

All voltages are referred to terminal 1.

Normally, the SAJ110 is delivered in the dual-in-line plastic package TO-116 (Fig. 1a, add suffix "A" to type No.). Upon special request it is also available in the quad-in-line package (Fig. 1b, add suffix "B" to type No.).

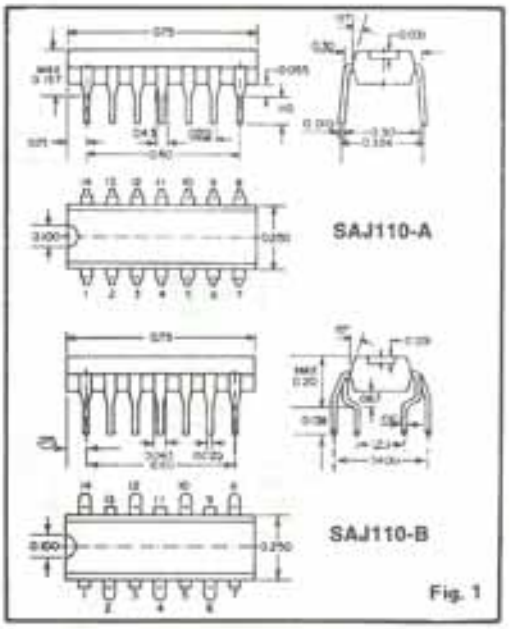


Fig. 1

ABSOLUTE MAXIMUM RATINGS

	Characteristic	Unit
V_t	Supply voltage	11 V
	Input voltage see Fig. 4	
I_{th}	Output current per stage	5 mA*
V_{ext}	External voltage at output terminals	+5V
T_{amb}	Ambient temperature range	−10 to +60°C
T_s	Storage temperature range	−30 to +125°C

CHARACTERISTICS PER DIVIDER STAGE

at V_t = 9 V, R_L = 2.2 kΩ, T_{amb} = 25°C

	Characteristic	Unit
I	Supply current (low state at output)	<3 mA
V_i	Input voltage high state (see Fig. 4)	6 to 9 V
V_i	Input voltage low state	<1 V
V_o	Output voltage low state	<0.1 V
V_o	Output voltage high state	>7.0 V
t_r	Rise time of output voltage	<0.2 us
t_f	Fall time of output voltage	<0.2 us
r_i	Input resistance (see Fig. 5)	6 to 9 kΩ

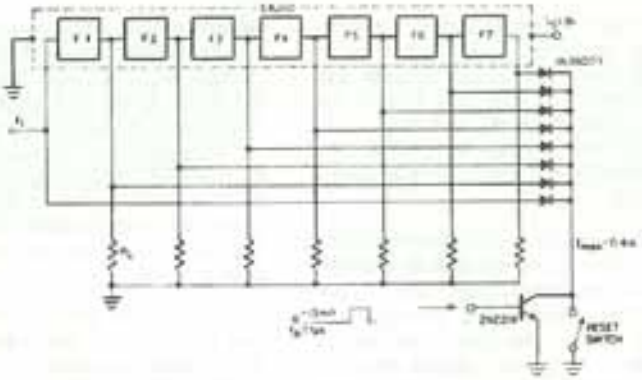
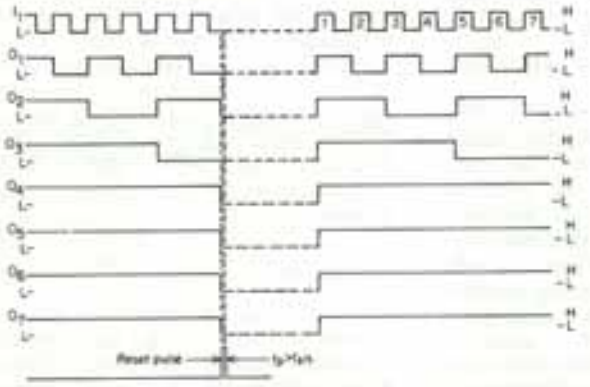


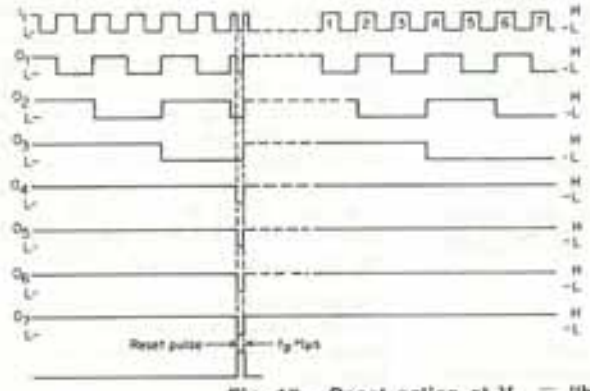
Fig. 13—Reset circuit for a seven stage counter



TRUTH TABLE

I_1	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	L	L	L	L	L	L	L
1	H	H	H	H	H	H	H
2	L	H	H	H	H	H	H
3	H	L	H	H	H	H	H
4	L	L	H	H	H	H	H
5	H	H	L	H	H	H	H
6	L	H	L	H	H	H	H
7	H	L	L	H	H	H	H

Fig. 14—Reset action at V_{I_1} = "low"



TRUTH TABLE

I_1	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	H	H	H	H	H	H	H
1	L	H	H	H	H	H	H
2	H	L	H	H	H	H	H
3	L	L	H	H	H	H	H
4	H	H	L	H	H	H	H
5	L	H	L	H	H	H	H
6	H	L	L	H	H	H	H
7	L	L	L	H	H	H	H

Fig. 15—Reset action at V_{I_1} = "high"

ITT SAJ110
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CHARACTERISTICS PER DIVIDER STAGE

at $V_t = 9$ V, $R_L = 2.2$ kΩ, $T_{amb} = 25°C$

r_s	Output resistance low state	>1 MΩ
r_s	Output resistance high state	200 Ω

Recommended Operating Conditions

V_t	Supply voltage	9 V
f_{max}	Max input frequency	50 kHz
R_L	Load resistance	2 to 20 kΩ

Fig. 3 — Output voltage versus supply voltage.

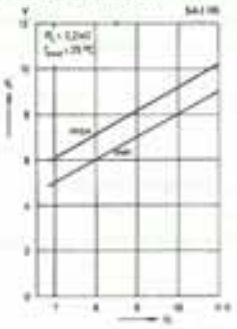


Fig. 4 — Max. admissible and min. required value of input pulses (high state) versus supply voltage.

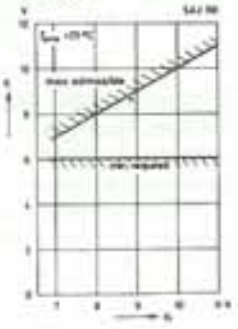


Fig. 5 — Input characteristic

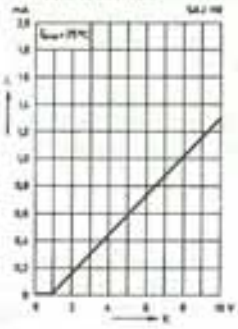
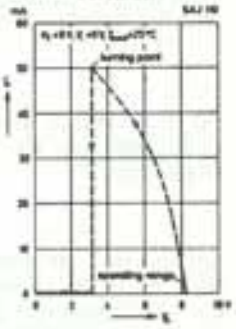


Fig. 6 — Output characteristic



ITT SAJ110 IN FREQUENCY DIVIDER CIRCUITS

Introduction

Integrated digital frequency dividers have for long been widely used in professional digital equipment but have so far found little application in the entertainment sector of the electronic industry. This, no doubt, is due to the fact that the devices presently available do not quite meet the specific requirements of the consumer market, and that they were, until recently, rather expensive. Advances in integration techniques have now made it possible to produce inexpensive linear, as well as digital integrated circuits which should be of special interest to the electronic consumer industry. These devices offer many advantages when compared with circuits employing dicrete components and are in many instances already cheaper. It is certain that the availability of these new integrated circuits will lead to rapid new developments in all branches of the electronic industry.

The new monolithic integrated frequency divider circuit SAJ110, developed by ITT Semiconductors, incorporates seven divider stages which can be used either individually or interconnected to form a divider chain. Because the SAJ110 requires no additional components and can be used in place of conventional discrete-component flipflop dividers, its use as a frequency divider in electronic organs is particularly advantageous.

The Integrated Circuit SAJ110

Integration of a conventional flipflop circuit would offer virtually no advantage over a discrete component circuit — only a circuit which does not incorporate capacitors or other charge-storing elements is suitable for integration. Because the master slave flipflop (a frequency divider often used in digital equipment) is far too complex for consumer applications,

A-B being the normal operating range. As mentioned previously, in order to initiate a reset it is necessary to force the output through the range B-C to point "C", and this should be effected in the shortest time possible (t_r < 0.1msec) to avoid overheating the device (the output transistor dissipates considerable power during this period).

If the divider input potential is higher than OV, then the trigger point C is shifted to the left on the curve, which means that the output potential would then have to be pulled down to a level below 1.5V. If the input and output of a divider stage or if several inputs and outputs of a divider chain are to be pulled down to a low potential together, then this potential should be less than 1.5V to ensure that the circuits reset reliably under any condition (refer to Fig. 13).

Reset Circuit.

Fig. 13 outlines a reset circuit suitable for a seven stage counting chain. All the output points as well as the input point I are connected, via isolating diodes, to the collector of a switching transistor type 2N2218, or alternatively to a RESET switch. It is important that the transistor collector voltage drops to a saturation level of less than 0.6V for the duration of the reset pulse, and that the transistor is capable of passing up to 400 mA of collector current under the most unfavorable conditions (i.e. when all outputs are in "high" condition prior to the application of a reset pulse). The pulse source must therefore be capable of supplying at lease approximately 15mA to the base of the 2N2218 so that the requirement $V_{I1}=V_{O1}=\ldots V_{CC}>1.5V$ is fulfilled. The reset pulse duration is, however, not very critical provided it is not less than approximately 1μsec.

As mentioned previously, the output state of all the stages depends on the input state of the first stage immediately after the occurrence of the reset pulse. There are two possible conditions:

V_{I1} = "low" (Fig. 14)
V_{I1} = "high" (Fig. 15)

In Fig. 14 I_1 was "low" at the instant when the reset was applied; under this condition all the outputs which were in the "high" state immediately before application of the reset pulse change to "low" and maintain this state after the reset pulse has been removed. The next input pulse to I_1 then causes all the outputs to be triggered to "high", this corresponding to a "PRESET" condition of the counter. Only the second input pulse is counted. These conditions are summarized in the truth table in Fig. 14 and it can be seen that the counter counts (n-1).

Fig. 15, on the other hand, illustrates a condition in which all the outputs are in the "PRESET" state immediately after the occurrence of the reset pulse so that the next pulse is correctly counted as No. 1. The explanation for this is as follows: Although in this case the reset pulse initially pulls all the outputs, as well as the input I_1, to "low", the input I_1 is immediately returned to "high" at the end of the pulse ($t = t_r$), because the positive edge at the end of the pulse is equivalent to the application of a logic "H" to the input. This positive edge triggers first output O_1 and then, in turn, all the other outputs to "high" — this corresponding to the "PRESET" state of the counter.

Conclusion

The SAJ110 is an inexpensive seven-stage frequency divider which, in comparison with equivalent discrete-component circuits, offers many advantages, the most important ones being: small size and low wiring and assembly cost. The device, because of its electrical characteristics, is particularly suitable for use in electronic organs where its performance is superior to that of discrete component flipflops. Being insensitive to the waveform of the input signal, the SAJ110 will accept a square wave as well as other types of waveforms (e.g. sinusoids; moreover, the low output impedance ensures that the output remains virtually constant irrespective of load, the lowest permissible load being approximately 2kΩ. At maximum loading the output amplitude is only 1.5V less than supply voltage.

The generation of output waveforms which are very similar to, and possess virtually the same frequency spectrum as, that of an ideal sawtooth, is possible simply by connection of RC networks across the outputs.

development of a new circuit was necessary. This circuit had to function in a similar manner to a conventional flipflop but had to be designed so that no additional charge-storing elements were required. The result is a device which combines seven single divider stages on a single chip.

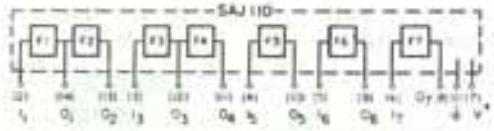


Fig. 7 — SAJ110 Block diagram — The figures in brackets are the same as the pin numbers of package.

In order to make maximum use of the 14 connections available on a TO-116 package the pins are connected as shown in Fig. 1, being arranged so that access to two divider pairs and three single divider stages is possible. The circuits can thus be used either singly or interconnected in various combinations.

Functional Description of an SAJ110 Divider Stage

Each stage used in the SAJ110 comprises basically a trigger network, two transistors connected as a flipflop, and an output stage (Fig. 8). The input is first applied to a trigger network which always steers the input pulse to that transistor which is cut off at the time. Fig. 8 shows the input and output waveforms produced by one such stage. Each positive edge of the input waveform causes the flipflop to change state so that frequency division by two results. The flipflop output is fed to a transistor connected as an emitter follower output stage, this being provided to isolate the flipflop from an external load and to supply output pulses of constant amplitude. The output pin is connected to the emitter of this transistor.

Performance Requirement Summary for the Integrated Frequency Divider SAJ110

The integrated frequency divider had to meet the following customer requirements:

Supply voltage ..... 7 - 11 V
Input (trigger waveforms) ..... Sinusoid or square wave
Output voltage ..... Not less than 6V — high enough to permit reliable triggering of another divider stage under all operating conditions.
Permissible load range ..... 2k to 100kΩ
Ambient operating temperature range ..... 0° to 60°C
Number of stages to be accommodated in one package 7
Packaging . 14-pin DIP or QIL plastic package

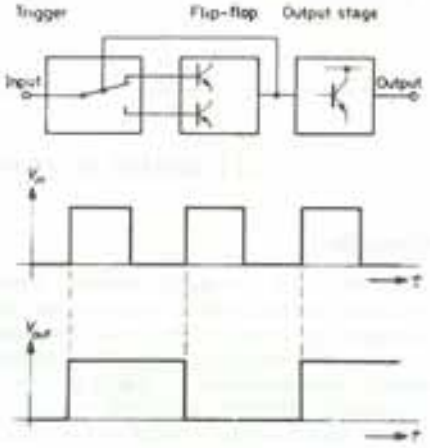


Fig. 8 — Block diagram of one divider stage with input and output waveforms

For reason of economy and reliability, it was also considered desirable that the number of integrated elements and the total resistance of all the resistors used in the IC should be kept to a minimum.

In Fig. 12 the frequency spectrum of the waveform V_{R1} is compared with that of two sawtooth waveforms, and it can be seen that the spectrum attained with the circuit arrangement of Fig. 10 approaches that of an ideal sawtooth. Note that the sub-harmonic component is extremely small — much smaller than is necessary for this application.

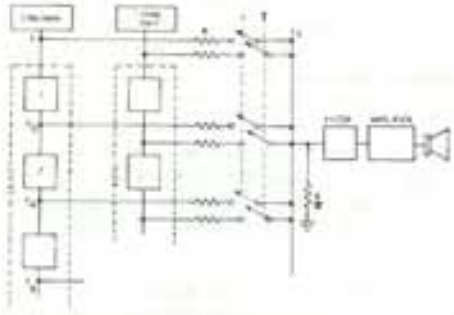


Fig. 9—Block diagram of the tone generating circuits in electronic organs

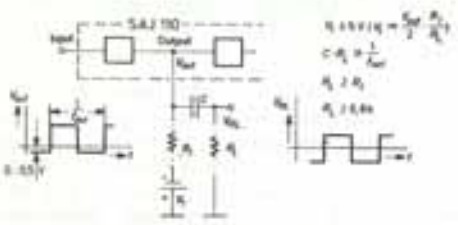


Fig. 10-Conversion of divider undirectional output into alternating output

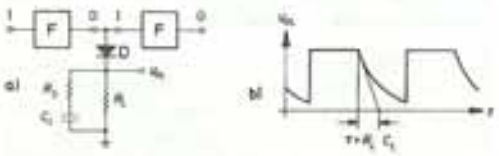


Fig. 11—Modification of the divider frequency spectrum using RC networks

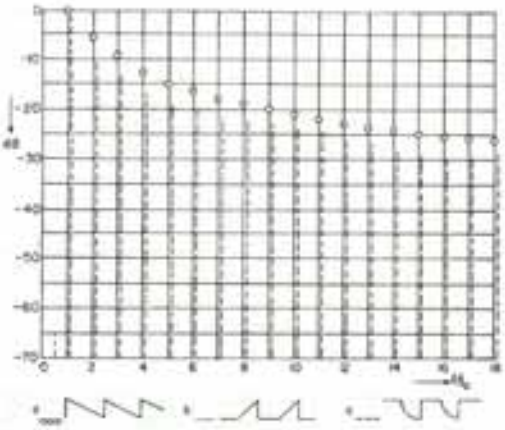


Fig. 12 —Frequency spectrum associated with various waveforms

Use of the SAJ110 in Counting Circuits

Use of the SAJ110 in a counting circuit raises the problem of how to reset the flipflops. With the SAJ110 it is possible to reset a single stage as well as several stages connected in a counting chain. However, when designing a suitable reset circuit the following features of the device must be taken into account:

The output of a divider stage can change state only while its input is positive going.

The frequency divider SAJ110, unlike a master slave flipflop, does not possess a buffer stage between input and output, nor a special reset input.

It is, however, possible to use the inputs and outputs for reset purpose. Because the reset capability of an SAJ110 stage depends on its input state, it is necessary to use both the input and the output terminals for reset purpose.

Output Characteristic

Referring to the output characteristic of a single stage (Fig. 6) it can be seen that a "high" output can only be flipped to ""low" if the output is pulled down to 1.5V or less by some external means, and this can only be accomplished while the input voltage V_{in} is "low". The output characteristic in Fig. 6 is divided into the sections A-B and B-C, section

The curves shown in Figs. 3 to 6 illustrate the performance of the divider in more detail.

The input parameters of a frequency divider stage at various supply voltages can be deduced from Figs. 3 and 4. The input pulse amplitude should be not less than 6V, but should, on the other hand, not exceed the supply voltage. The curves in Fig. 3 give the maximum permissible input pulse amplitude range as a function of supply voltage. The input corresponding to "low" level should be less than 1V. Fig. 4 may be used to determine the static input resistance, which varies between 6 and 9kΩ.

In the curve shown in Fig. 5 the output voltage is plotted as a function of supply voltage. As can be seen, the output voltage is 1 to 1.5V lower than the supply voltage and varies somewhat with the load. Assuming the same loading conditions the output voltages of all individual stages are within ±5% — this applies to stages on the same IC as well as to stages on different IC's.

Fig. 6 shows the loading characteristic of a divider stage which gives a "high" output. Note that as the output current of the stage is increased (by reducing the load resistor, for example), point "B" on the curve moves towards "C" (I_{out} = 35 mA and V_{out} = 1.7V) at which point the stage flips into the "low" state and remains there. This bistable output effect is discussed further on in connection with the resetting of dividers used in counting circuits.

Applications for the SAJ110

Use in Electronic Organs

The heart of modern electronic organs is usually a set of LC master oscillators tuned to the frequencies of the highest octave. The frequencies of the lower octaves are then derived from these master oscillators by frequency division. In most conventional organs this frequency division is accomplished by the use of bistable multivibrators (flip-flops). These have the disadvantage of producing a square wave output, which contains practically no even harmonics and offers only limited scope for modifying the character of the notes produced.

However, if the SAJ110 is used, simple RC networks can be connected across the outputs to generate sawtooth waveforms which contain even harmonics. An additional advantage of the SAJ110 is its small size, making it particularly suitable for use in portable instruments.

Fig. 9 shows the usual frequency generating circuits employed in electronic organs. Twelve master oscillators produce the frequencies of the highest octave while all the frequencies for the lower octaves are generated by frequency division. The arrangement shown in Fig. 9 requires up to twelve SAJ110 circuits for one organ. If the organ has less than seven octaves, then there are several spare divider stages which may be utilized in the divider chains associated with other frequencies so that in this case less than 12 integrated circuits are required.

Depression of one of the organ keys, T, causes several outputs to be switched to a common line, S, via high value resistors, R, and this signal, which is a combination of several frequencies, is then further processed. The spectrum of this signal is considerably richer in harmonics than that of an ordinary square wave.

It is an advantage to give a signal to the following filters the mean value of which does little change when the organ keys are pressed. In order to obtain this, the ground of resistor R/10 (Fig. 9) should be connected to a positive potential. Another possibility is to ensure that the divider outputs supply proper AC signals. Fig.10 shows such an alternative circuit. Use of a suitable bias causes the full alternating divider output component to be developed across the load R_L.

The circuit shown in Fig. 11 fully exploits the high output voltage and low output resistance of the frequency divider SAJ110. In this circuit RC networks are connected, via protection diodes, to the outputs of individual divider stages so that waveforms which are not very different from that of an ideal sawtooth are presented across the load R_L. The protective resistor R_s connected in series with each capacitor C_L is included to limit the capacitor surge to a value which the output stage can safely handle.