BURR-BROWN®

REF102

Precision VOLTAGE REFERENCE

FEATURES

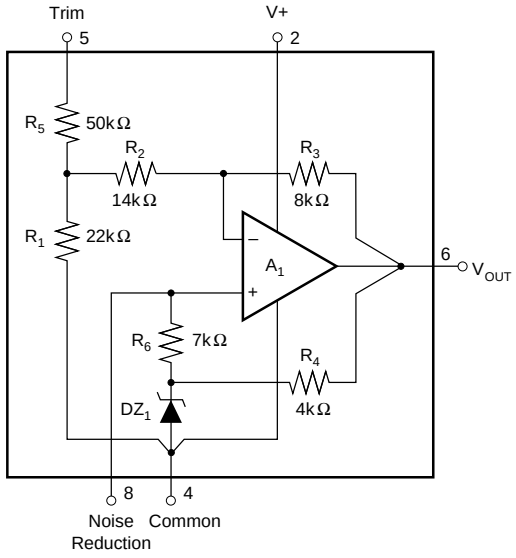
- +10V ±0.0025V OUTPUT
- VERY LOW DRIFT: 2.5ppm/°C max
- EXCELLENT STABILITY: 5ppm/1000hr typ
- EXCELLENT LINE REGULATION: 1ppm/V max
- EXCELLENT LOAD REGULATION: 10ppm/mA max
- LOW NOISE: 5μVp-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE: 11.4VDC to 36VDC
- LOW QUIESCENT CURRENT: 1.4mA max
- PACKAGE OPTIONS: HERMETIC TO-99, PLASTIC DIP, SOIC

APPLICATIONS

- PRECISION-CALIBRATED VOLTAGE STANDARD
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT
- PC-BASED INSTRUMENTATION

DESCRIPTION

The REF102 is a precision 10V voltage reference. The drift is laser-trimmed to 2.5ppm/°C max (CM grade) over the industrial temperature range and 5ppm/°C max (SM grade) over the military temperature range. The REF102 achieves its precision without a heater. This results in low power, fast warm-up, excellent stability, and low noise. The output voltage is extremely insensitive to both line and load variations and can be externally adjusted with minimal effect on drift and stability. Single supply operation from 11.4V to 36V and excellent overall specifications make the REF102 an ideal choice for demanding instrumentation and system reference applications.



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Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and V_S = +15V power supply unless otherwise noted.

PARAMETER	CONDITIONS	REF102A, R			REF102B, S			REF102C, M			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT VOLTAGE											
Initial	T_A = 25°C	9.99		10.01	9.995		10.005	9.9975		10.0025	V
vs Temperature [1]				10			5			2.5	ppm/°C
vs Supply											
(Line Regulation)	V_S = 11.4V to 36V			2			1			1	ppm/V
vs Output Current											
(Load Regulation)	I_L = 0mA to +10mA			20			10			10	ppm/mA
	I_L = 0mA to –5mA			40			20			20	ppm/mA
vs Time	T_A = 25°										
M Package			5			*			*		ppm/1000hr
P, U Packages [2]			20			*					ppm/1000hr
Trim Range [3]		±3			*			*			%
Capacitive Load, max			1000			*			*		pF
NOISE	(0.1Hz to 10Hz)		5			*			*		µVp-p
OUTPUT CURRENT		+10, –5			*			*			mA
INPUT VOLTAGE RANGE		+11.4		+36	*		*	*		*	V
QUIESCENT CURRENT	(I_{OUT} = 0)			+1.4			*			*	mA
WARM-UP TIME [4]	(To 0.1%)		15			*			*		µs
TEMPERATURE RANGE											
Specification											
REF102A, B, C		–25		+85	*		*	*		*	°C
REF102R, S		–55		+125	*		*				°C

*Specifications same as REF102A/R.

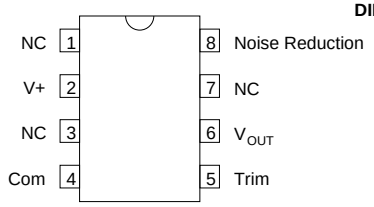
NOTES: (1) The "box" method is used to specify output voltage drift vs temperature. See the Discussion of Performance section. (2) Typically 5ppm/1000hrs after 168hr powered stabilization. (3) Trimming the offset voltage affects drift slightly. See Installation and Operating Instructions for details. (4) With noise reduction pin floating. See Typical Performance Curves for details.

ORDERING INFORMATION

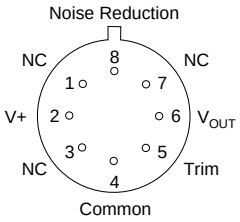
MODEL	PACKAGE	TEMPERATURE RANGE	MAX INITIAL ERROR (mV)	MAX DRIFT (ppm/°C)
REF102AU	8-Pin SOIC	–25°C to +85°C	±10	±10
REF102AP	8-Pin Plastic DIP	–25°C to +85°C	±10	±10
REF102BP	8-Pin Plastic DIP	–25°C to +85°C	±5	±5
REF102AM	Metal TO-99	–25°C to +85°C	±10	±10
REF102BM	Metal TO-99	–25°C to +85°C	±5	±5
REF102CM	Metal TO-99	–25°C to +85°C	±2.5	±2.5
REF102RM	Metal TO-99	–55°C to +125°C	±10	±10
REF102SM	Metal TO-99	–55°C to +125°C	±5	±5

PIN CONFIGURATIONS

Top View **DIP/SOIC**



Top View **TO-99**



ABSOLUTE MAXIMUM RATINGS

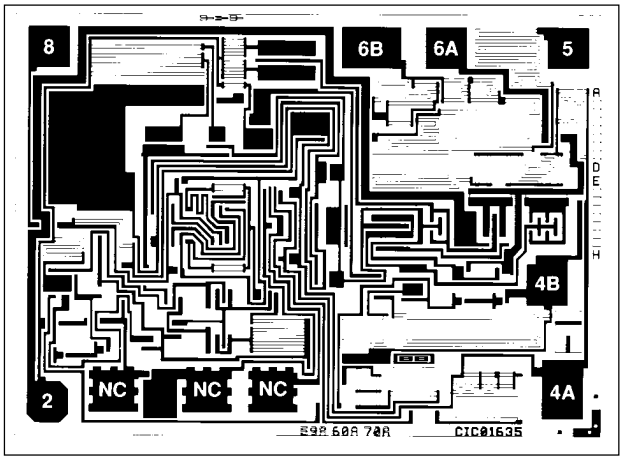
Input Voltage ..... +40V
Operating Temperature
P,U ..... –25°C to +85°C
M ..... –55°C to +125°C
Storage Temperature Range
P,U ..... –40°C to +85°C
M ..... –65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
(SOIC, 3s) ..... +260°C
Short-Circuit Protection to Common or V+ ..... Continuous

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
REF102AU	8-Pin SOIC	182
REF102AP	8-Pin Plastic DIP	006
REF102BP	8-Pin Plastic DIP	006
REF102AM	Metal-TO-99	001
REF102BM	Metal-TO-99	001
REF102CM	Metal-TO-99	001
REF102RM	Metal-TO-99	001
REF102SM	Metal-TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DICE INFORMATION



REF102 DIE TOPOGRAPHY

PAD	FUNCTION
2	V_{CC}
3A	NC
3B	NC
3C	NC
4A	Common (Sense)
4B	Common (Force)
5	Trim
6A	V_{OUT}
6B	V_{OUT} (Feedback)
8	Noise Reduction

Substrate Bias: $-V_{CC}$.

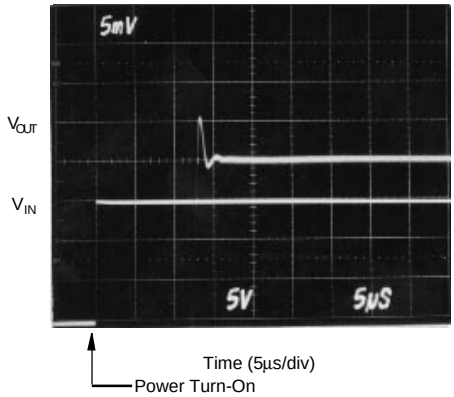
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	55 x 75 ±5	1.40 x 1.91 ±13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

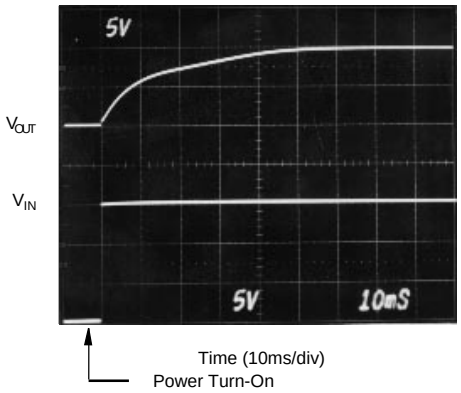
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = +15V unless otherwise noted.

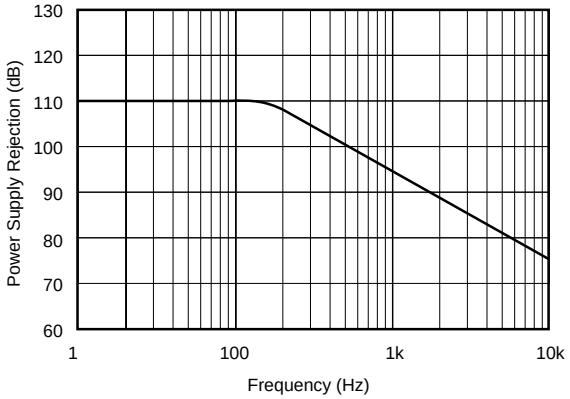
POWER TURN-ON RESPONSE



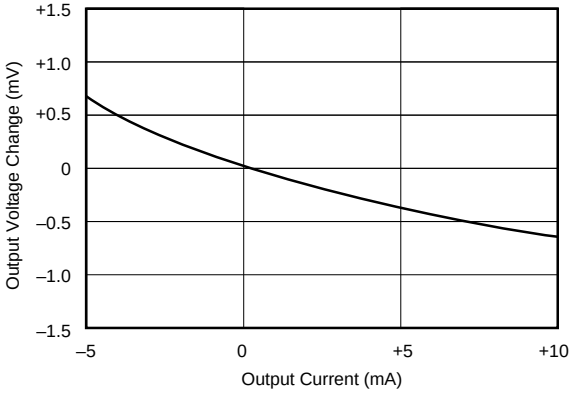
POWER TURN-ON RESPONSE with 1µF Cn



POWER SUPPLY REJECTION vs FREQUENCY



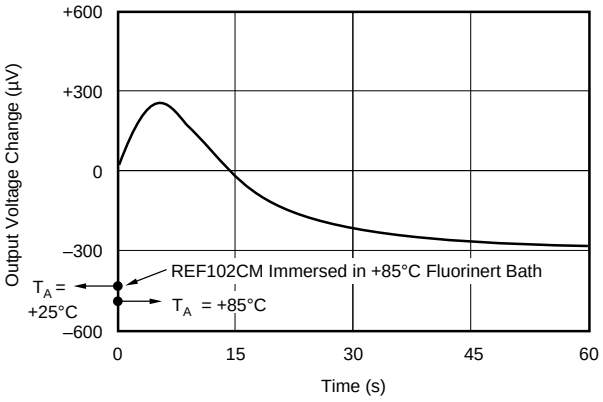
LOAD REGULATION



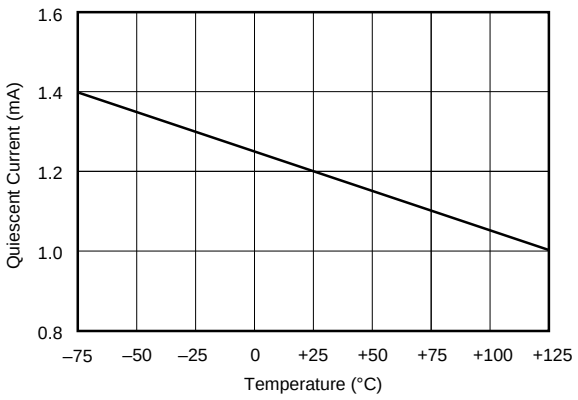
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = +15V unless otherwise noted.

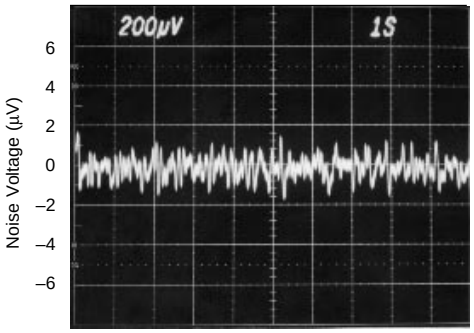
RESPONSE TO THERMAL SHOCK



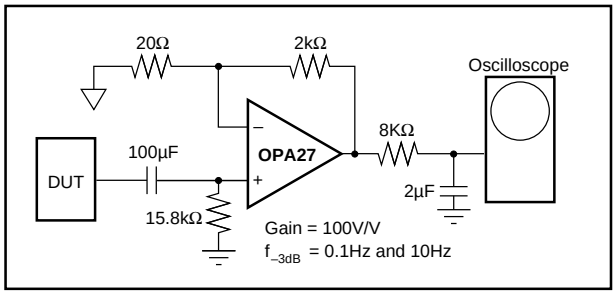
QUIESCENT CURRENT vs TEMPERATURE



TYPICAL REF102 REFERENCE NOISE



Low Frequency Noise (1s /div)
(See Noise Test Circuit)



Noise Test Circuit.

THEORY OF OPERATION

Refer to the diagram on the first page of this data sheet. The 10V output is derived from a compensated buried zener diode DZ_1, op amp A_1, and resistor network R_1–R_6.

Approximately 8.2V is applied to the non-inverting input of A_1 by DZ_1. R_1, R_2, and R_3 are laser-trimmed to produce an exact 10V output. The zener bias current is established from the regulated output voltage through R_4. R_5 allows user-trimming of the output voltage by providing for small external adjustment of the amplifier gain. Because the TCR of R_5 closely matches the TCR of R_1, R_2 and R_3, the voltage trim has minimal effect on the reference drift. The output voltage noise of the REF102 is dominated by the noise of the zener diode. A capacitor can be connected between the Noise Reduction pin and ground to form a low-pass filter with R_6 and roll off the high-frequency noise of the zener.

DISCUSSION OF PERFORMANCE

The REF102 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry—the "butterfly method" and the "box method." The REF102 is specified with the more commonly used "box method." The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{UPPER\ BOUND}$ and $V_{LOWER\ BOUND}$ (see Figure 1). Figure 1 uses the REF102CM as an example. It has a drift specification of 2.5ppm/°C maximum and a specification temperature range of –25°C to +85°C. The "box" height, V_1 to V_2, is 2.75mV.

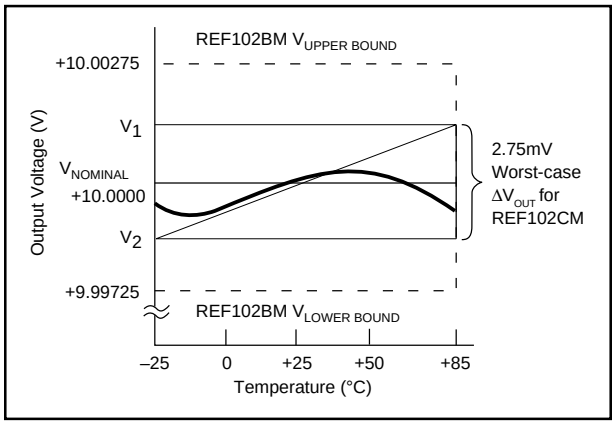
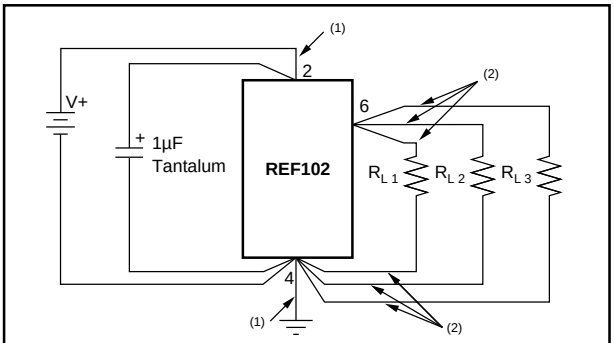


FIGURE 1. REF102CM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF102. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.



NOTES: (1) Lead resistances here of up to a few ohms have negligible effect on performance. (2) A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF102 Installation.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.008ppm/°C per mV of trimmed voltage. In the circuit in Figure 3, any mismatch in TCR between the two sections of the potentiometer will also affect drift, but the effect of the ΔTCR is reduced by a factor of five by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a minimum trim range of ±300mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 50kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

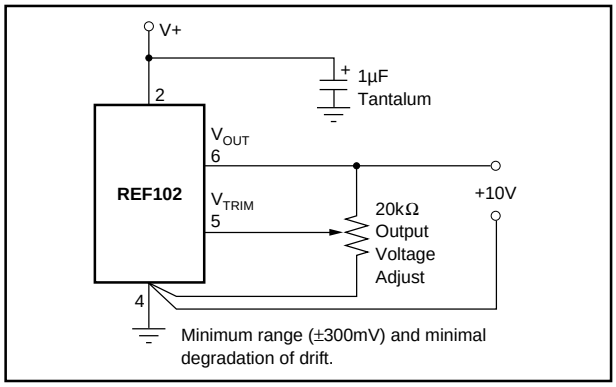


FIGURE 3. REF102 Optional Output Voltage Adjust.

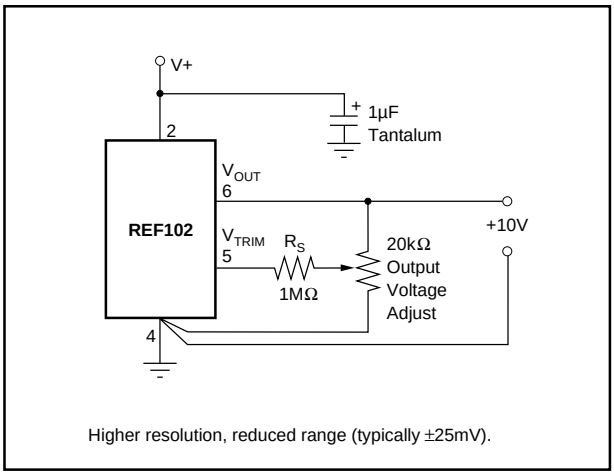


FIGURE 4. REF102 Optional Output Voltage Fine Adjust.

OPTIONAL NOISE REDUCTION

The high-frequency noise of the REF102 is dominated by the zener diode noise. This noise can be greatly reduced by connecting a capacitor between the Noise Reduction pin and ground. The capacitor forms a low pass filter with R_6 (refer to the figure on the first page of the data sheet) and attenuates the high-frequency noise generated by the zener. Figure 5 shows the effect of a 1µF noise reduction capacitor on the high frequency noise of the REF102. R_6 is typically 7kΩ so the filter has a –3dB frequency of about 22Hz. The result is a reduction in noise from about 800µVp-p to under 200µ Vp-p. If further noise reduction is required, use the circuit in Figure 14.

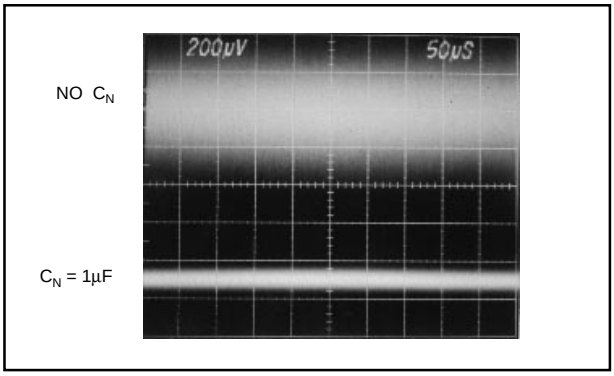


FIGURE 5. Effect of 1µF Noise Reduction Capacitor on Broadband Noise (f_{-3dB} = 1MHz).

APPLICATIONS INFORMATION

High accuracy, extremely low drift, outstanding stability, and low cost make the REF102 an ideal choice for all instrumentation and system reference applications. Figures 6 through 14 show a variety of useful application circuits.

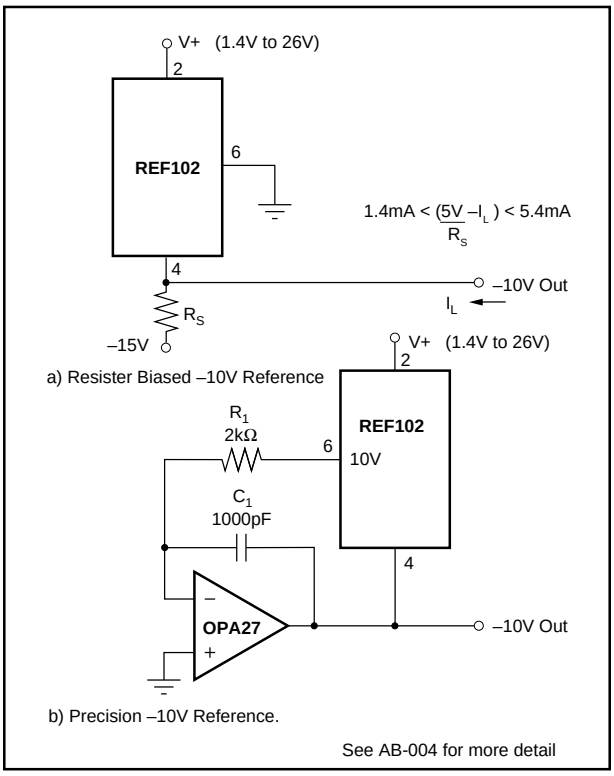


FIGURE 6. –10V Reference Using a) Resistor or b) OPA27.

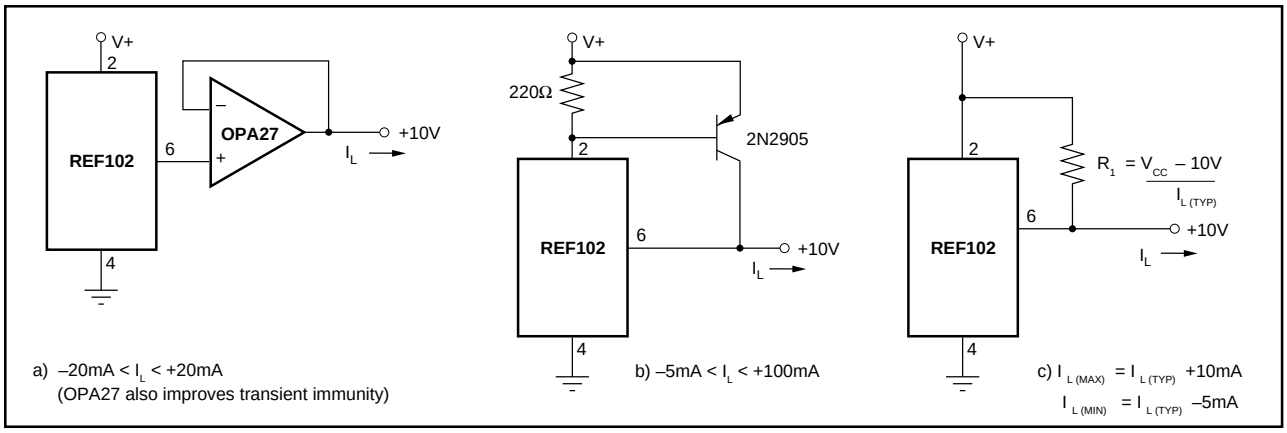


FIGURE 7. +10V Reference With Output Current Boosted to: a) ±20mA, b) +100mA, and c) $I_{L\ (TYP)}$ +10mA, –5A.

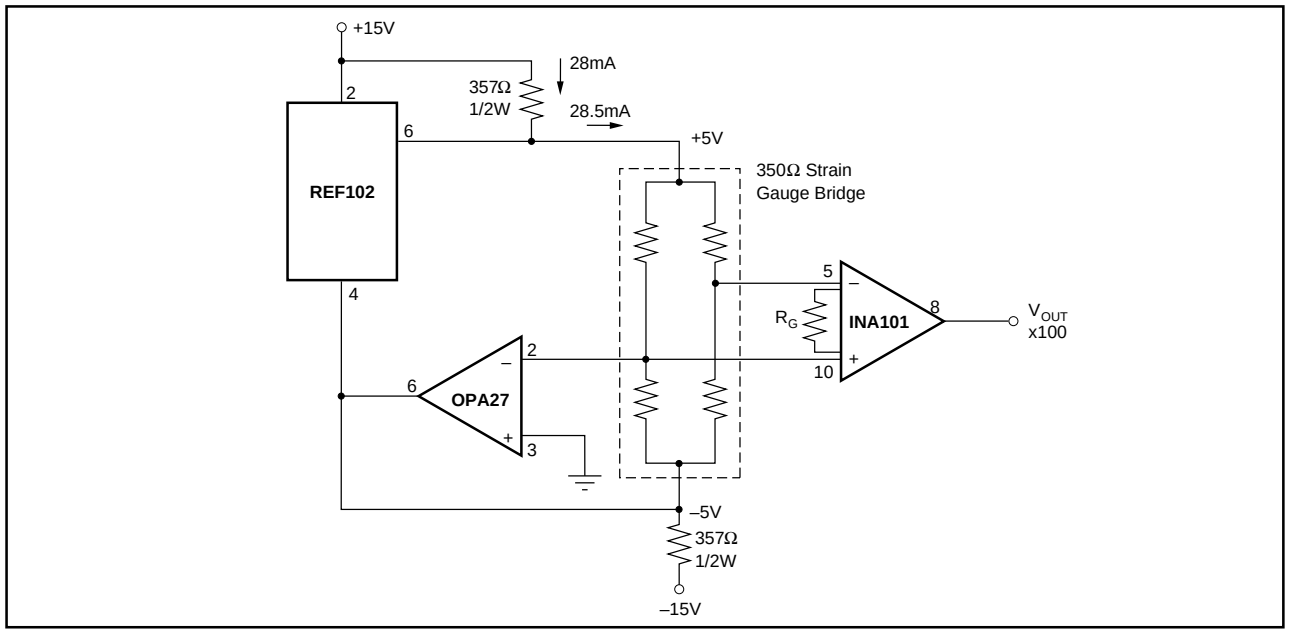


FIGURE 8. Strain Gauge Conditioner for 350Ω Bridge.

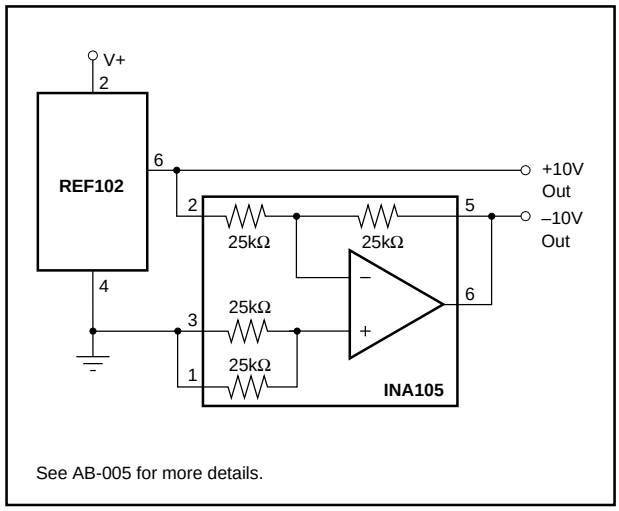


FIGURE 9. ±10V Reference.

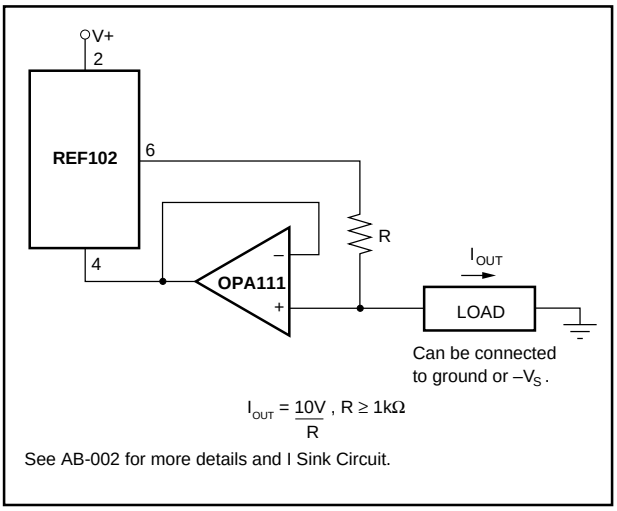
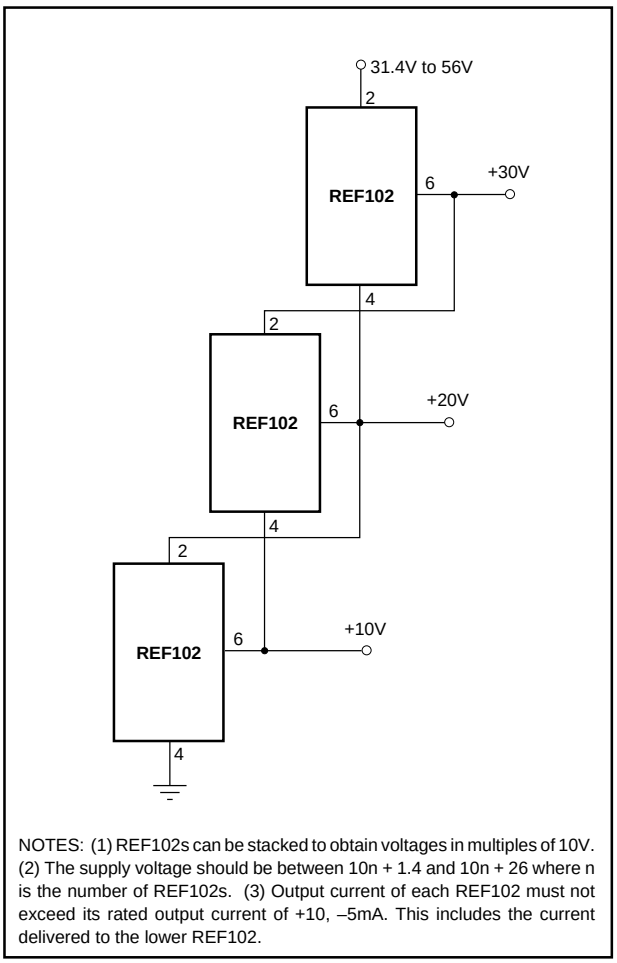


FIGURE 10. Positive Precision Current Source.



NOTES: (1) REF102s can be stacked to obtain voltages in multiples of 10V. (2) The supply voltage should be between 10n + 1.4 and 10n + 26 where n is the number of REF102s. (3) Output current of each REF102 must not exceed its rated output current of +10, –5mA. This includes the current delivered to the lower REF102.

FIGURE 11. Stacked References.

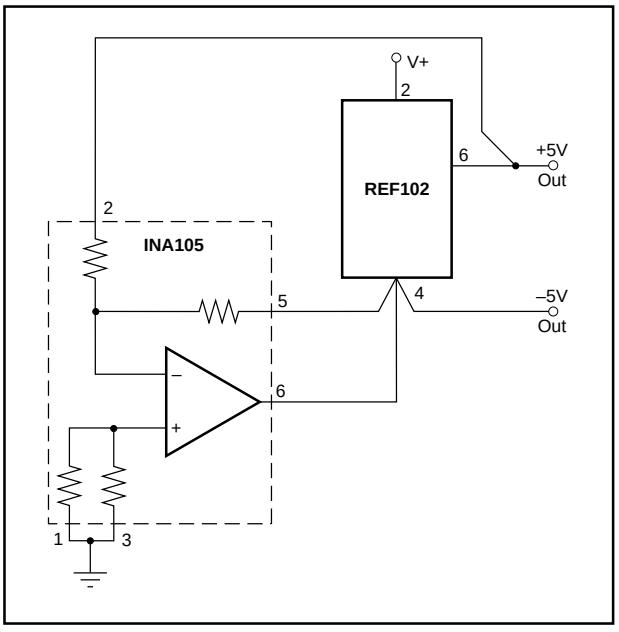


FIGURE 12. ±5V Reference.

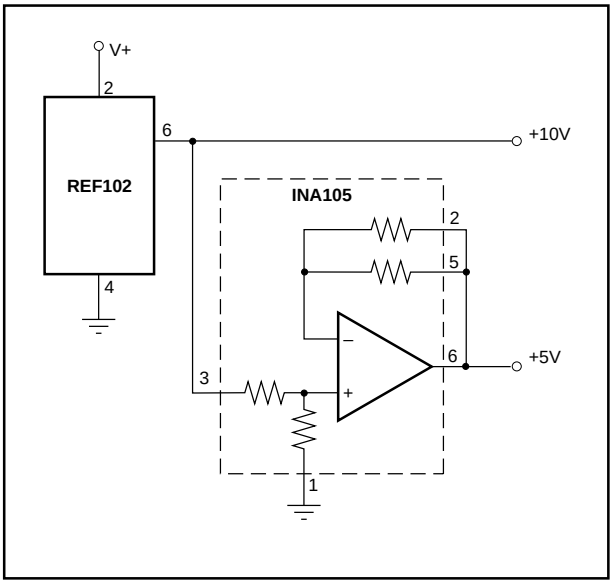


FIGURE 13. +5V and +10V Reference.

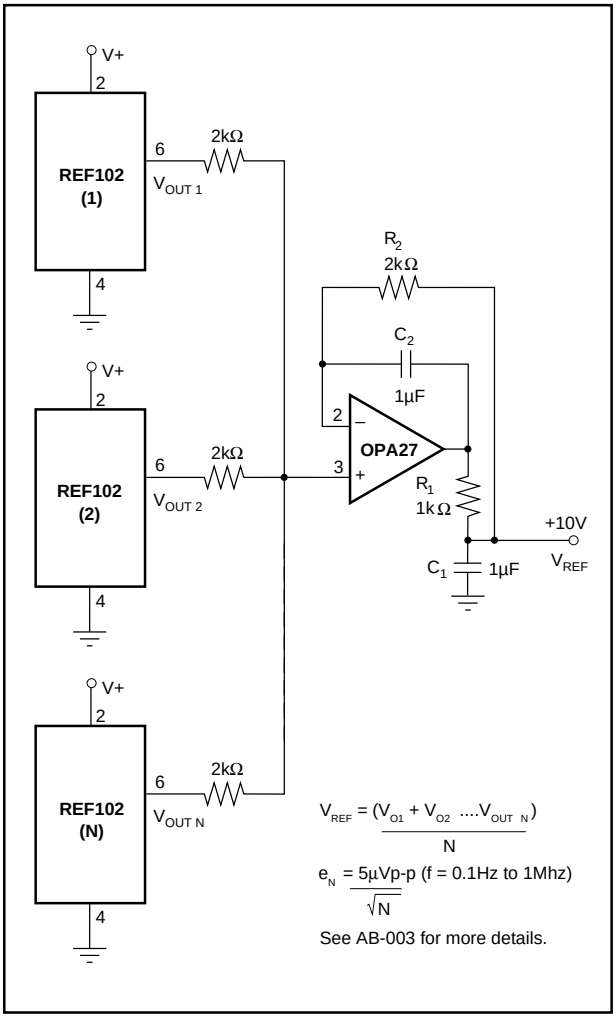
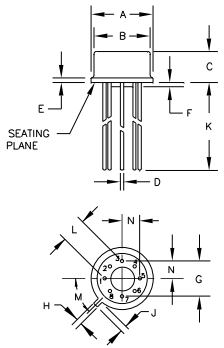


FIGURE 14. Precision Voltage Reference with Extremely Low Noise.

PACKAGE DRAWINGS

Package Number 001 - Metal TO-99

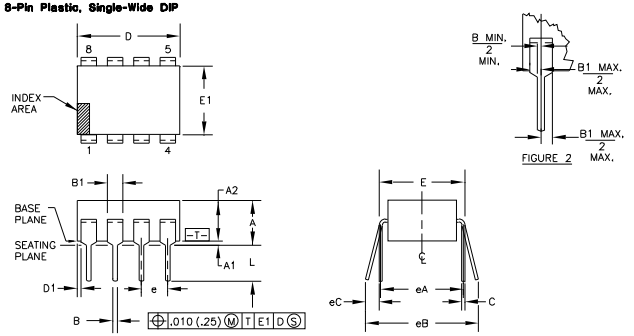


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.335	.380	8.51	9.65	
B	.305	.335	7.75	8.51	
C	.165	.185	4.19	4.70	
D	.016	.021	0.41	0.53	
E	.010	.040	0.25	1.02	
F	.010	.040	0.25	1.02	
G	.200	BASIC	5.08	BASIC	
H	.028	.034	0.71	0.86	
J	.029	.045	0.74	1.14	
K	.500	--	12.7	--	
L	.110	.160	2.79	4.06	
M	45°	BASIC	45°	BASIC	
N	.095	.105	2.41	2.67	

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ001 | REV.: B
JEDEC NUMBER: UNKNOWN

Package Number 006 - 8-Pin Plastic, Single-Wide DIP

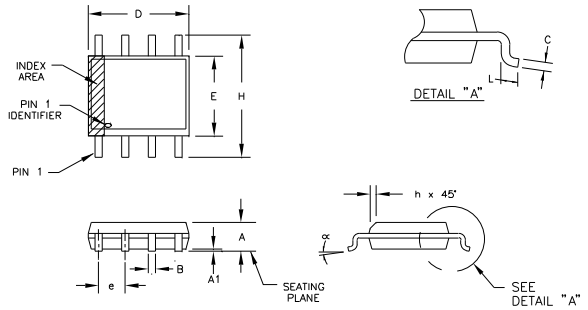


DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
B	.014	.022	0.36	0.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	0.20	0.38	
D	.348	.430	8.84	10.92	4
D1	.005	--	0.13	--	
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.63	BASIC	5
eB	--	.430	--	10.92	6
L	.115	.160	2.92	4.06	3
N	8		8		7

NOTES:
1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 4, 5, AND 8) MAY BE CONFIGURED AS SHOWN IN FIGURE 2.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 | REV.: D
JEDEC NUMBER: MS-001

Package Number 182 - 8-Lead SO-8 Surface Mount



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.054	.068	1.37	1.73	
A1	.004	.009	0.10	0.23	
B	.014	.019	0.36	0.48	
C	.008	.0098	0.20	0.25	
D	.189	.196	4.80	4.98	
E	.150	.157	3.81	3.99	
e	.050	BASIC	1.27	BASIC	
H	.229	.244	5.82	6.20	
h	.010	.019	0.25	0.48	
L	.016	.050	0.41	1.27	
N	8		8		
∝	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.086 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 | REV.: F
JEDEC NUMBER: MS-012