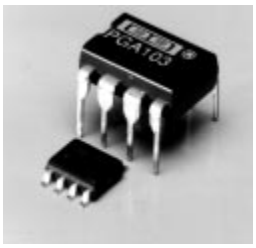
BURR - BROWN®



# PGA103

# Programmable Gain AMPLIFIER

## FEATURES

- DIGITALLY PROGRAMABLE GAINS: G=1, 10, 100V/V
- CMOS/TTL-COMPATIBLE INPUTS
- LOW GAIN ERROR: ±0.05% max, G=10
- LOW OFFSET VOLTAGE DRIFT: 2μV/°C
- LOW QUIESCENT CURRENT: 2.6mA
- LOW COST
- 8-PIN PLASTIC DIP, SO-8 PACKAGES

## APPLICATIONS

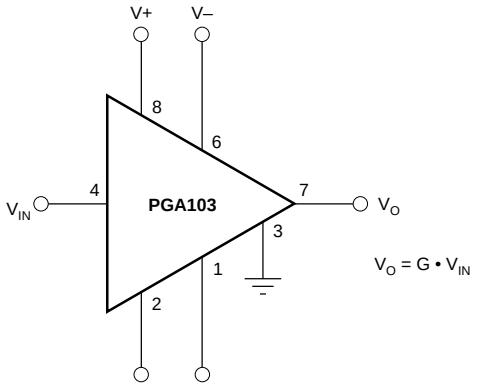
- DATA ACQUISITION SYSTEMS
- GENERAL PURPOSE ANALOG BOARDS
- MEDICAL INSTRUMENTATION

## DESCRIPTION

The PGA103 is a programmable-gain amplifier for general purpose applications. Gains of 1, 10, or 100 are digitally selected by two CMOS/TTL-compatible inputs. The PGA103 is ideal for systems that must handle wide dynamic range signals.

The PGA103's high speed circuitry provides fast settling time, even at G=100 (8μs to 0.01%). Bandwidth is 250kHz at G=100, yet quiescent current is only 2.6mA. It operates from ±4.5V to ±18V power supplies.

The PGA103 is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the –40°C to +85°C temperature range.




| GAIN | $A_1$ | $A_0$ |
|---|---|---|
| 1 | 0 | 0 |
| 10 | 0 | 1 |
| 100 | 1 | 0 |

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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132


PDS-1208B Printed in U.S.A. November, 1993

# SPECIFICATIONS

## ELECTRICAL

$T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ unless otherwise specified.

| PARAMETER | CONDITIONS | PGA103P, U | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **INPUT** | | | | | |
| Offset Voltage, RTI | | | | | |
| G = 1 | $T_A$ = +25°C | | ±200 | ±1500 | µV |
| G = 10 | | | ±100 | ±500 | µV |
| G = 100 | | | ±100 | ±500 | µV |
| vs Temperature | $T_A = T_{MIN}$ to $T_{MAX}$ | | | | |
| G = 1 | | | ±5 | | µV/°C |
| G = 10 | | | ±2 | | µV/°C |
| G = 100 | | | ±2 | | µV/°C |
| vs Power Supply | $V_S$ = ±4.5V to ±18V | | | | |
| G = 1 | | | 30 | 70 | µV/V |
| G = 10 | | | 10 | 35 | µV/V |
| G = 100 | | | 10 | 35 | µV/V |
| Impedance | | | $10^8$ \|\| 2 | | Ω \|\| pF |
| **INPUT BIAS CURRENT** | | | | | |
| Initial Bias Current | | | ±50 | ±150 | nA |
| vs Temperature | | | ±100 | | pA/°C |
| **NOISE VOLTAGE, RTI** | G = 100, $R_S$ = 0Ω | | | | |
| f = 10Hz | | | 16 | | nV/√Hz |
| f = 100Hz | | | 11 | | nV/√Hz |
| f = 1kHz | | | 11 | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.6 | | µVp-p |
| **NOISE CURRENT** | | | | | |
| f = 10Hz | | | 2.8 | | pA/√Hz |
| f = 1kHz | | | 0.3 | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 76 | | pAp-p |
| **GAIN** | | | | | |
| Gain Error | | | | | |
| G = 1 | | | ±0.005 | ±0.02 | % |
| G = 10 | | | ±0.02 | ±0.05 | % |
| G = 100 | | | ±0.04 | ±0.2 | % |
| Gain vs Temperature | | | | | |
| G = 1 | | | ±2 | | ppm/°C |
| G = 10 | | | ±10 | | ppm/°C |
| G = 100 | | | ±30 | | ppm/°C |
| Nonlinearity | | | | | |
| G = 1 | | | ±0.001 | ±0.003 | % of FSR |
| G = 10 | | | ±0.002 | ±0.005 | % of FSR |
| G = 100 | | | ±0.004 | ±0.01 | % of FSR |
| **OUTPUT** | | | | | |
| Voltage, Positive | | (V+) –3.5 | (V+) –2.5 | | V |
| Negative | | (V–) +3.5 | (V–) +2.5 | | V |
| Load Capacitance, max | | | 1000 | | pF |
| Short-Circuit Current | | | ±25 | | mA |
| **FREQUENCY RESPONSE** | | | | | |
| Bandwidth, –3dB | | | | | |
| G = 1 | | | 1.5 | | MHz |
| G = 10 | | | 750 | | kHz |
| G = 100 | | | 250 | | kHz |
| Slew Rate | $V_O$ = ±10V | | 9 | | V/µs |
| Settling Time, 0.1% | | | | | |
| G = 1 | | | 2 | | µs |
| G = 10 | | | 2.2 | | µs |
| G = 100 | | | 6.5 | | µs |
| Settling Time, 0.01% | | | | | |
| G = 1 | | | 2.5 | | µs |
| G = 10 | | | 2.5 | | µs |
| G = 100 | | | 8 | | µs |
| Overload Recovery | 50% Overdrive | | 2.5 | | µs |
| **DIGITAL LOGIC INPUTS** | | | | | |
| Digital Low Voltage | | –5.6 | | 0.8 | V |
| Digital Low or High Current | | | 1 | | µA |
| Digital High Voltage | | 2 | | V+ | V |

# SPECIFICATIONS (CONT)

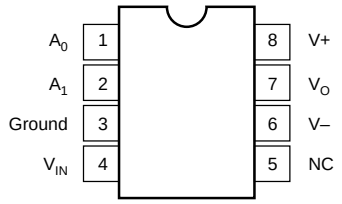
## ELECTRICAL

$T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ unless otherwise specified.

| PARAMETER | CONDITIONS | PGA103P, U | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **POWER SUPPLY** | | | | | |
| Voltage Range | | ±4.5 | ±15 | ±18 | V |
| Current | $V_{IN}$ = 0V | | ±2.6 | ±3.5 | mA |
| **TEMPERATURE RANGE** | | | | | |
| Specification | | –40 | | +85 | °C |
| Operating | | –40 | | +125 | °C |
| $\theta_{JA}$: P or U Package | | | 100 | | °C/W |

## PIN CONFIGURATION

**Top View** **DIP/SO-8**




## ORDERING INFORMATION

| MODEL | PACKAGE | TEMPERATURE RANGE |
|---|---|---|
| PGA103P | 8-Pin Plastic DIP | –40°C to +85°C |
| PGA103U | SO-8 Surface-Mount | –40°C to +85°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## ABSOLUTE MAXIMUM RATINGS

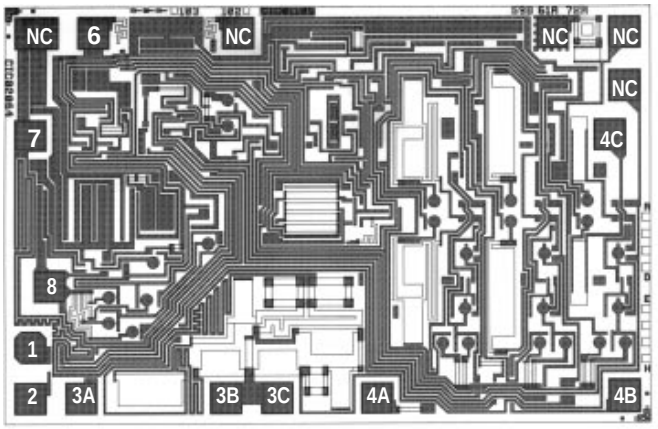
| | |
|---|---|
| Supply Voltage | ±18V |
| Analog Input Voltage Range | V– to V+ |
| Logic Input Voltage Range | V– to V+ |
| Output Short Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering,10s) | +300°C |

## PACKAGE INFORMATION

| MODEL | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| PGA103P | 8-Pin Plastic DIP | 006 |
| PGA103U | SO-8 Surface-Mount | 182 |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## DICE INFORMATION




**PGA103 DIE TOPOGRAPHY**

| PAD | FUNCTION |
|---|---|
| 1 | $A_0$ |
| 2 | $A_1$ |
| 3A, 3B, 3C(1) | Ground |
| 4A, 4B, 4C(2) | $V_{IN}$ |
| 6 | V– |
| 7 | $V_O$ |
| 8 | V+ |

NC: No Connection
NOTES: (1) Connect all three indicated pads. (2) Connect all three indicated pads.
**Substrate Bias:** Internally connected to V– power supply.

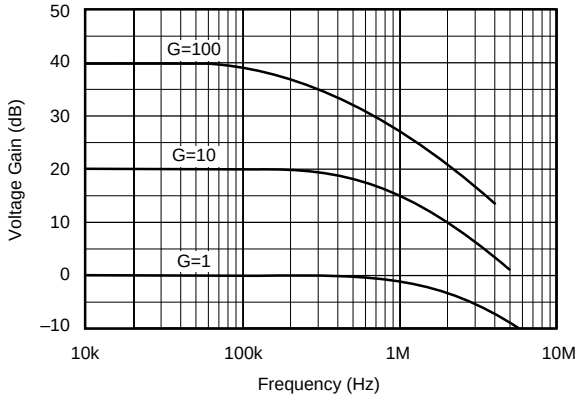
### MECHANICAL INFORMATION

| | MILS (0.001") | MILLIMETERS |
|---|---|---|
| Die Size | 69 x 105 ±5 | 1.75 x 2.67 ±0.13 |
| Die Thickness | 20 ±3 | 0.51 ±0.08 |
| Min. Pad Size | 4 x 4 | 0.1 x 0.1 |
| Backing | | Gold |

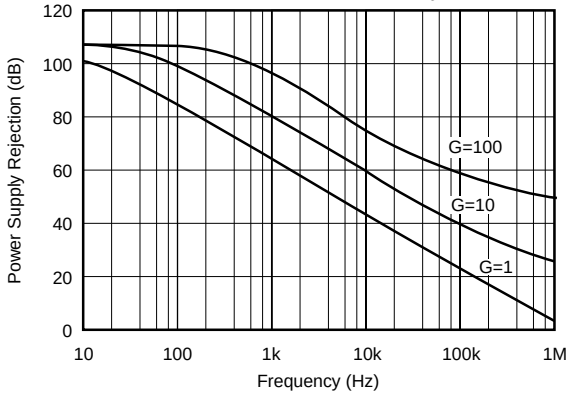
# TYPICAL PERFORMANCE CURVES

$T_A$ = +25°C, $V_S$ = ±15V unless otherwise noted.

VOLTAGE GAIN vs FREQUENCY



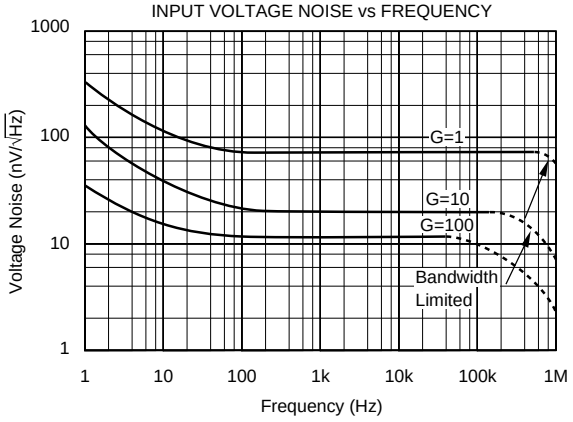

POWER SUPPLY REJECTION vs FREQUENCY



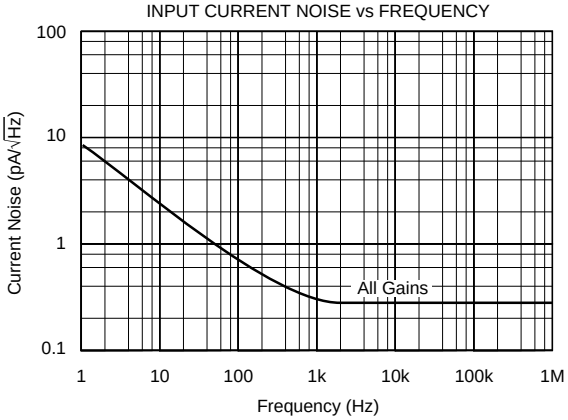
# TYPICAL PERFORMANCE CURVES (CONT)

$T_A$ = +25°C, $V_S$ = ±15V unless otherwise noted.

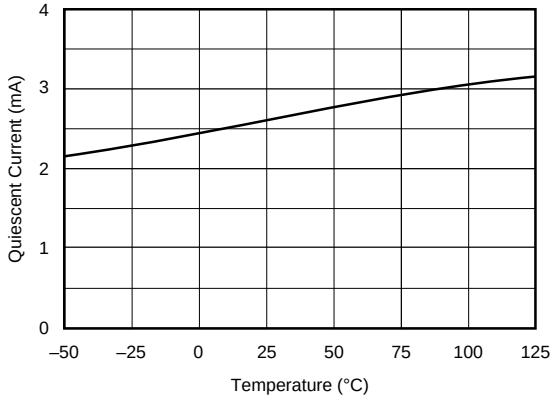
INPUT VOLTAGE NOISE vs FREQUENCY



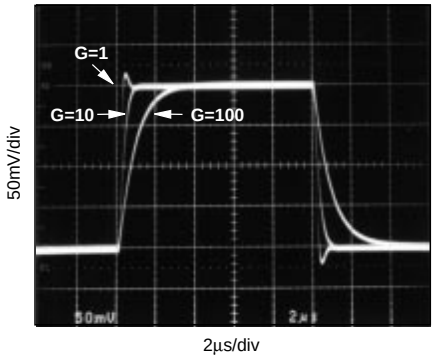

INPUT CURRENT NOISE vs FREQUENCY



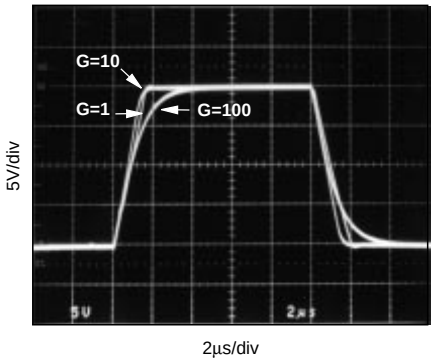

QUIESCENT CURRENT vs TEMPERATURE




SMALL SIGNAL RESPONSE

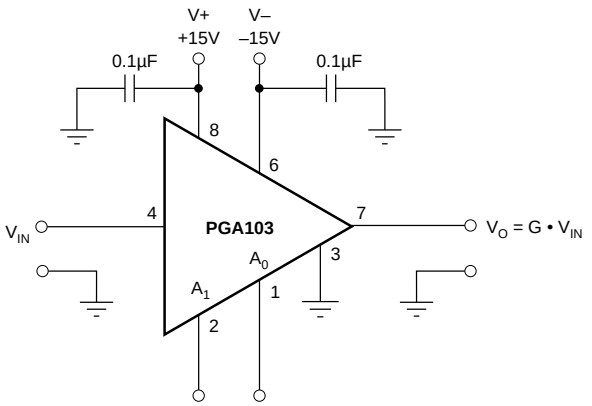



LARGE SIGNAL RESPONSE



# APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the PGA103. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.




| GAIN | $A_1$ | $A_0$ |
|---|---|---|
| 1 | 0 | 0 |
| 10 | 0 | 1 |
| 100 | 1 | 0 |
| Not Valid | 1 | 1 |

Logic 0: (–5.6) ≤ V ≤ 0.8V
Logic 1: 2V ≤ V ≤ (V+)
Logic voltages referred to pin 3.

NOTE: (1) Low impedance ground connection required for good gain accuracy—see text.

FIGURE 1. Basic Connections.

The input and output are referred to the ground terminal, pin 3. This must be a low-impedance connection to assure good gain accuracy. A resistance of 0.1Ω in series with the ground pin will cause the gain in G=100 to decrease by approximately 0.2%.

## DIGITAL INPUTS

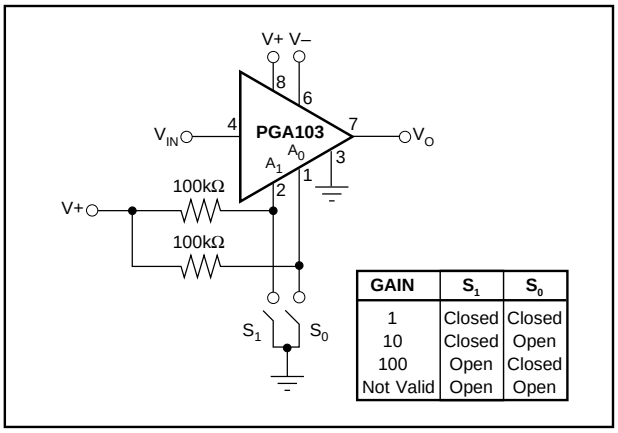
The digital inputs, $A_0$ and $A_1$, select the gain according to the logic table in Figure 1. The digital inputs interface directly to common CMOS and TTL logic components. The logic inputs are referenced to the ground terminal, pin 3.

The logic table in Figure 1 shows that logic "1" on both $A_0$ and $A_1$ is invalid. This logic code will not cause damage, but the amplifier output will not be predictable while this code is selected. The output will recover when a valid code is selected.

The digital inputs are not latched, so a change in logic inputs immediately selects a new gain. Switching time of the logic is approximately 0.5µs. The time to respond to gain change is equal to the switching time plus the time it takes the amplifier to settle to a new output voltage in the newly selected gain (see settling time specifications).

Many applications use an external logic latch to access gain control signals from a high speed data bus. Using an external latch isolates the high speed digital bus from sensitive analog circuitry. Locate the latch circuitry as far as practical from analog circuitry to avoid coupling digital noise into the analog circuitry.

Some applications select gain of the PGA103 with switches or jumpers. Figure 2 shows pull-up resistors connected to assure a noise-free logic "1" when the switch or jumper is off or open. Fixed-gain applications can connect the logic inputs directly to V+ or ground (or other valid logic level) without a series resistor.

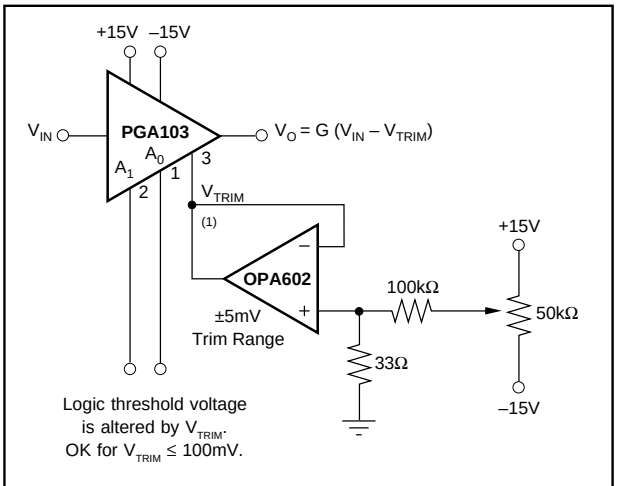



| GAIN | $S_1$ | $S_0$ |
|---|---|---|
| 1 | Closed | Closed |
| 10 | Closed | Open |
| 100 | Open | Closed |
| Not Valid | Open | Open |

FIGURE 2. Switch or Jumper-Selected Gains.

## OFFSET TRIMMING

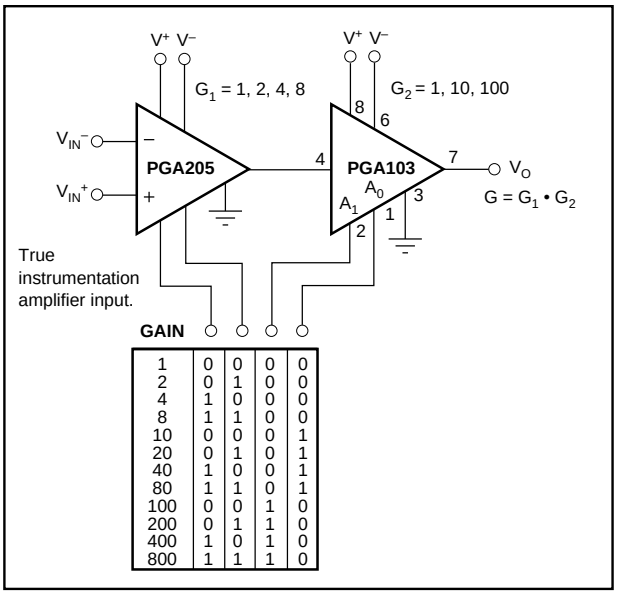
Offset voltage is laser-trimmed to typically less than 200µV (referred to input) in all three gains. The input-referred offset voltage can be different for each gain.




NOTE: (1) Op amp buffer is required to preserve good gain accuracy—see text.

FIGURE 3. Offset Voltage Trim Circuit.

Figure 3 shows a circuit used to trim the offset voltage of the PGA103. An op amp buffers the trim voltage to provide a low impedance at the ground terminal. This is required to maintain accurate gain. Remember that the logic inputs, $A_0$ and $A_1$, are referenced to this ground connection, so the logic threshold voltage will be affected by the trim voltage. This is insignificant if the offset adjustment is used only to trim offset voltage. If a large offset is used (greater than 0.1V), be sure that the logic input signals provide valid logic levels when referred to the voltage at the ground terminal, pin 3.




| | | | | |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 4 | 1 | 0 | 0 | 0 |
| 8 | 1 | 1 | 0 | 0 |
| 10 | 0 | 0 | 0 | 1 |
| 20 | 0 | 1 | 0 | 1 |
| 40 | 1 | 0 | 0 | 1 |
| 80 | 1 | 1 | 0 | 1 |
| 100 | 0 | 0 | 1 | 0 |
| 200 | 0 | 1 | 1 | 0 |
| 400 | 1 | 0 | 1 | 0 |
| 800 | 1 | 1 | 1 | 0 |

FIGURE 4. Programmable Gain Instrumentation Amplifier.

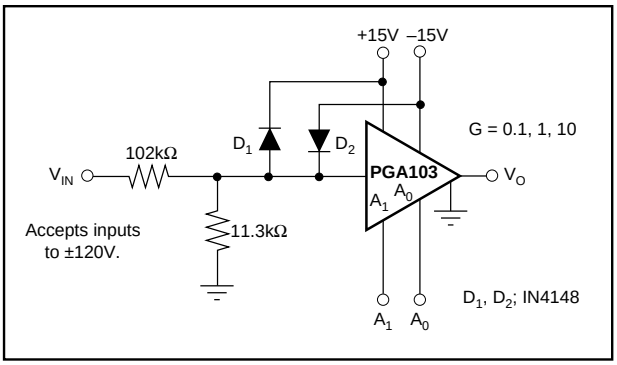



FIGURE 5. Wide Input Voltage Range Amplifer.

| MODEL | CHARACTERISTICS |
|---|---|
| INA103 | Low Noise, 1nV/√Hz IA |
| INA105 | G = 1 Difference Amp |
| INA106 | G = 10 Difference Amp |
| INA114 | Resistor-Programmed Gain, Precision |
| INA117 | ±200V C-M Input Range Difference Amp |
| INA111 | FET Input, High Speed IA |
| INA131 | Precision, G = 100 IA |

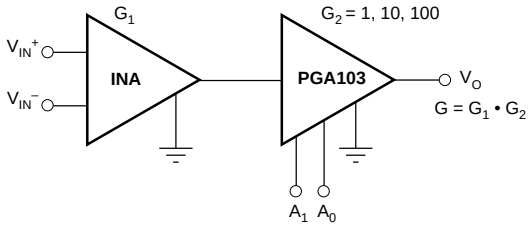
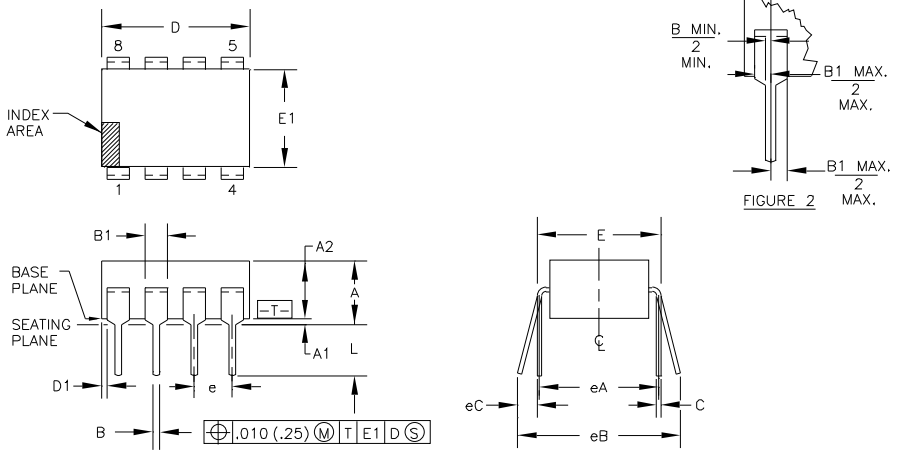



FIGURE 6. Instrumentation Amplifier with Programmable Gain Output Amp.

## PACKAGE DRAWINGS

**Package Number 006 - 8-Pin Plastic, Single-Wide DIP**



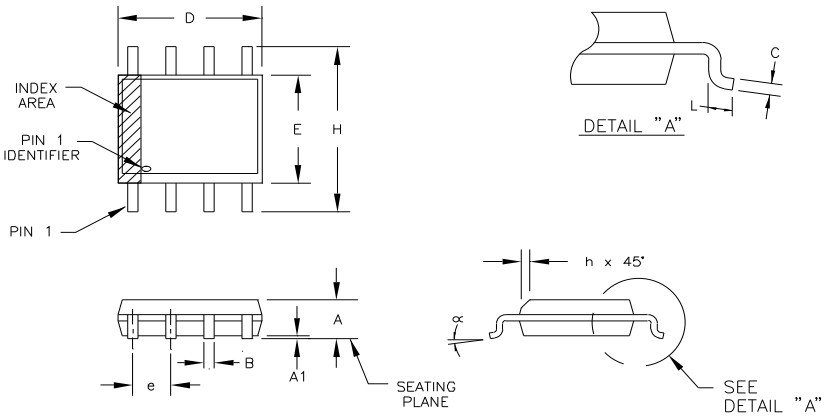

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| B | .014 | .022 | 0.36 | 0.56 | |
| B1 | .045 | .070 | 1.14 | 1.78 | |
| C | .008 | .015 | 0.20 | 0.38 | |
| D | .348 | .430 | 8.84 | 10.92 | 4 |
| D1 | .005 | -- | 0.13 | -- | |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 BASIC | | 2.54 BASIC | | |
| eA | .300 BASIC | | 7.63 BASIC | | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| L | .115 | .160 | 2.92 | 4.06 | 3 |

| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| N | 8 | | 8 | | 7 |

NOTES:
1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 4, 5, AND 8) MAY BE CONFIGURED AS SHOWN IN FIGURE 2.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

| PACKAGE NUMBER: ZZ006 | REV.: D |
|---|---|
| JEDEC NUMBER: MS-001 | |

**Package Number 182 - 8-Lead SO-8 Surface Mount**




| DIM | INCHES | | MILLIMETERS | | NOTE |
|---|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. | |
| A | .054 | .068 | 1.37 | 1.73 | |
| A1 | .004 | .009 | 0.10 | 0.23 | |
| B | .014 | .019 | 0.36 | 0.48 | |
| C | .008 | .0098 | 0.20 | 0.25 | |
| D | .189 | .196 | 4.80 | 4.98 | |
| E | .150 | .157 | 3.81 | 3.99 | |
| e | .050 BASIC | | 1.27 BASIC | | |
| H | .229 | .244 | 5.82 | 6.20 | |
| h | .010 | .019 | 0.25 | 0.48 | |
| L | .016 | .050 | 0.41 | 1.27 | |
| N | 8 | | 8 | | |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.086 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

| PACKAGE NUMBER: ZZ182 | REV.: F |
|---|---|
| JEDEC NUMBER: MS-012 | |