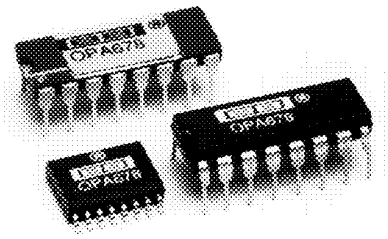
BURR - BROWN®



OPA678

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 11ns (1%)
- WIDE BANDWIDTH: 200MHz
- TWO LOGIC SELECTABLE INPUTS
- LOW OFFSET VOLTAGE: ±380µV
- FAST INPUT SWITCHING: 4ns
- ACCEPTS TTL/ECL SWITCHING SIGNALS
- UNITY GAIN STABLE
- 16-PIN DIP AND SOIC PACKAGES

APPLICATIONS

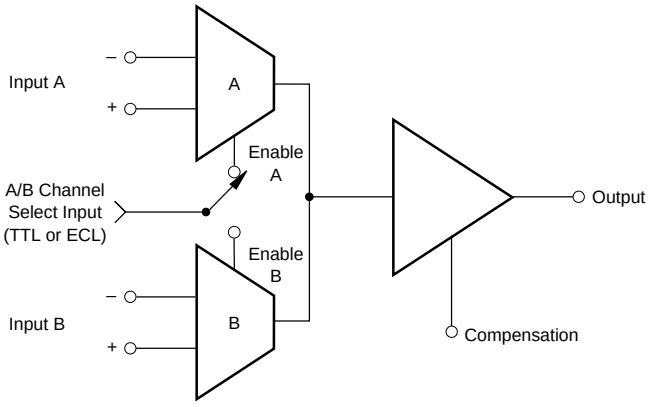
- VIDEO AMPLIFICATION AND SWITCHING
- FAST 2-INPUT MULTIPLEXER
- PULSE/RF AMPLIFIERS
- PROGRAMMABLE-GAIN AMPLIFIER
- ACTIVE FILTERS
- SYNCHRONOUS DEMODULATOR

DESCRIPTION

The OPA678 is a wideband monolithic operational amplifier with two independent differential inputs. Either input can be selected by an external TTL or ECL logic signal. The amplifier is externally compensated and features a very fast input selection speed, 4ns for either ECL or TTL. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA678 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make this amplifier suitable for RF and video applications.

The OPA678 is available in DIP, SOIC, and sidebraze packages. A military temperature range part is available in the sidebraze package.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1136C
Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG, AP, AU			OPA678SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE[1]								
Voltage: f_O = 100Hz	R_S = 0Ω		55			*		nV/√Hz
f_O = 1kHz			21			*		nV/√Hz
f_O = 10kHz			7.8			*		nV/√Hz
f_O = 100kHz			4.9			*		nV/√Hz
f_B = 10Hz to 10MHz			18			*		µVrms
Current: f_O = 10Hz to 1MHz			2.1			*		pA/√Hz
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0VDC		±380	±1.5mV		±380	±1mV	µV
Offset Voltage Drift	T_A = T_{MIN} to T_{MAX}		±3	±15		±3	±10	µV/°C
Supply Rejection	$±V_{CC}$ = 4.5V to 5.5V	65	71		*	*		dB
BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0VDC		14	50		*	*	µA
OFFSET CURRENT[1]								
Input Offset Current	V_{CM} = 0VDC		0.2	2		*	1.5	µA
INPUT IMPEDANCE[1]								
Differential			25k || 2			*		Ω || pF
Common-Mode			10^6 || 5			*		Ω || pF
INPUT VOLTAGE RANGE[1]								
Common-Mode Input Range		2.0	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	75	85		*	*		dB
OPEN-LOOP GAIN, DC[1]								
Open-Loop Voltage Gain		50	60		*	*		dB
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	Gain = +1V/V, C_C = 9pF	140	200		*	*		MHz
	Gain = +2V/V, C_C = 7pF		100			*		MHz
	Gain = +5V/V, C_C = 1pF		70			*		MHz
Crosstalk	Gain = +1V/V, f = 100kHz		–102			*		dBC[2]
	f = 1MHz		–83			*		dBC
	f = 10MHz		–64			*		dBC
	f = 100MHz		–44			*		dBC
Harmonic Distortion: 5MHz	G = +1V/V, R_L= 150Ω, V_O = 0.25Vp-p							
	Second Harmonic		–71			*		dBC[3]
	Third Harmonic		–82			*		dBC
Large Signal Response[4]	V_O = 2.5Vp-p, Gain = +1V/V	32	45		*	*		MHz
Slew Rate	Gain = +1V/V	250	350		*	*		V/µs
Settling Time: 1%	Gain = –1V/V, $1V_{OUT}$ Step		11			*		ns
0.1%			22			*		ns
0.01%			30			*		ns
Differential Gain (0V to 0.7V)	4.5MHz, Gain = +2V/V, C_C = 2.2pF		0.02					%
Differential Phase (0V to 0.7V)	4.5MHz, Gain = +2V/V, C_C = 2.2pF		0.02					Degrees
INPUT SELECTION[5]								
Transition Time	ECL: Operation		4	8		*	9	ns
50% In to 50% Out	TTL: Operation		4	8		*	9	ns
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic “LO”	0		+0.8	*		*	V
V_{IH}	Logic “HI”	+2.0		+5	*		*	V
I_{IL}	Logic “LO”, V_{IL} = 0V		–0.05	–0.2		*	*	mA
I_{IH}	Logic “HI”, V_{IH} = +2.7V		1	20		*	*	µA
ECL Logic Levels: V_{IL}	Logic “LO”	–1.81		–1.475	*		*	V
V_{IH}	Logic “HI”	–1.15		– 0.88	*		*	V
I_{IL}	Logic “LO”, V_{IL} = –1.6V		–50	–100		*		µA
I_{IH}	Logic “HI”, V_{IH} = –1.0V		–50	–100		*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.5	±3.75		*	*		V
	R_L = 50Ω	±1.7	±2.2		*	*		V
Current Output		±30	±44			*		mA
Output Resistance	1MHz, Open Loop, C_C = 5pF		5			*		Ω
Load Capacitance Stability	R_F = 100Ω, Gain = +1V/V, C_C = 10pF		17			*		pF
Short Circuit Current	Continuous to Gnd		+45			±45		mA

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG, AP, AU			OPA678SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Rated Voltage	$\pm V_{CC}$		5			*		VDC
Derated Performance	$\pm V_{CC}$	4.5		5.5	*		*	VDC
Current, Quiescent	I_O = 0mADC		26	30		*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp AG, AP, AU	–40		+85	*		*	°C
	SG	–55		+125				°C
θ_{JA}	AG, SG		125			*		°C/W
	AP		90					°C/W
	AU		100					°C/W

* Same specifications as for OPA678AG/AP/AU.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

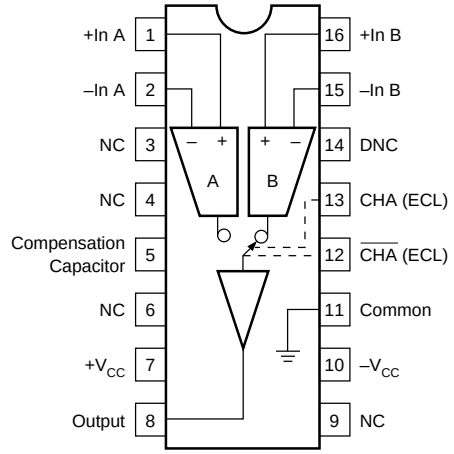
At V_{CC} = ±5VDC, R_L = 150Ω, C_{COMP} = 5pF, and T_A = T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA678AG, AP, AU			OPA678SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	Ambient Temp AG/AP/AU	–40		+85	*		*	°C
	SG				–55		+125	°C
OFFSET VOLTAGE								
Input Offset Voltage	T_A = T_{MIN} to T_{MAX}		600	±2.4mV		*	±2mV	µV
Offset Voltage Drift	T_A = T_{MIN} to T_{MAX}		±3	±15		*	±10	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	60	70		*	73		dB
BIAS CURRENT								
Input Bias Current	V_{CM} = 0VDC		15	85		*	*	µA
OFFSET CURRENT								
Input Offset Current	V_{CM} = 0VDC		0.5	5		*	7	µA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	60	80		*	*		dB
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain		50	60		*	*		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic “LO”	0		+0.8	*		*	V
V_{IH}	Logic “HI”	+2.0		+5	*		*	V
I_{IL}	Logic “LO”, V_{IL} = 0V		–0.08	–0.4		*	*	mA
I_{IH}	Logic “HI”, V_{IH} = +2.7V		5	50		*	*	µA
ECL Logic Levels: V_{IL}	Logic “LO”	–1.81		–1.475	*		*	V
V_{IH}	Logic “HI”	–1.15		–0.88	*		*	V
I_{IL}	Logic “LO”, V_{IL} = –1.6V		–50			*		µA
I_{IH}	Logic “HI”, V_{IH} = –1.0V		–50			*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.5	±3.75		*	*		V
	R_L = 50Ω	±1.5	±2.0		±1.5	*		V
Output Current			44			40		mA
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		25	35		*	*	mA

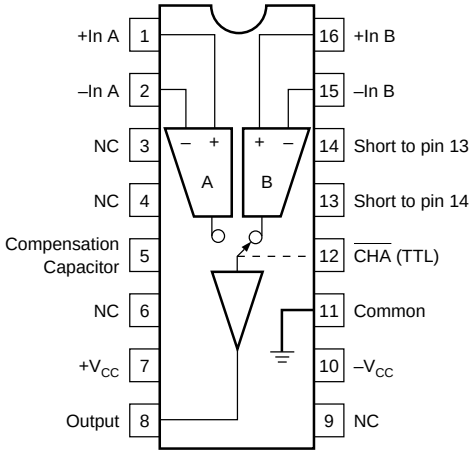
* Same specifications as for AG/AP/AU.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Harmonic distortion will typically be improved significantly in the inverting mode. (4) Large Signal Response is calculated from the formula $LSBW = \frac{SR}{2\pi V_{PEAK}}$. (5) Switching time from application of digital logic signal to input signal selection.

Pin Assignments for Differential ECL Channel Switching



Pin Assignments for TTL Channel Switching



ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Differential Input Voltage	Total V_{CC}
Input Voltage Range (Analog and Digital)	±V_{CC}
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

ORDERING INFORMATION

OPA678 ( ) ( )

Basic Model Number

Performance Grade Code
- A: –40°C to +85°C
- S: –55°C to +125°C

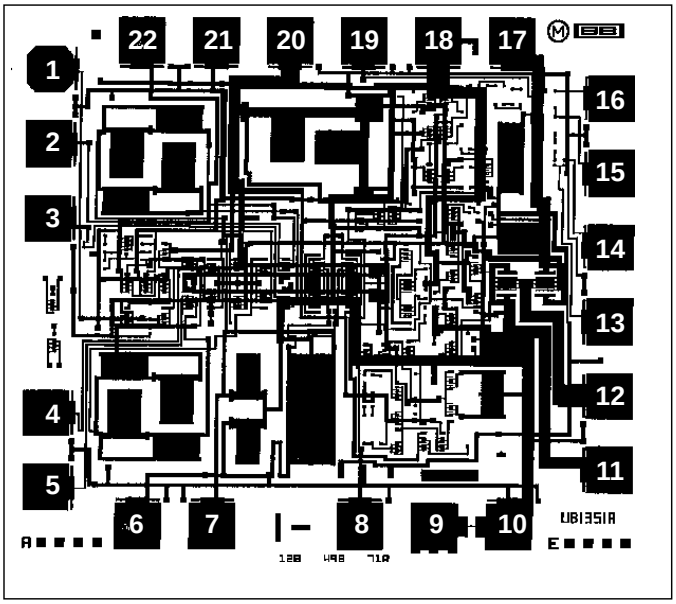
Package Code
- G: 16-pin Ceramic DIP
- P: 16-pin Plastic DIP
- U: 16-pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA678AG	16-Pin Hermetic DIP	109
OPA678AP	16-Pin Plastic DIP	180
OPA678AU	16-Pin SOIC	211
OPA678SG	16-Pin Hermetic DIP	109

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DICE INFORMATION



OPA678B DIE TOPOGRAPHY

PAD	FUNCTION
1	TTL set
2	$-In_2$
3	$+In_2$
4	+In
5	–In
6	V_{OS1}
7	V_{OS2}
8	Comp
9(1)	Fuse
10	V_{CC}
11	V_{CC} O/P
12	Output
13(1)	$FDBK_3$
14(1)	$FDBK_4$
15(1)	$FDBK_5$
16(1)	$FDBK_1$
17	V_{EE} O/P
18	V_{EE}
19(1)	SRC_1
20	GND
21	CH_1 LO
22	CH_1 HI

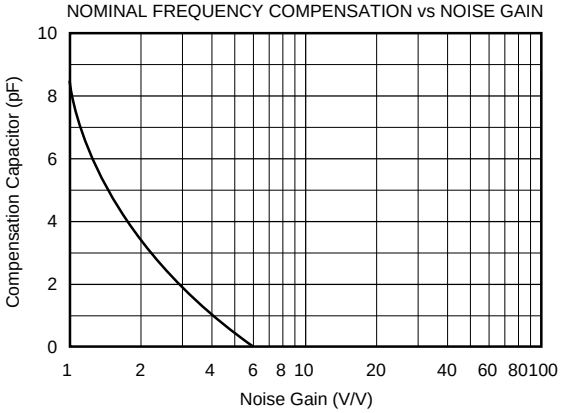
NOTE: (1) No connection required.

MECHANICAL INFORMATION

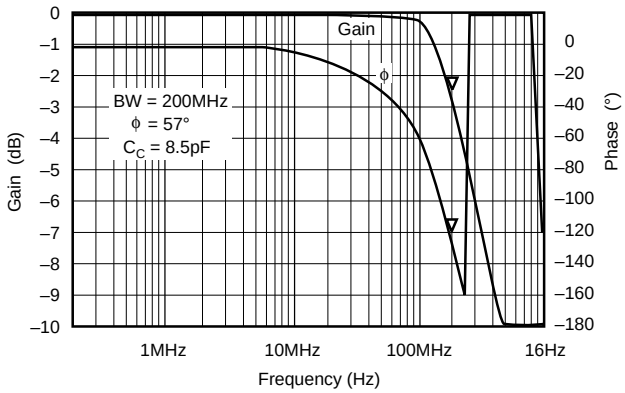
	MILS (0.001")
Die Size	103 x 90±5
Die Thickness	20 ± 3
Min. Pad Size	4 x 4
Backing	Gold
Top Metallization	Gold

TYPICAL PERFORMANCE CURVES

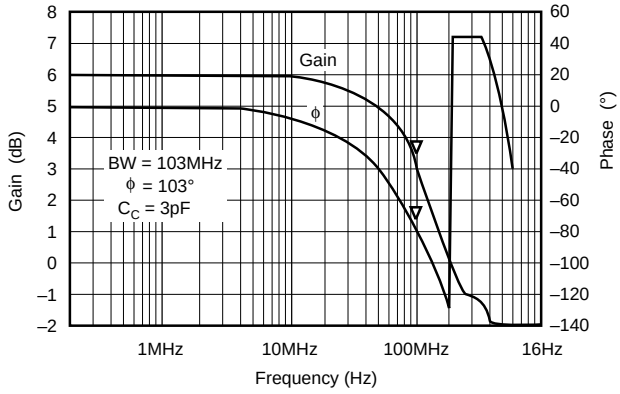
NOMINAL FREQUENCY COMPENSATION vs NOISE GAIN



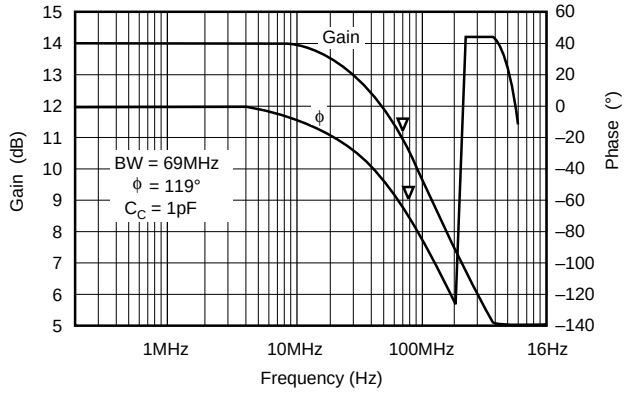
A_V = +1V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



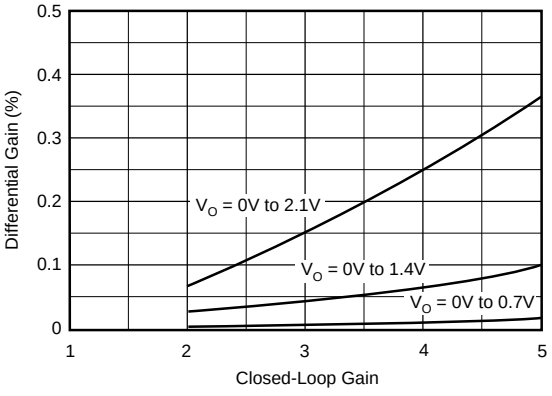
A_V = +2V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



A_V = +5V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

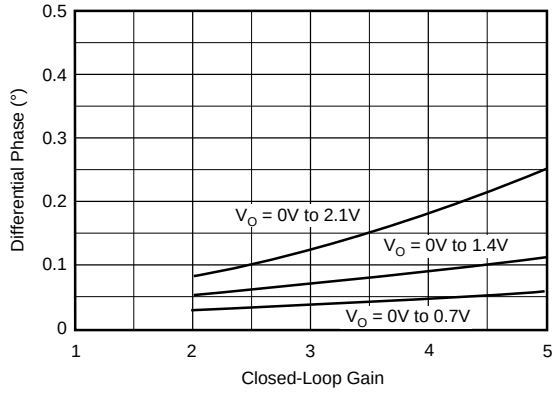


DIFFERENTIAL GAIN vs CLOSED-LOOP GAIN
(f = 4.5MHz)



NOTE: For the gain of +2V/V, C_C = 2.2pF; for the gain of +5V/V, C_C = 0.

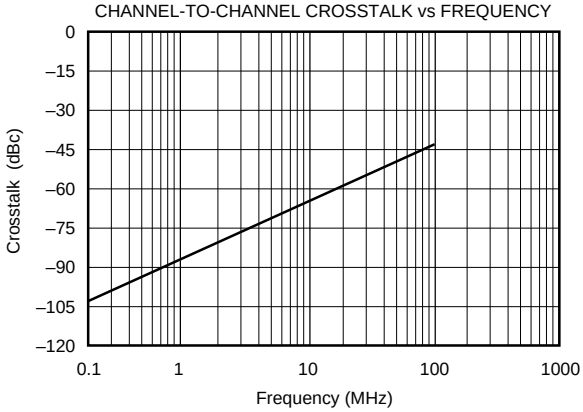
DIFFERENTIAL PHASE vs CLOSED-LOOP GAIN
(f = 4.5MHz)



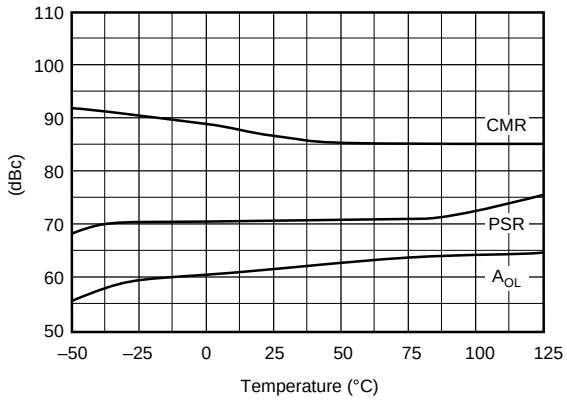
NOTE: For the gain of +2V/V, C_C = 2.2pF; for the gain of +5V/V, C_C = 0.

TYPICAL PERFORMANCE CURVES (CONT)

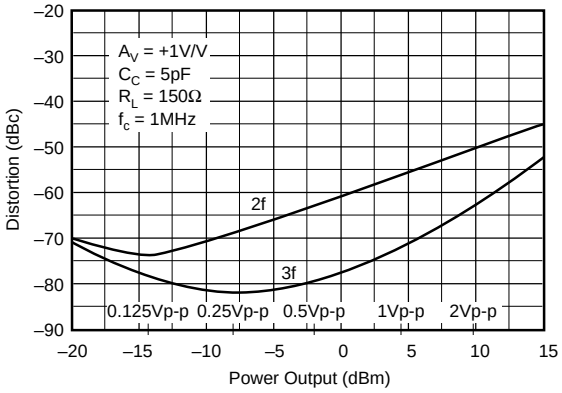
CHANNEL-TO-CHANNEL CROSSTALK vs FREQUENCY



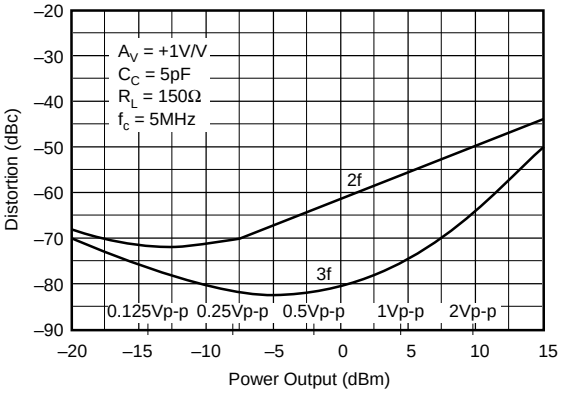
OPEN-LOOP GAIN, CMR, AND PSR vs TEMPERATURE



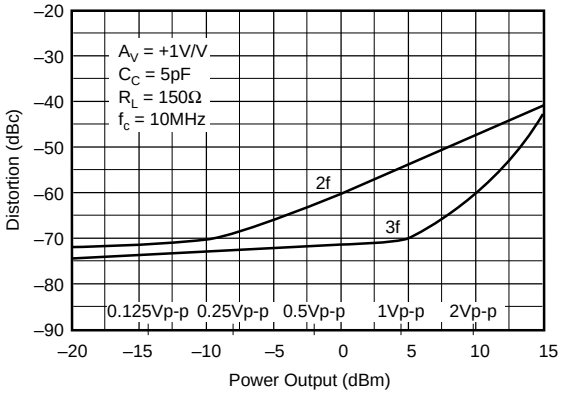
1MHz HARMONIC DISTORTION vs POWER OUTPUT



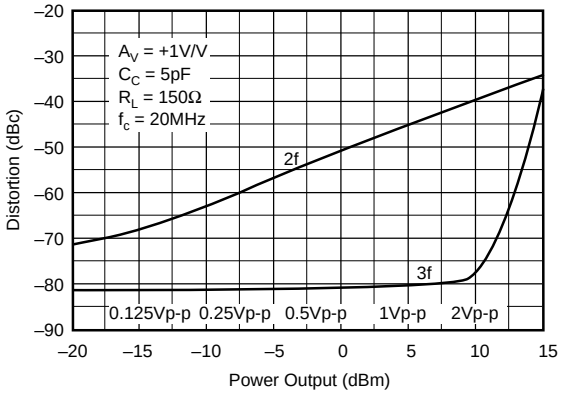
5MHz HARMONIC DISTORTION vs POWER OUTPUT



10MHz HARMONIC DISTORTION vs POWER OUTPUT



20MHz HARMONIC DISTORTION vs POWER OUTPUT



THEORY OF OPERATION

The simplified circuit of the ECL compatible OPA678 is shown in Figure 1. It is a "classical" high-speed op amp architecture with one important exception—the amplifier has two ECL logic selectable differential input stages. An appropriate differential ECL logic signal on A and $\overline{A}$ will turn on either Q5 or Q6, steering operating (tail) current to either differential input pair Q1 and Q2 or Q3 and Q4. The input pair receiving the tail current operates as a conventional op-amp input stage while the de-selected input pair receiving no tail current appears as an open circuit. The de-selected inputs have only a few pF parasitic capacitance and in the off condition exhibit only a very low leakage (bias) current of about 100pA. Two feedback networks can be connected to each input separately allowing a wide range of circuit applications. The feedback network connected to the selected input operates in a normal op amp fashion while the feedback network connected to the de-selected input is totally inactive, appearing only as an additional load to the amplifier's output stage.

For TTL operation, "A select" is held to an internal reference level by tying pins 13 and 14 together. This allows "$\overline{A}$" to become the single-ended TTL input.

Standard TTL and ECL logic levels may be applied to each input selection circuit but only 350mV is typically required to switch between inputs. This logic input sensitivity allows simpler high-speed logic driver circuitry and it minimizes digital noise coupling into adjacent wideband analog circuitry and allows single ended ECL inputs to be used with V_{BB} applied to the other input.

The OPA678 is designed to be frequency compensated by a single capacitor connected from pin 5 to ground. Recommended compensation is shown in the Typical Performance Curve section. A small variable capacitor may be trimmed for best bandwidth, settling time, and gain peaking. Closed-loop gain/phase (Bode) plots are shown in the Typical Performance Curves.

OFFSET TRIM

The laser trimmed input offset voltage is low enough for many video and RF applications. Independent control of input offset will require that trim adjust current be summed into one or both inputs.

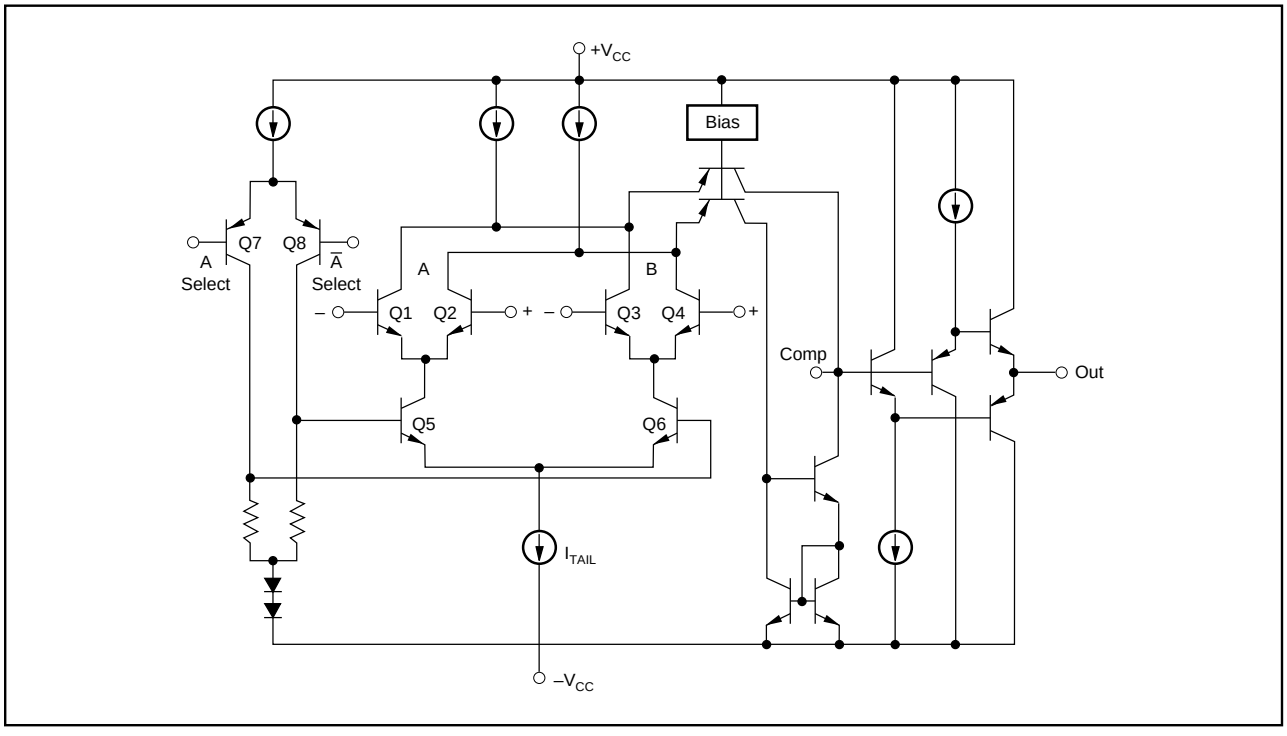


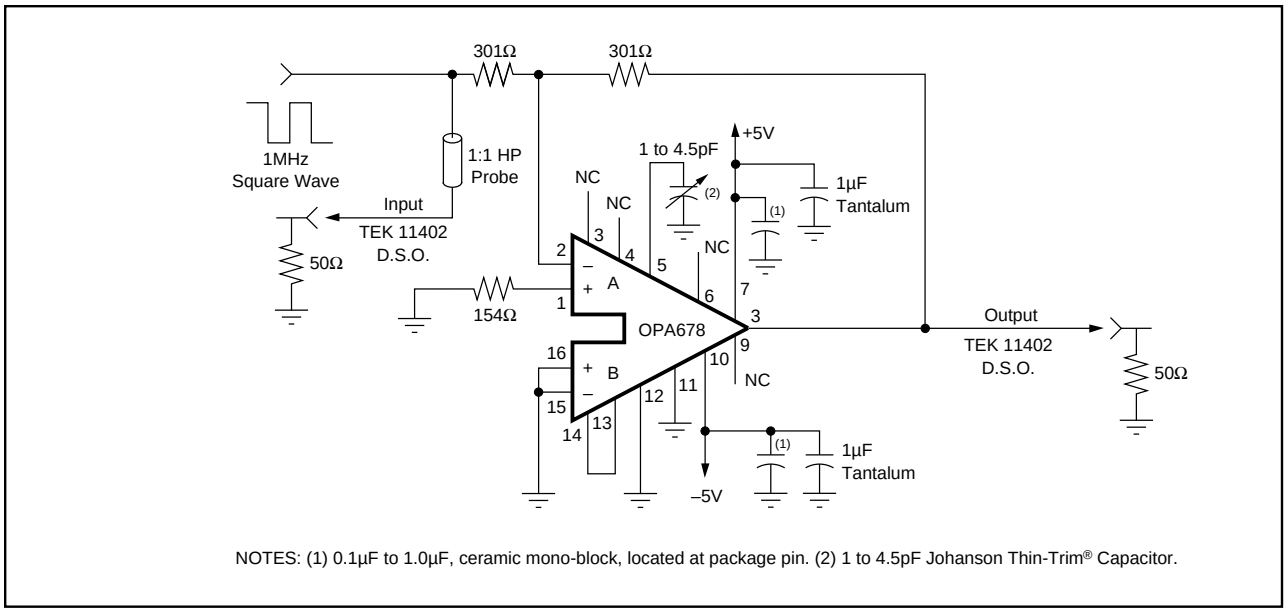
FIGURE 1. OPA678 Simplified Circuit Diagram.

APPLICATION TIPS

Wideband amplifier circuits require good layout techniques to be successful. The use of short, direct signal paths and heavy (2oz copper recommended) ground planes are absolutely necessary to achieve the performance level inherent in the OPA678. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems that plague all high-speed amplifiers when they are used in poor layouts. The OPA678 is no different in this respect—any amplifier with a gain bandwidth product of a few GHz requires some care be taken in its application.

Points to remember:

1. Use a heavy copper ground plane on the component side of your PC board. This provides a low inductance ground and it also conducts heat from active circuit package pins into ambient air by convection.
2. Bypass power supply pins directly at the active device. The use of monoblock or tantalum capacitors with very short leads is highly recommended. A 0.1µF in parallel with a 1.0µF will be optimum in most applications. The 0.1µF should be placed directly at the device's power supply leads.
3. When using the OPA678 in the unity gain voltage follower configuration it is recommended that a 100Ω resistor be connected from the output to the inverting input for optimum performance.
4. Signal paths should be short and direct. Feedback resistors, compensation capacitors, termination resistors, etc. should have lead lengths no longer than 1/4 inch (6cm).
5. Surface mount components (chip resistors, capacitors, etc.) have low inductance and are therefore recommended. Parasitic inductance and capacitance should be avoided if best performance is to be achieved.
6. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable range to about 1kΩ or on the high resistance end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon compensation resistors will be satisfactory.
7. Wirewound resistors (even "noninductive" types) are absolutely unacceptable in high frequency circuits.
8. Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its "load." Lowest distortion is achieved with high impedance loads.
9. PC board traces for signal and power lines should be wide to reduce impedance or inductance.
10. Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, the use of ±15V supplies will result in destruction.
11. Standard commercial test equipment has not been designed to test devices in the OPA678 speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.
12. High-speed amplifiers can drive only a limited amount of capacitance. If the load exceeds 10 to 20pF consider using a fast buffer or a small resistor to isolate the capacitance from the amplifier's output. Capacitive loads will cause loop instability if not compensated for.
13. Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears as a purely resistive impedance.
14. For clean, fast input selection the logic input pins should be terminated with appropriate resistors. Resistors should be connected from input selection pins to ground plane with short leads. Failure to terminate long lines will result in ringing and poor high frequency switching.
15. Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is required; there is no shortcut.



NOTES: (1) 0.1µF to 1.0µF, ceramic mono-block, located at package pin. (2) 1 to 4.5pF Johanson Thin-Trim® Capacitor.

FIGURE 2. OPA678 Settling Time Test Circuit.

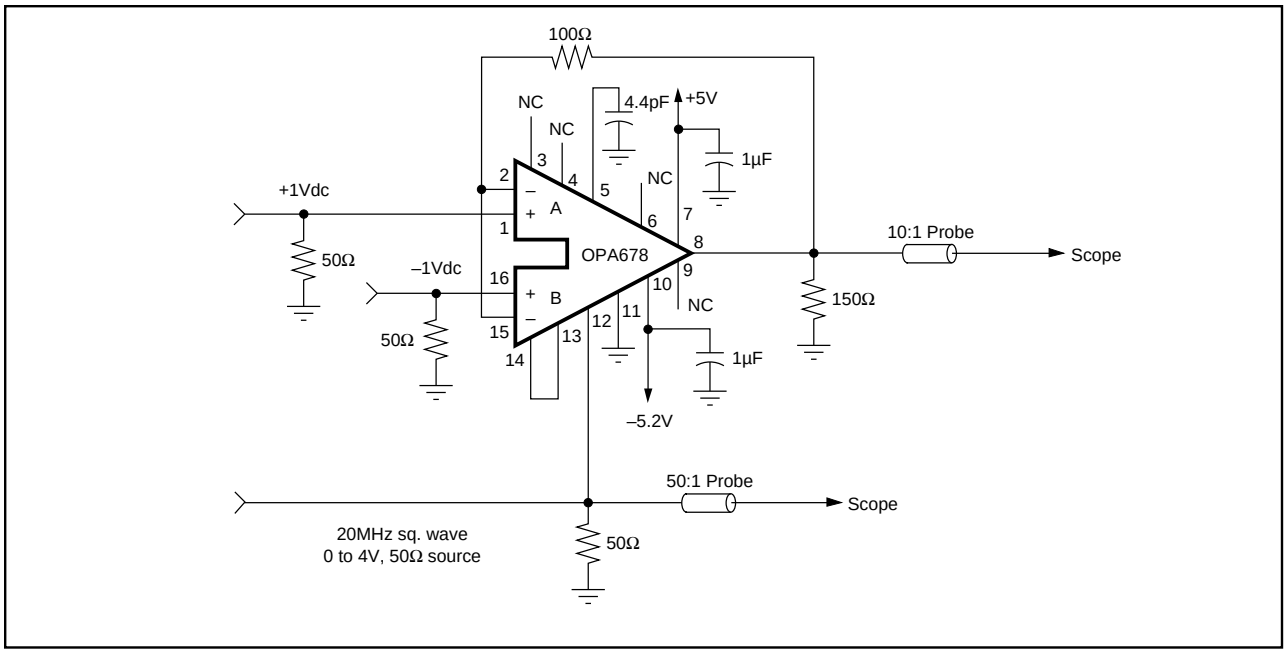


FIGURE 3. OPA678 (TTL) Input Selection Transition Time Test Circuit.

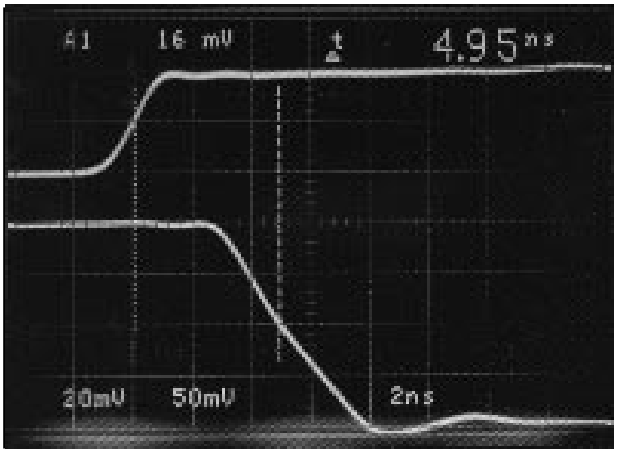


FIGURE 4. OPA678 (TTL) Input Selection Time. Input A to B. Larger output voltages will have slightly slower switching times due to more slewing of the op amp.

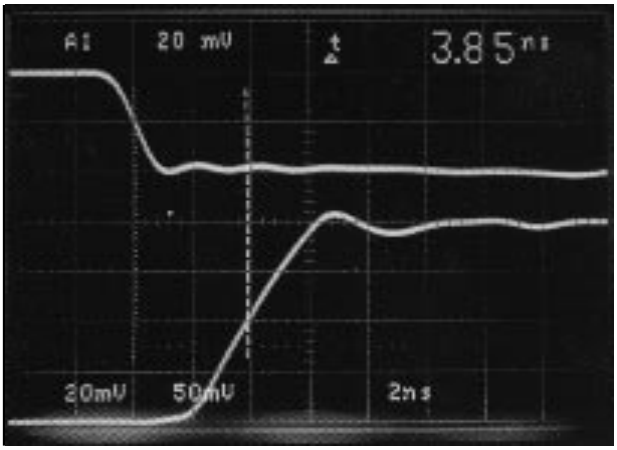


FIGURE 5. OPA678 (ECL) Input Selection Time. Input A to B. Larger output voltages will have slightly slower switching times due to more slewing of the op amp.

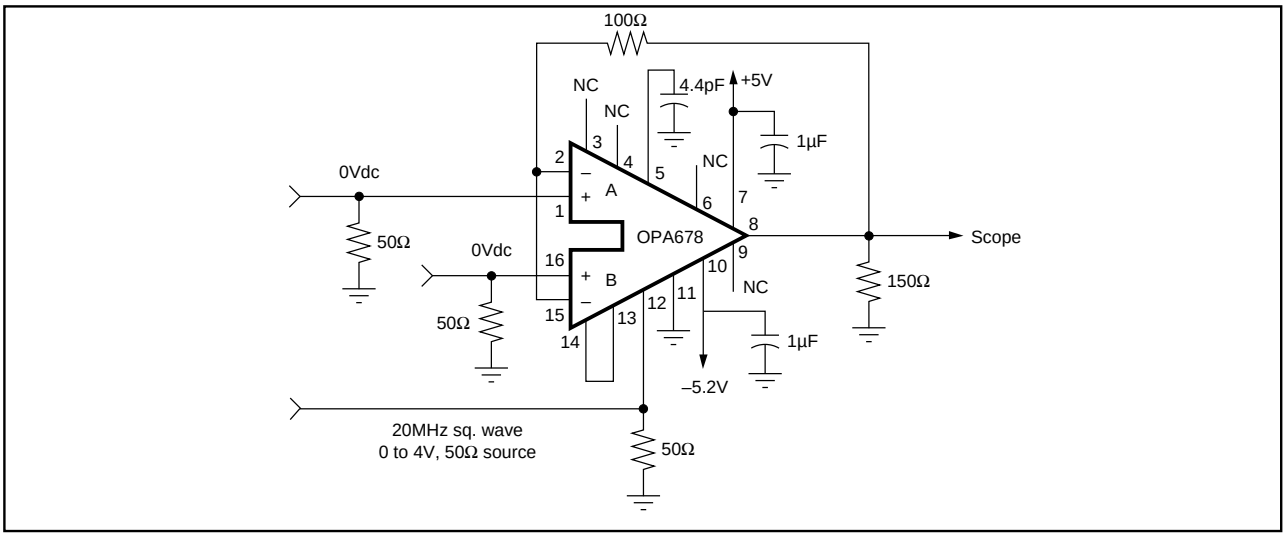


FIGURE 6. Channel Select Switching Transient Test Schematic.

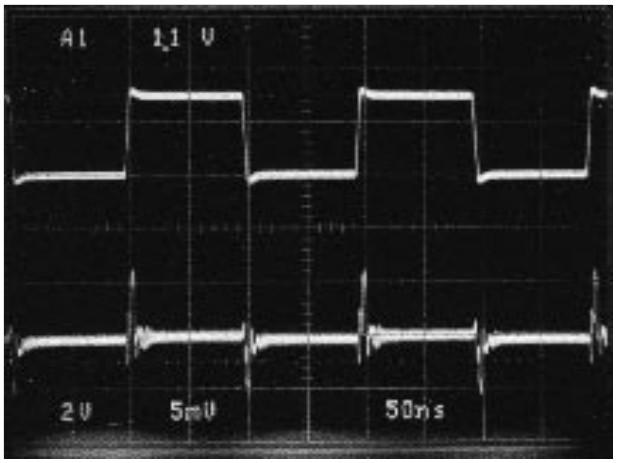
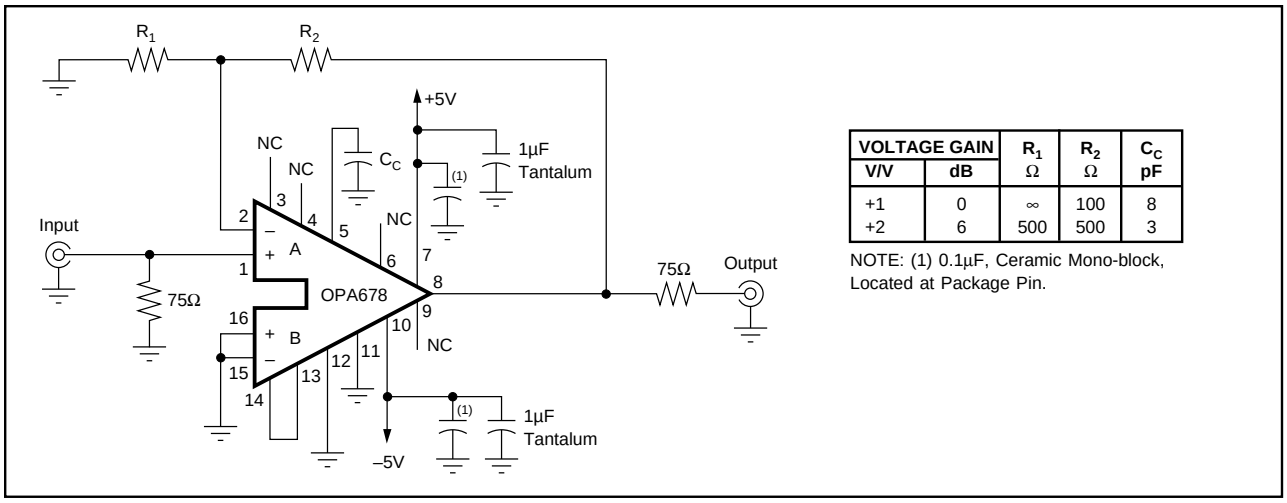


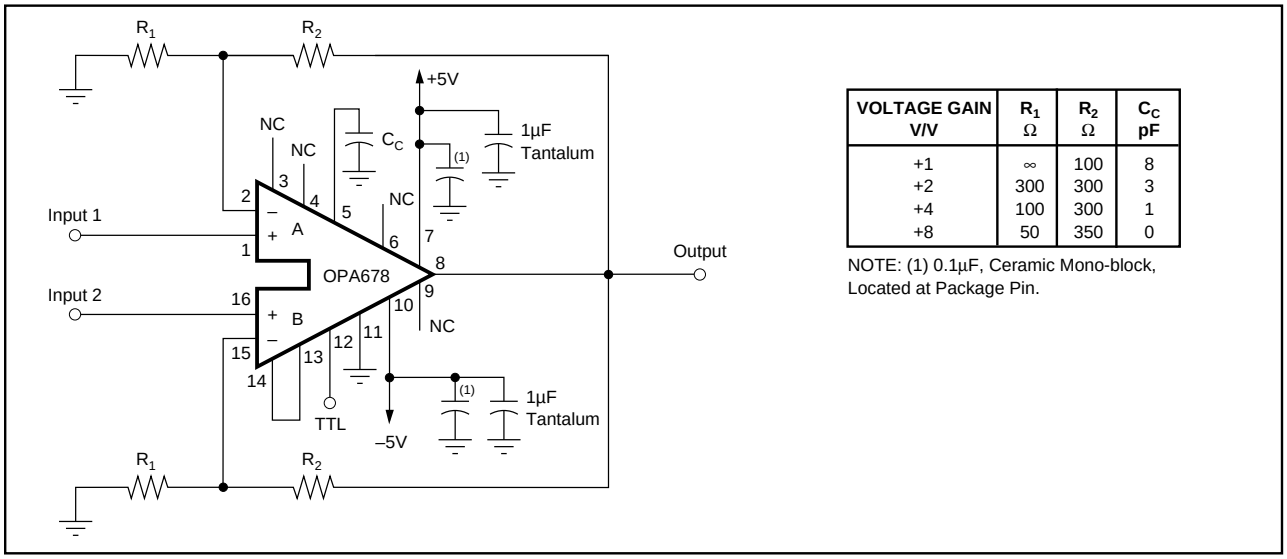
FIGURE 7. OPA678 Switching Transient. The switching transient levels will be lower for switching signals with slower rising edges.



VOLTAGE GAIN		R_1	R_2	C_C
V/V	dB	Ω	Ω	pF
+1	0	∞	100	8
+2	6	500	500	3

NOTE: (1) 0.1µF, Ceramic Mono-block, Located at Package Pin.

FIGURE 8. OPA678 used as Conventional Op Amp. A wideband video amplifier with 75Ω input and output impedance.



VOLTAGE GAIN	R_1	R_2	C_C
V/V	Ω	Ω	pF
+1	∞	100	8
+2	300	300	3
+4	100	300	1
+8	50	350	0

NOTE: (1) 0.1µF, Ceramic Mono-block, Located at Package Pin.

FIGURE 9. Two Input Multiplexer with Gain. This circuit can be used to multiplex I & Q signals into one sampling ADC.

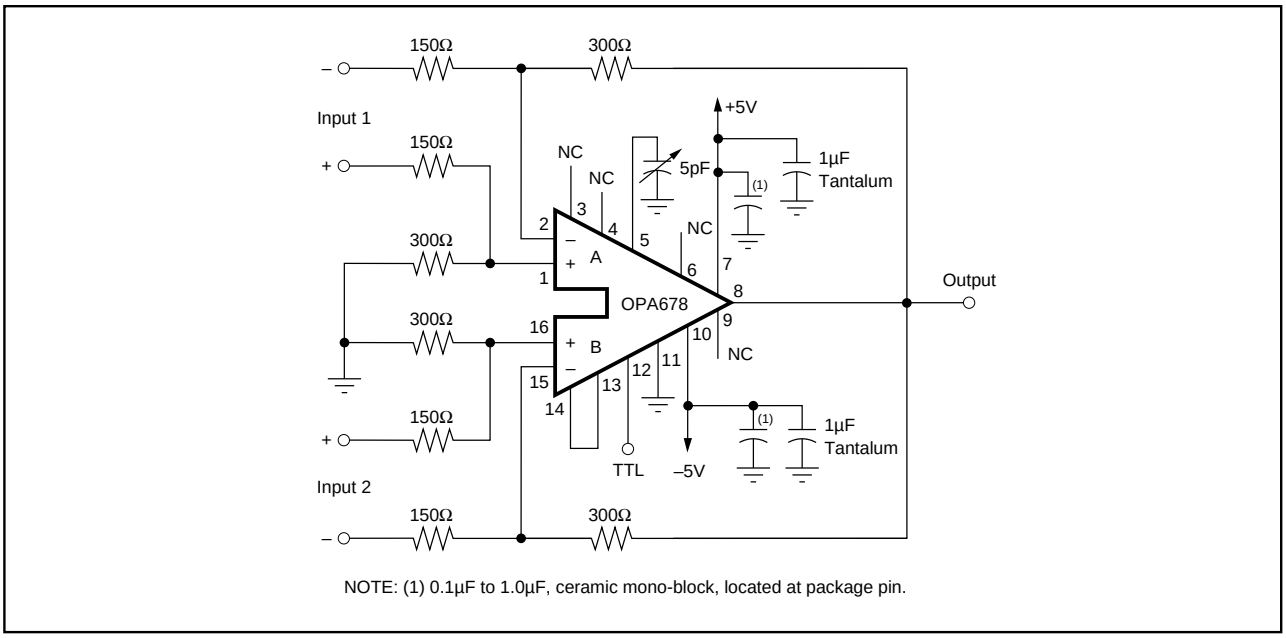
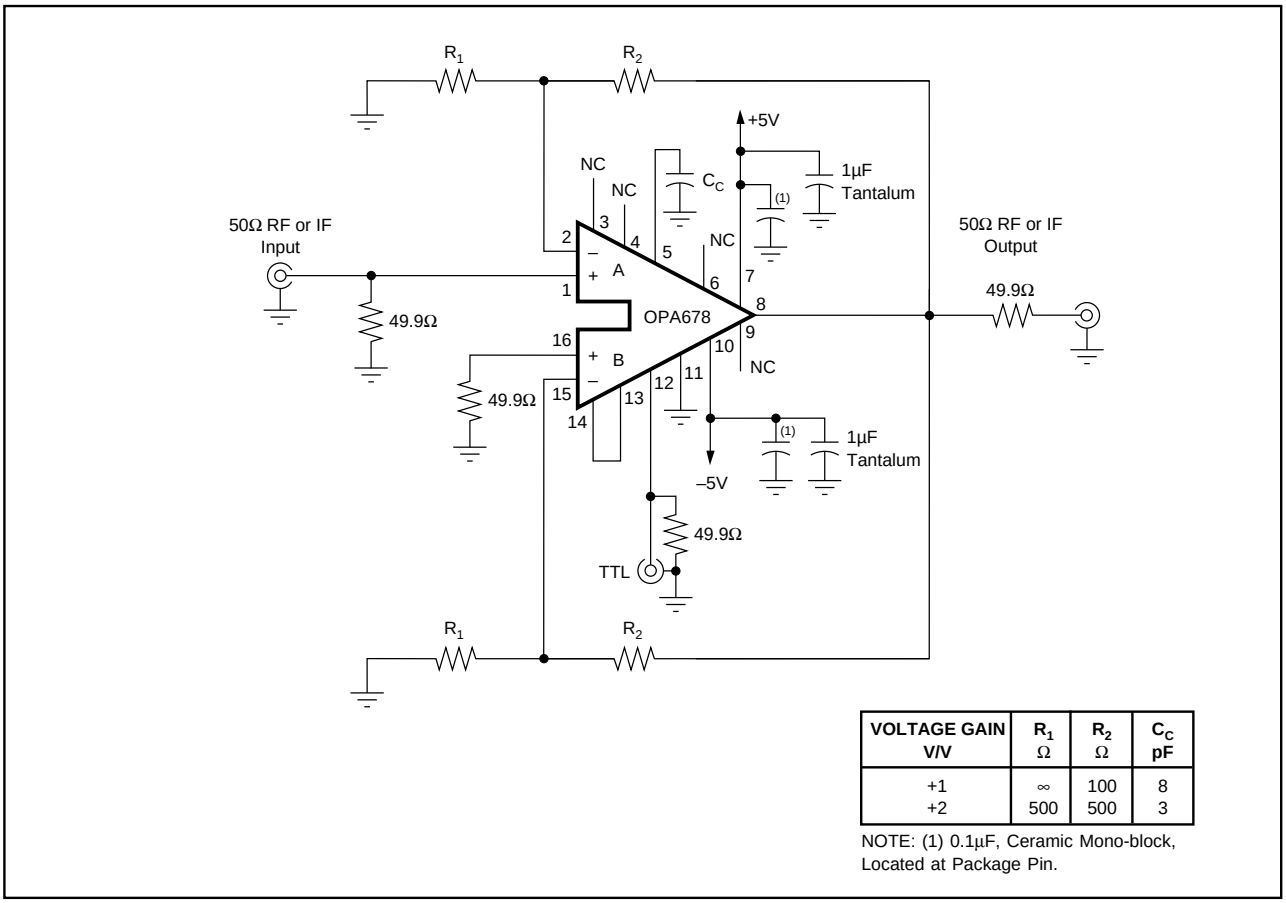
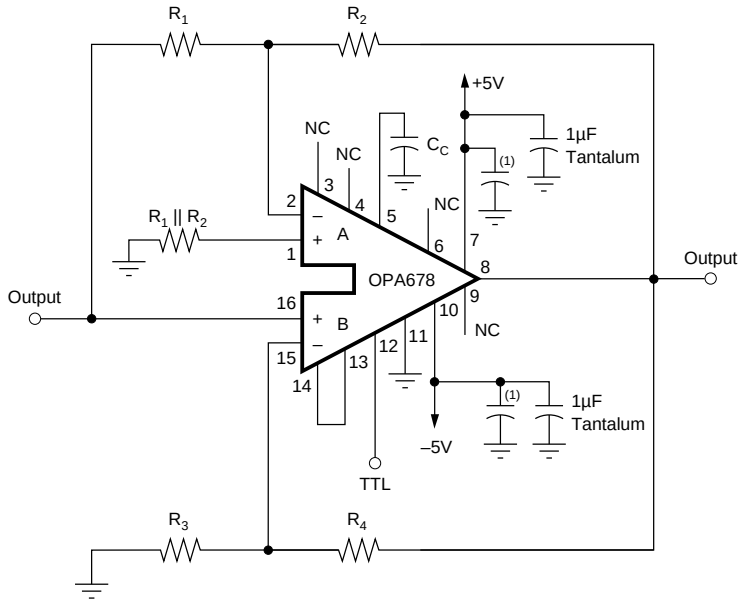


FIGURE 10. Differential Input Multiplexer with Gain of +2V/V.



VOLTAGE GAIN V/V	R_1 Ω	R_2 Ω	C_C pF
+1	∞	100	8
+2	500	500	3

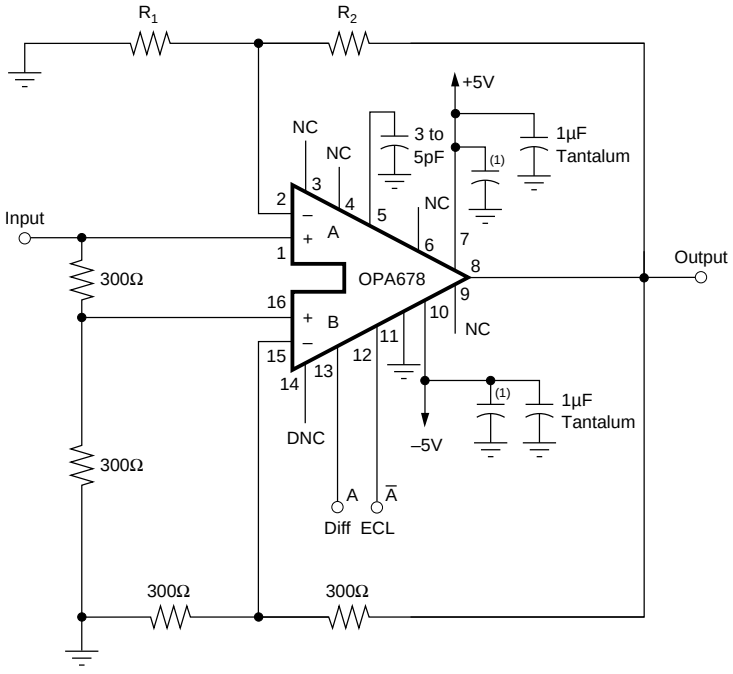
FIGURE 11. Receiver Noise Blanker: A Wideband Gated Video Amplifier.



VOLTAGE GAIN V/V	R_1 Ω	R_2 Ω	R_3 Ω	R_4 Ω	C_C pF
±2	100	200	200	200	4
±5	40	200	50	200	1

NOTE: (1) 0.1µF, Ceramic Mono-block, Located at Package Pin.

FIGURE 12. Synchronous Modulator/Demodulator (with Gain).



NOTE: (1) 0.1µF to 1.0µF, ceramic mono-block, located at package pin.

FIGURE 13. Very Fast Programmable Gain Amplifier with Voltage Gains of +1V/V and +2V/V (0dB and 6dB).

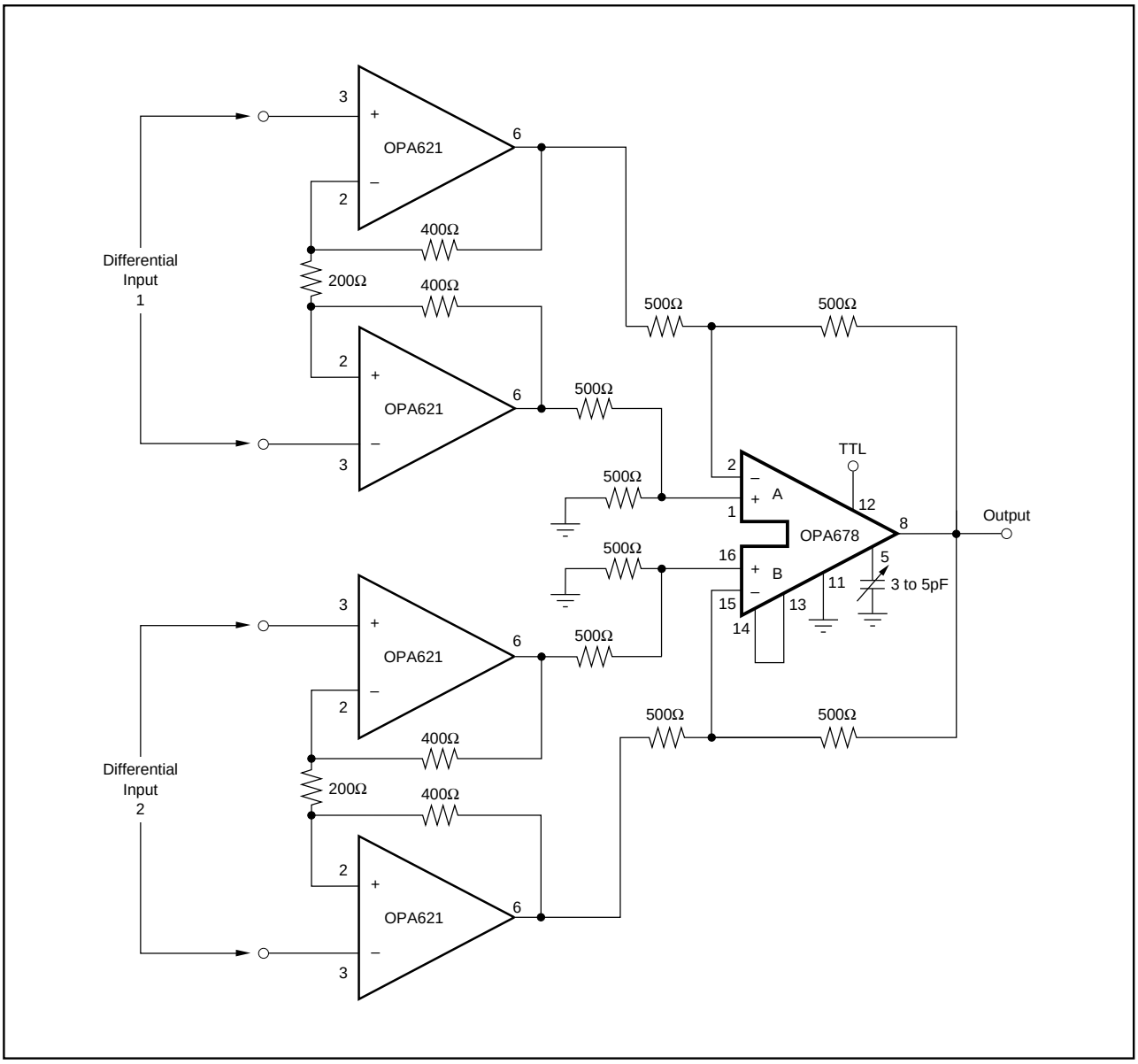
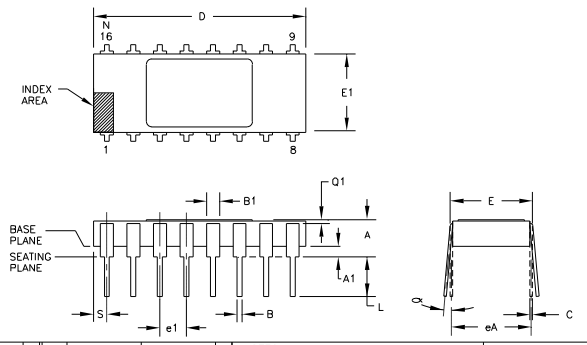


FIGURE 14. High Input Impedance Differential Input Multiplexer with Gain of 5V/V (14dB).

PACKAGE DRAWINGS

Package Number 109 - 16-Lead, Ceramic Side Braze DIP, .300 Wide



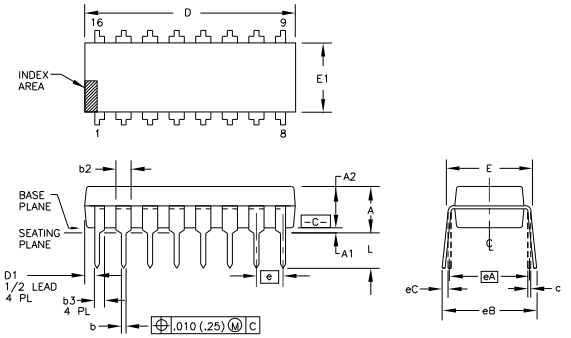
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45	
A1	.025	.055	0.64	1.40	
B	.015	.021	0.38	0.53	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	.770	.830	19.56	21.08	
E	.290	.325	7.37	8.26	
E1	.280	.310	7.11	7.87	6
e1	.100 TYP.		2.54 TYP.		2
eA	.300 TYP.		7.62 TYP.		2
L	.125	.175	3.18	4.45	
N	16		16		4
Q1	.010	--	0.25	--	
S	.020	.065	0.51	1.65	

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
α	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ109	REV.: D
JEDEC NUMBER: MO-36-AD	

Package Number 180 - 16-Pin Plastic, Single-Wide DIP



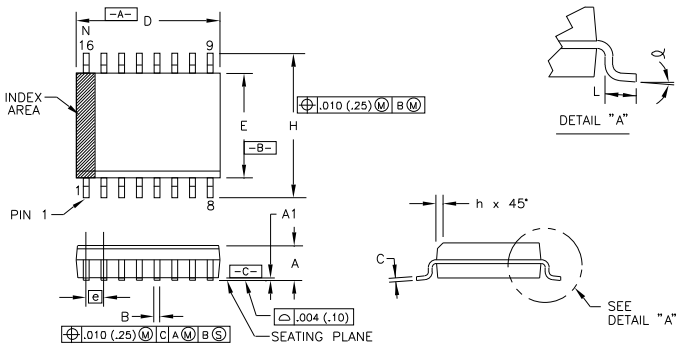
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.735	.775	18.67	21.34	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	16		16		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ180	REV.: F
JEDEC NUMBER: MS-001-BB	

Package Number 211 - 16-Lead SOIC



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0926	.1043	2.35	2.65	
A1	.004	.0118	0.10	0.30	
B	.013	.020	0.33	0.51	7
C	.0091	.0125	0.23	0.32	
D	.3977	.4133	10.10	10.50	2
E	.2914	.2992	7.40	7.60	3
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	4
L	.016	.050	0.40	1.27	5
N	16		16		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ211	REV.: E
JEDEC NUMBER: MS-013-AA	