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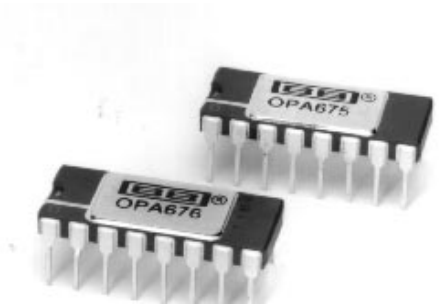


OPA675
OPA676

Wideband Switched-Input OPERATIONAL AMPLIFIER

FEATURES

- FAST SETTLING: 9ns (1%)
- WIDE BANDWIDTH: 185MHz (A_V = 10)
- LOW OFFSET VOLTAGE: ±250µV
- TWO LOGIC SELECTABLE INPUTS
- FAST INPUT SWITCHING: 8ns (TTL)
- 16-PIN DIP PACKAGE

APPLICATIONS

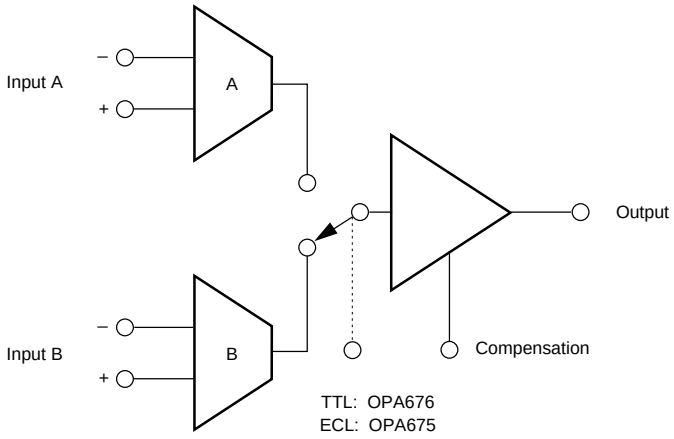
- PROGRAMMABLE-GAIN AMPLIFIER
- FAST 2-INPUT MULTIPLEXER
- SYNCHRONOUS DEMODULATOR
- PULSE/RF AMPLIFIERS
- VIDEO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

The OPA675 and OPA676 are wideband monolithic operational amplifiers with two independent differential inputs. Either input can be selected by an external logic signal. The OPA675 is compatible with ECL logic while the OPA676 is TTL compatible. Both amplifiers are externally compensated and feature very fast input selection speed: ECL = 4ns, TTL = 6ns. This amplifier features fully symmetrical differential inputs due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA675/676 may be used in all op amp applications requiring high speed and precision.

Low distortion and crosstalk make these amplifiers suitable for RF and video applications.

The OPA675 and OPA676 are available in KG (0°C to +70°C) and SG (–55°C to +125°C) grades. All grades are packaged in a 16-pin DIP.



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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG, SG MIN	OPA675/676JG, SG TYP	OPA675/676JG, SG MAX	OPA675/676KG MIN	OPA675/676KG TYP	OPA675/676KG MAX	UNITS
INPUT NOISE[1]								
Voltage: f_O = 10Hz	R_S = 0Ω		27			*		nV/√Hz
f_O = 100Hz			10			*		nV/√Hz
f_O = 1kHz			3.8			*		nV/√Hz
f_O = 10kHz			2.6			*		nV/√Hz
f_O = 100kHz			2.4			*		nV/√Hz
f_B = 10Hz to 10MHz			7.9			*		µVrms
Current: f_O = 10Hz to 1MHz			2.7			*		pA/√Hz
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0VDC		±500	±2mV		±250	±1mV	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	±V_{CC} = 4.5V to 5.5V	65	86		70	*		dB
BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0VDC		23	35		*	30	µA
OFFSET CURRENT[1]								
Input Offset Current	V_{CM} = 0VDC		0.8	5		*	*	µA
INPUT IMPEDANCE[1]								
Differential			4k || 2			*		Ω || pF
Common-Mode			10^5 || 5			*		Ω || pF
INPUT VOLTAGE RANGE[1]								
Common-Mode Input Range		±1.25	±2.5		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	75	100		85	*		dB
OPEN LOOP GAIN, DC[1]								
Open-Loop Voltage Gain		65	70		*	*		dB
FREQUENCY RESPONSE								
Closed-Loop Bandwidth	Gain = +2V/V		100			*		MHz
	Gain = +5V/V		145			*		MHz
	Gain = +10V/V		185			*		MHz
	Gain = +50V/V		60			*		MHz
Crosstalk	Gain = +10V/V, f = 100kHz		–100			*		dBC[2]
	f = 1MHz		–80			*		dBC
	f = 10MHz		–68			*		dBC
	f = 100MHz		–35			*		dBC
Harmonic Distortion: 10MHz	G = +10V/V, R_L= 50Ω, V_O = 0.5Vp-p							
	Second Harmonic		–61			*		dBC
	Third Harmonic		–73			*		dBC
Full Power Response	V_O = 2.5Vp-p, Gain = +10V/V	25	44		30	*		MHz
Slew Rate	Gain = +10V/V	200	350		240	*		V/µs
Settling Time: 1%			9			*		ns
0.1%	Gain = +10V/V		15			*		ns
0.01%	0.625V Output Step		25			*		ns
INPUT SELECTION[3]								
Transition Time	ECL: OPA675		5			*		ns
50% In to 50% Out	TTL: OPA676		7.5			*		ns
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic “LO”	0		+0.8	*		*	V
V_{IH}	Logic “HI”	+2.0		+5	*		*	V
I_{IL}	Logic “LO”, V_{IL} = 0V		–0.05	–0.2		*	*	mA
I_{IH}	Logic “HI”, V_{IH} = +2.7V		1	20		*	*	µA
ECL Logic Levels: V_{IL}	Logic “LO”	–1.81		–1.475	*		*	V
V_{IH}	Logic “HI”	–1.15		– 0.88	*		*	V
I_{IL}	Logic “LO”, V_{IL} = –1.6V		–50	–100		*	*	µA
I_{IH}	Logic “HI”, V_{IH} = –1.0V		–50	–100		*	*	µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.1	±2.6		*	*		V
	R_L = 50Ω	+1.25	+1.8		*	*		V
		–0.95	–1.1		–1.0	*		V
Current Output			±30			*		mA
Output Resistance	1MHz, Open-Loop, C_C = 5pF		5			*		Ω
Load Capacitance Stability	Gain = +2V/V		50			*		pF
Short Circuit Current	Continuous to Gnd		+45			*		mA
			–25			*		mA

* Same specifications as for JG.

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA675/676JG, SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Rated Voltage	$\pm V_{CC}$		5			*		VDC
Derated Performance	$\pm V_{CC}$	4.5		6.5	*		*	VDC
Current, Quiescent	I_O = 0mADC		22	30		*	*	mA
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	–55		+125				°C
Operating:	Ambient Temp JG, KG, SG	–55		+125	*		*	°C
θ_{JA}			125			*		°C/W

* Same specifications as for JG.

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

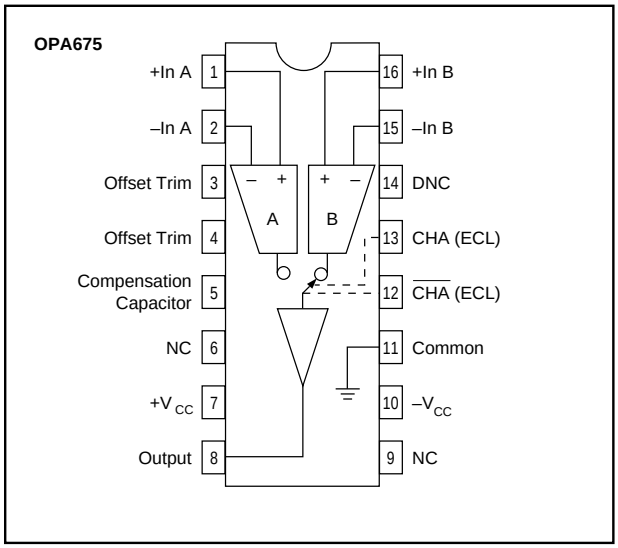
At V_{CC} = ±5VDC, R_L = 150Ω, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

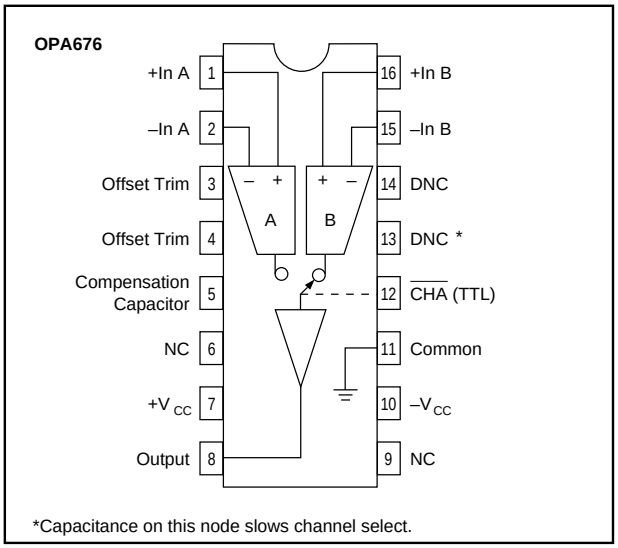
PARAMETER	CONDITIONS	OPA675/676JG, SG			OPA675/676KG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	Ambient Temp JG, KG	0		+70	*		*	°C
	SG	–55		+125				°C
OFFSET VOLTAGE								
Average Drift	T_A = T_{MIN} to T_{MAX}		±3	±10		±1	±5	µV/°C
Supply Rejection	$\pm V_{CC}$ = 4.5V to 5.5V	60	85		65	*		dB
BIAS CURRENT								
Input Bias Current	V_{CM} = 0VDC		29	50		*	*	µA
OFFSET CURRENT								
Input Offset Current	V_{CM} = 0VDC		0.8	10		*	*	µA
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.0	±2.3		*	*		V
Common-Mode Rejection	V_{IN} = ±0.5VDC, V_O = ±1.25V	60	80		65	*		dB
OPEN LOOP GAIN, DC								
Open-Loop Voltage Gain		60	68		63	69		dB
DIGITAL INPUT								
TTL Logic Levels: V_{IL}	Logic “LO”	0		+0.8	*		*	V
V_{IH}	Logic “HI”	+2.0		+5	*		*	V
I_{IL}	Logic “LO”, V_{IL} = 0V		–0.08	–0.4		*	*	mA
I_{IH}	Logic “HI”, V_{IH} = +2.7V		5	50		*	*	µA
ECL Logic Levels: V_{IL}	Logic “LO”	–1.81		–1.475	*		*	V
V_{IH}	Logic “HI”	–1.15		–0.88	*		*	V
I_{IL}	Logic “LO”, V_{IL} = –1.6V		–50			*		µA
I_{IH}	Logic “HI”, V_{IH} = –1.0V		–50			*		µA
RATED OUTPUT								
Voltage Output	R_L = 150Ω	±2.0	±2.5		*	*		V
	R_L = 50Ω	+1.25	+1.6		*	*		V
		–0.8	–1.0		–0.9	*		V
POWER SUPPLY								
Current, Quiescent	I_O = 0mADC		25	35		*	*	mA

* Same specifications as for JG.

NOTES: (1) Specifications are for both inputs (A and B). (2) dBC = Level referred to carrier-input signal. (3) Switching time from application of digital logic signal to input signal selection.

PIN CONFIGURATIONS





PIN ASSIGNMENTS: OPA675

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	$\overline{\text{CHA}}$ (ECL)
5	Compensation Capacitor	12	$\overline{\text{CHA}}$ (ECL)
6	NC	11	Common
7	$+V_{CC}$	10	$-V_{CC}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

PIN ASSIGNMENTS: OPA676

1	+In A	16	+In B
2	–In A	15	–In B
3	Offset Trim	14	DNC
4	Offset Trim	13	$\overline{\text{DNC}}$
5	Compensation Capacitor	12	$\overline{\text{CHA}}$ (TTL)
6	NC	11	Common
7	$+V_{CC}$	10	$-V_{CC}$
8	Output	9	NC

DNC = Do Not Connect NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Differential Input Voltage	Total V_{CC}
Input Voltage Range (Analog and Digital)	$\pm V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit to Ground (+25°C)	Continuous to ground
Junction Temperature	+175°C

ORDERING INFORMATION

OPA675 ( ) ( )
OPA676 ( ) ( )

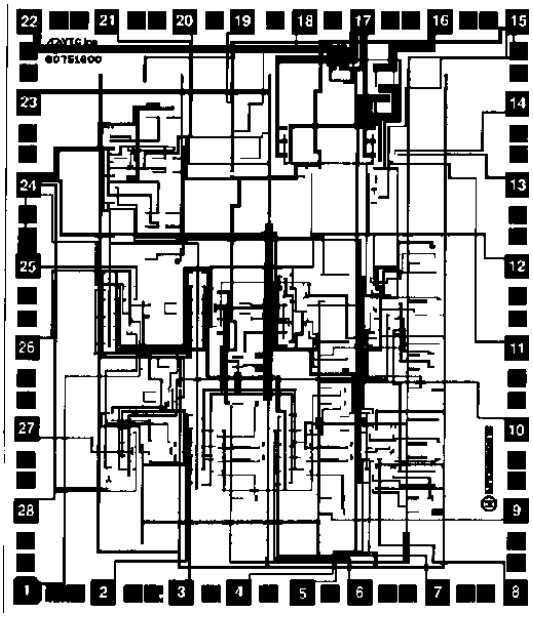
Basic Model Number
Performance Grade Code
J, K: 0°C to +70°C
S: –55°C to +125°C
Package Code
G: 16-pin Ceramic DIP

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA675/76JG	16-Pin Hermetic DIP	109
OPA675/76SG	16-Pin Hermetic DIP	109
OPA675/76KG	16-Pin Hermetic DIP	109

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DICE INFORMATION



OPA675/676 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	TTL Set	15	$+V_{CC}$
2	$-In_B$	16	$+V_{CC}$
3	$+In_B$	17	V_{OUT}
4	NC	18	NC
5	NC	19	NC
6	$+In_A$	20	NC
7	$-In_A$	21	NC
8	NC	22	$-V_{CC}$
9	V_{OS} Adjust	23	$-V_{CC}$
10	V_{OS} Adjust	24	Ground
11	NC	25	CHA (TTL)
12	Comp Cap	26	ECL_{OUT}
13	NC	27	CHA (ECL)
14	NC	28	CHA (ECL)

NC: No Connection (Do Not Connect). **OPA675**-Do not use pads 1, 25, 26. **OPA676**-Connect pad 26 to pad 27. Connect pad 1 to pad 28.

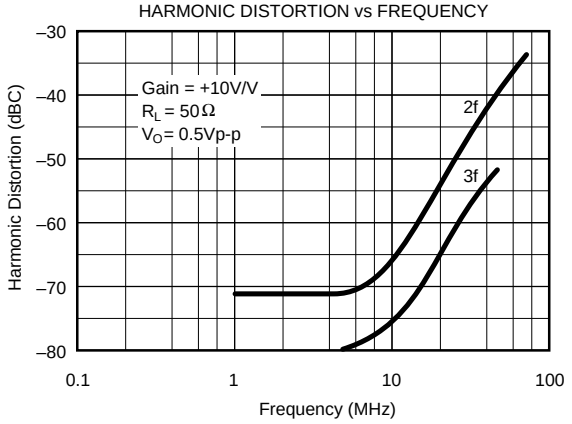
Substrate Bias: $-V_{CC}$

MECHANICAL INFORMATION

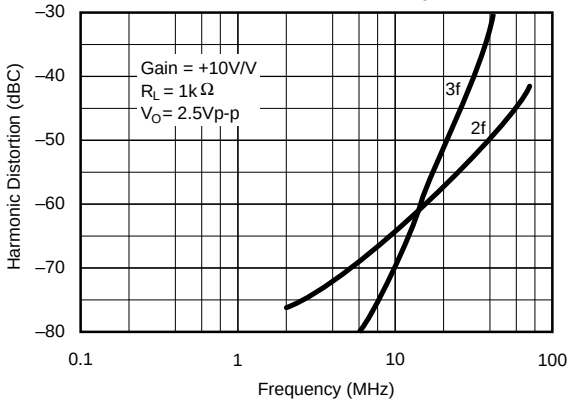
	MILS (0.001")
Die Size	103 x 90 ±5
Die Thickness	20 ±3

TYPICAL PERFORMANCE CURVES

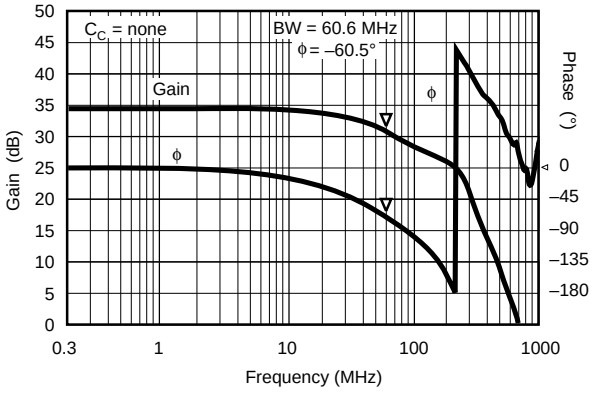
SMALL SIGNAL
HARMONIC DISTORTION vs FREQUENCY



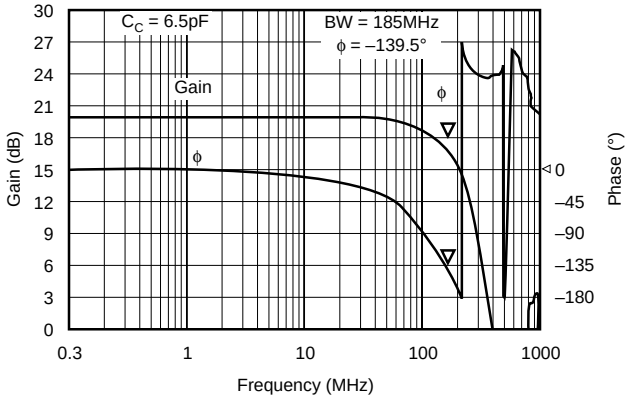
LARGE SIGNAL
HARMONIC DISTORTION vs FREQUENCY



A_V = +50V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

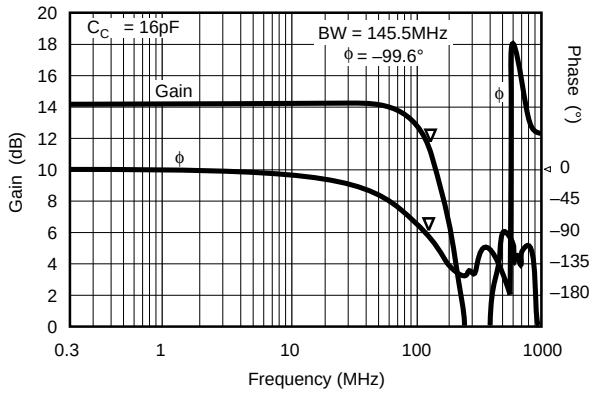


A_V = +10V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH

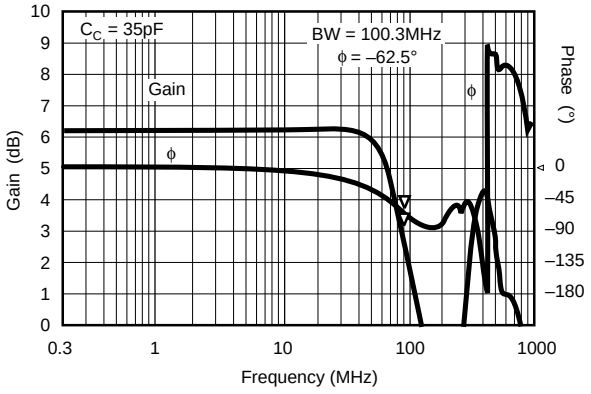


TYPICAL PERFORMANCE CURVES (CONT)

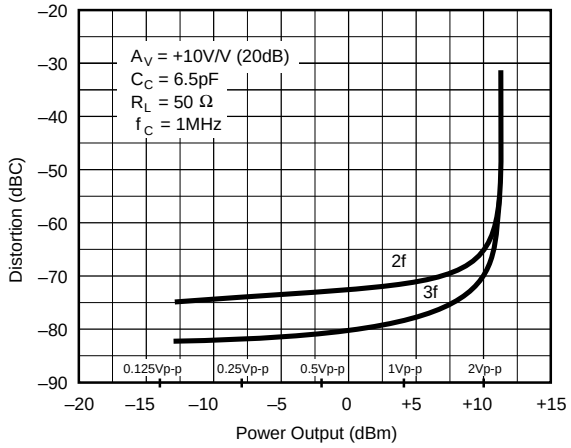
A_V = +5V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



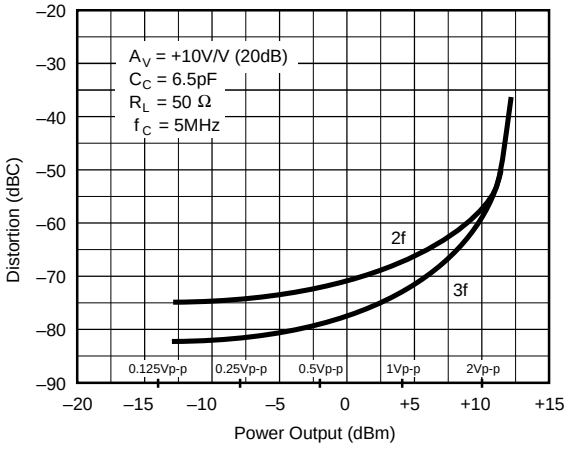
A_V = +2V/V CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



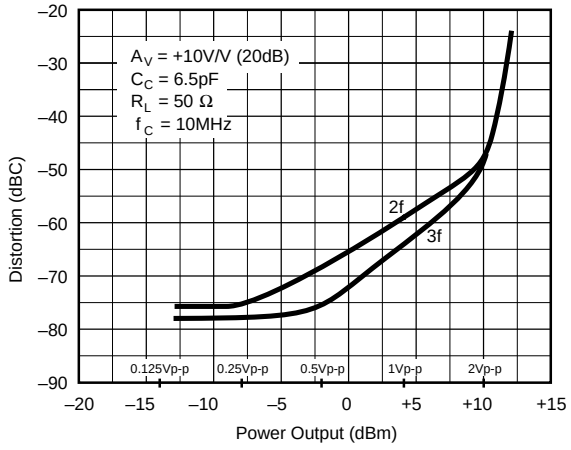
1MHz HARMONIC DISTORTION vs POWER OUTPUT



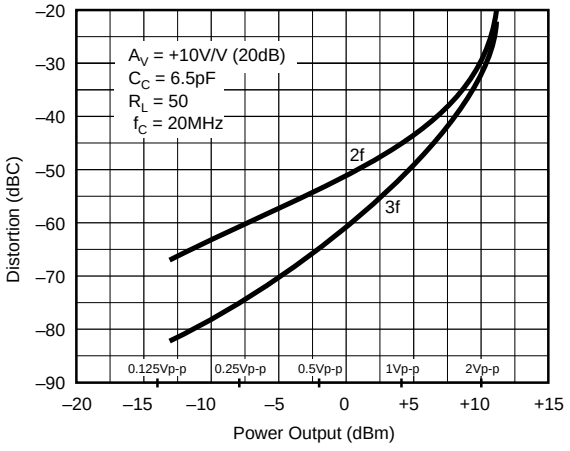
5MHz HARMONIC DISTORTION vs POWER OUTPUT



10MHz HARMONIC DISTORTION vs POWER OUTPUT

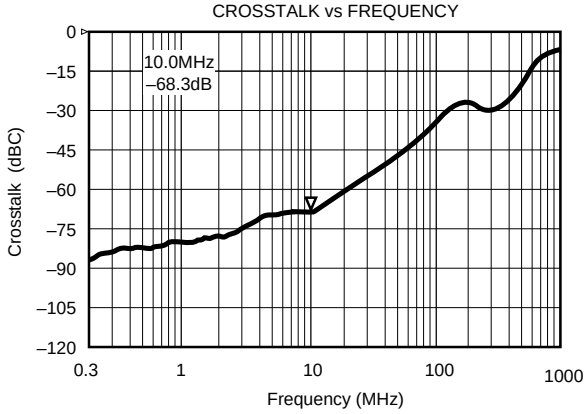


20MHz HARMONIC DISTORTION vs POWER OUTPUT

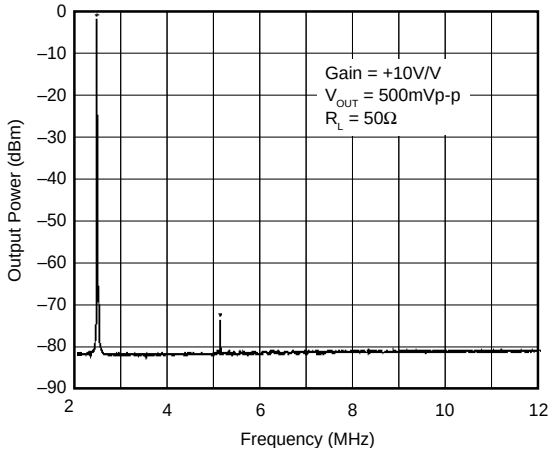


TYPICAL PERFORMANCE CURVES (CONT)

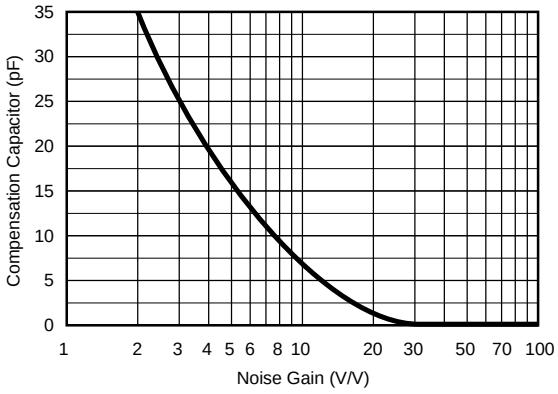
CHANNEL-TO-CHANNEL CROSSTALK vs FREQUENCY



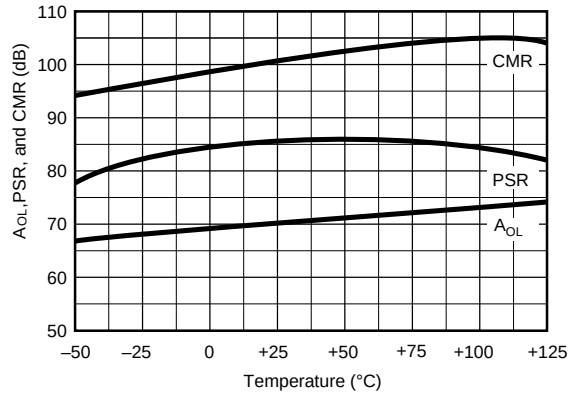
2.5MHz SMALL-SIGNAL HARMONIC DISTORTION SPECTRUM



NOMINAL FREQUENCY COMPENSATION vs NOISE GAIN



OPEN-LOOP GAIN, CMR AND PSR vs TEMPERATURE



THEORY OF OPERATION

An OPA675 simplified circuit is shown in Figure 1. It is a "classical" high-speed op-amp architecture with one important exception — the amplifier has two ECL logic selectable differential input stages. An appropriate differential ECL logic signal on A and $\overline{A}$ (labeled B Select) will turn on either Q5 or Q6, steering operating (tail) current to either differential input pair Q1 and Q2 or Q3 and Q4. The input pair receiving the tail current operates as a conventional op-amp input stage while the de-selected input pair receiving no tail current appears as an open circuit. The de-selected inputs have only a few pF parasitic capacitance and in the off condition exhibit only a very low leakage (bias) current of about 100pA. Two feedback networks can be connected to each input separately allowing a wide range of circuit applications. The feedback network connected to the selected input operates in a normal op amp fashion while the feedback network connected to the de-selected input is totally inactive, appearing only as an additional load to the amplifier's output stage.

The switched-input op amp (SWOP AMP) circuit of the OPA676 is basically the same as the OPA675 but a TTL compatible level shifter (Figure 2) has been added to its input selection logic circuit.

Standard TTL (OPA676) and ECL (OPA675) logic levels may be applied to each input selection circuit but only

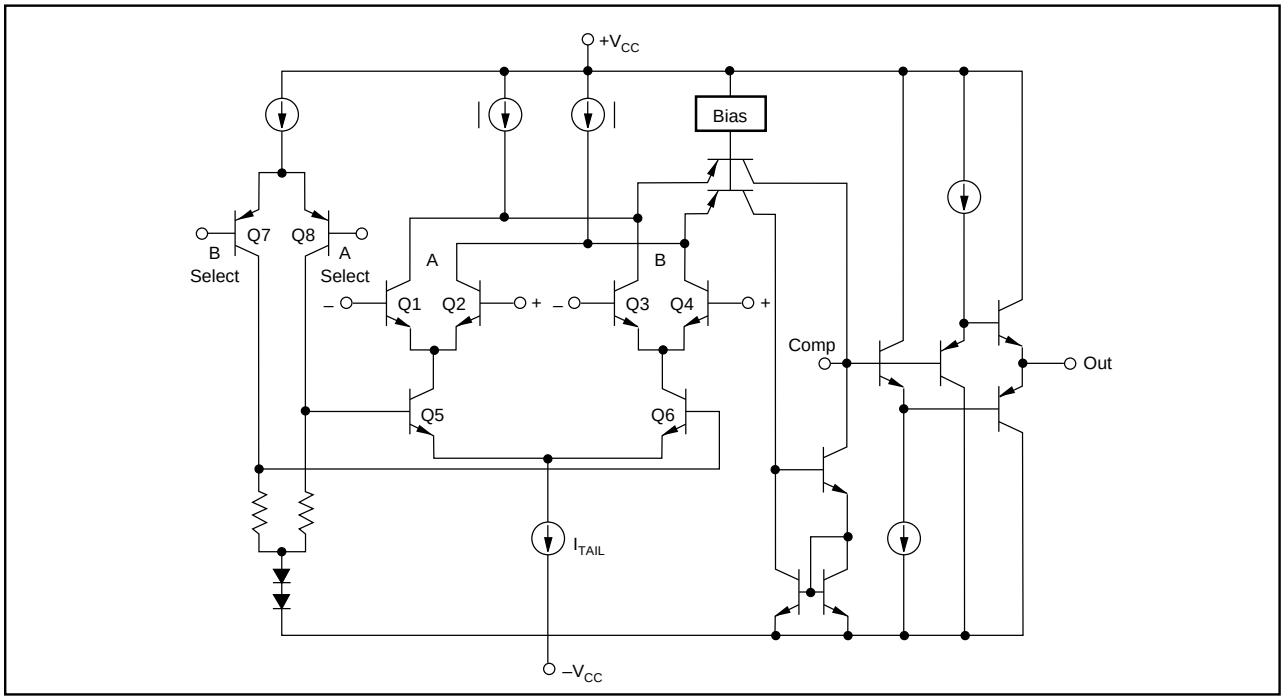


FIGURE 1. OPA675 Simplified Circuit Diagram.

350mV is typically required to switch between inputs. This logic input sensitivity allows simpler high-speed logic driver circuitry and it minimizes digital noise coupling into adjacent wideband analog circuitry and allows single ended ECL inputs to be used with V_{BB} applied to the other input.

The OPA675 and OPA676 are designed to be frequency compensated by a single capacitor connected from pin 5 to ground. Recommended compensation is shown in Typical Performance Curves. A small variable capacitor may be trimmed for best bandwidth, settling time, and gain peaking. This amplifier is designed for optimum performance in gains of 5V/V to 20V/V, but it can also be used over a far wider range of gains with excellent results. Closed-loop gain/phase (Bode) plots are shown in the Typical Performance Curves.

OFFSET TRIM

Input offset voltage is low enough for many video applications. If desired, offset voltage can be trimmed with a 1kΩ potentiometer connected to $+V_{CC}$. Trimming offset voltage in this manner will effect both input A and input B; independent control of input offset will require that trim adjust current be summed into one or both inputs. This technique is shown in a few applications circuits on the pages to follow.

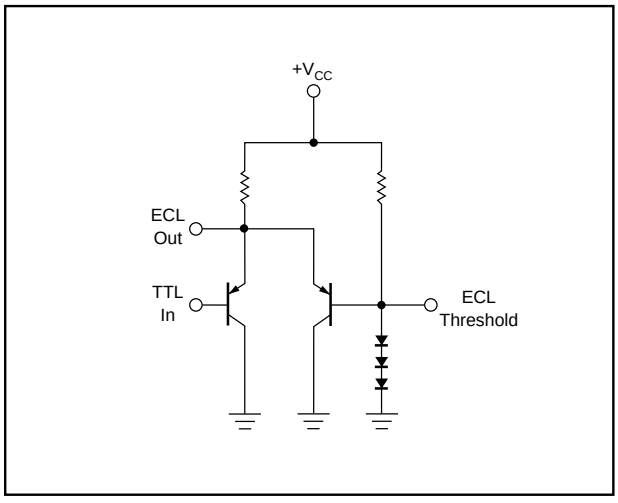


FIGURE 2. Internal OPA676 TTL Logic Level Shifter.

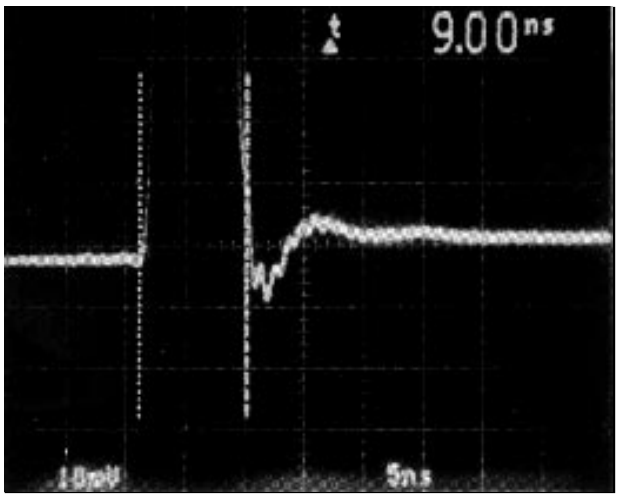


FIGURE 3. 1% Settling Time.

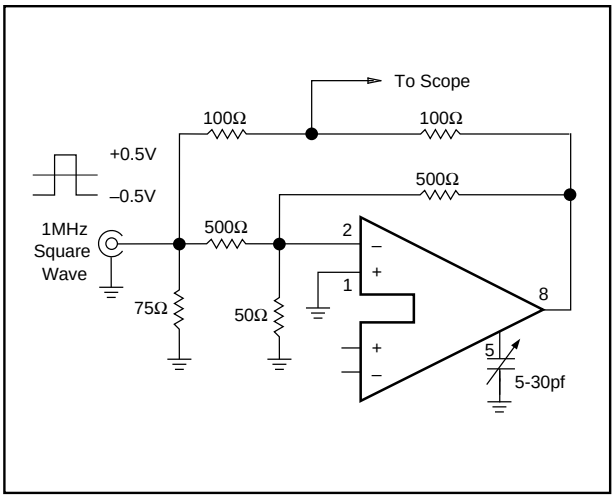


FIGURE 4. OPA675/676 Settling Time Test Circuit.

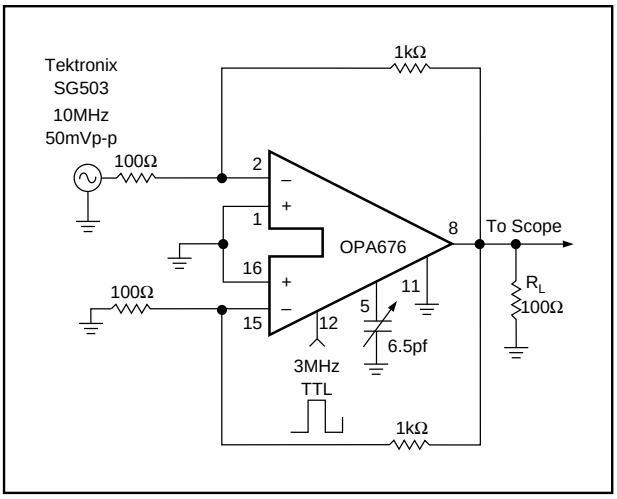


FIGURE 5. OPA676 Input Selection Transition Time Test Circuit.

APPLICATION TIPS

Wideband amplifier circuits require good layout techniques to be successful. The use of short, direct signal paths and heavy (2 oz. copper recommended) ground planes are absolutely necessary to achieve the performance level inherent in the OPA675/676. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems that plague all high-speed amplifiers when they are used in poor layouts. The OPA675 and OPA676 are no different in this respect—any amplifier with a gain bandwidth product of a few GHz requires some care be taken in its application.

Points to remember:

1. Use a heavy copper ground plane on the component side of your PC board. This provides a low inductance ground and it also conducts heat from active circuit package pins into ambient air by convection.
2. Bypass power supply pins directly at the active device. The use of tantalum capacitors (1 to 10μF/10V) with very short leads is highly recommended. Supply pins should not be left unbypassed.
3. Signal paths should be short and direct. Feedback resistors, compensation capacitors, termination resistors, etc., should have lead lengths no longer than 1/4 inch (6cm).
4. Surface-mount components (chip resistors, capacitors, etc.) have low inductance and are therefore recommended. Parasitic inductance and capacitance should be avoided if best performance is to be achieved.
5. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable range to about 1kΩ or on the high resistance end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon compensation resistors will be satisfactory.
6. Wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high frequency circuits.
7. Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its "load." Lowest distortion is achieved with high impedance loads.
8. PC board traces for signal and power lines should be wide to reduce impedance or inductance.
9. Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, the use of ±15V supplies will result in destruction.
10. Standard commercial test equipment has not been designed to test devices in the OPA675/676 speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.
11. High-speed amplifiers can drive only a limited amount of capacitance. If the load exceeds 10 to 20pF consider using a fast buffer or a small resistor to isolate the capacitance from the amplifier's output. Capacitive loads will cause loop instability if not compensated for.
12. Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears as a purely resistive impedance.
13. For clean, fast input selection the logic input pins should be terminated with appropriate resistors. Resistors should be connected from input selection pins to ground plane with short leads. Failure to terminate long lines will result in ringing and poor high frequency switching.
14. Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is required; there is no shortcut.

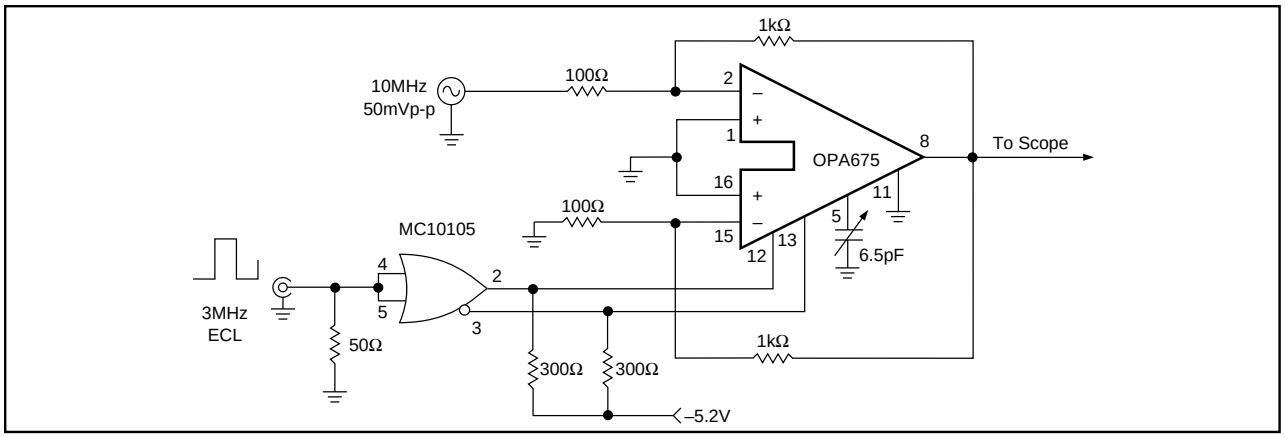


FIGURE 6. OPA675 Input Selection Transition Time Test Circuit.

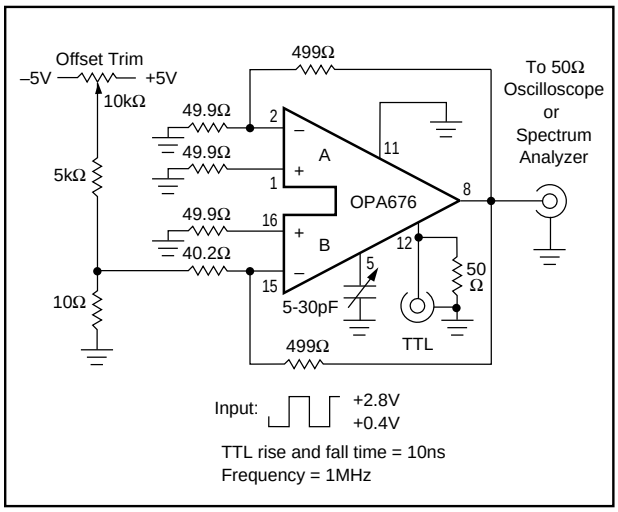


FIGURE 7. OPA676 Carrier Feedthrough and Switching Transient Test Circuit.

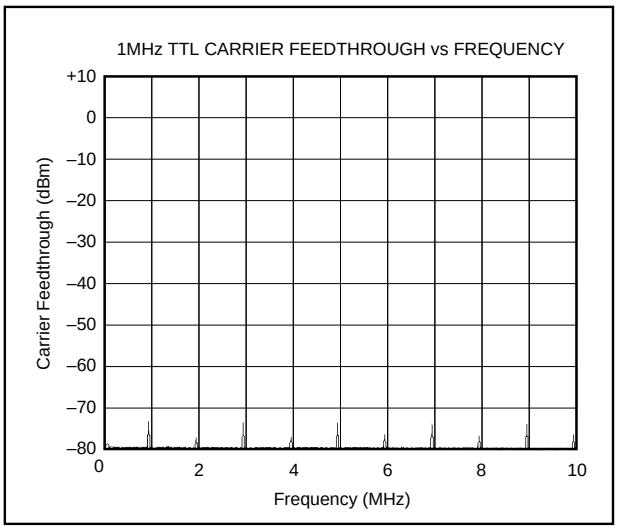


FIGURE 9. Carrier Feedthrough from 1MHz TTL Logic. Offset Trimmed for Maximum Carrier Rejection

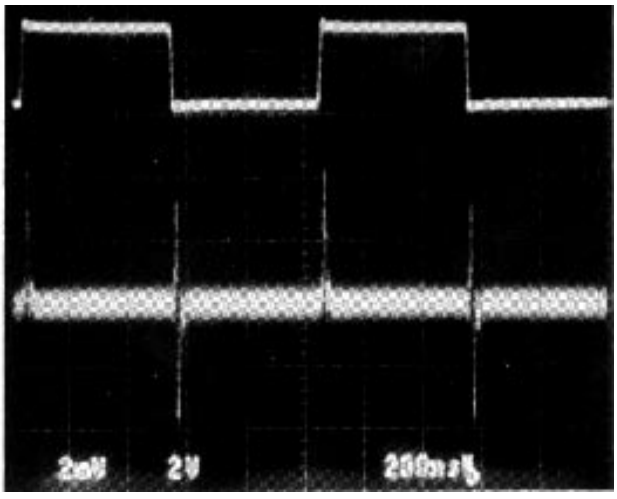


FIGURE 8. OPA676 Switching Transient. Top Trace: TTL Input (2V/cm). Bottom Trace: Amplifier Output (2mV/cm). Input B Offset Voltage has been Trimmed to Match Input A Offset Voltage.

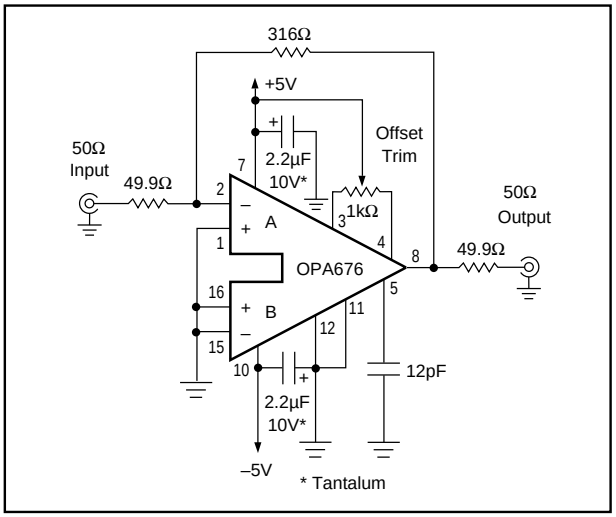


FIGURE 10. OPA676 Used as a Conventional Op Amp: A 10dB Gain Wideband Video Amplifier with 50Ω Input/Output Impedance.

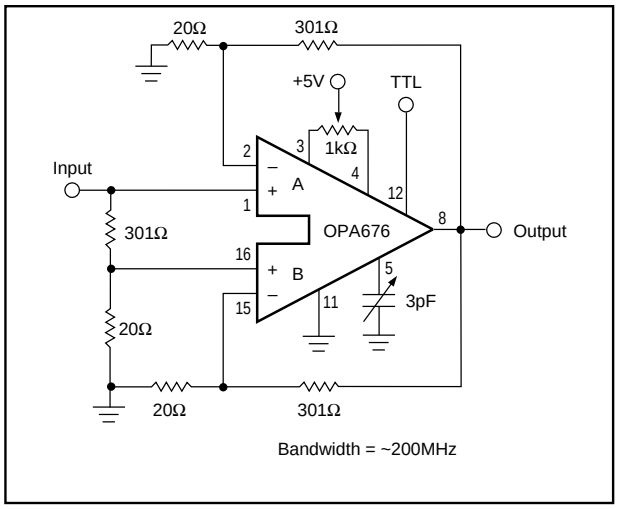


FIGURE 11. Very Fast Programmable Gain Amplifier with Voltage Gains of +1V/V and +16V/V (0dB and 24dB).

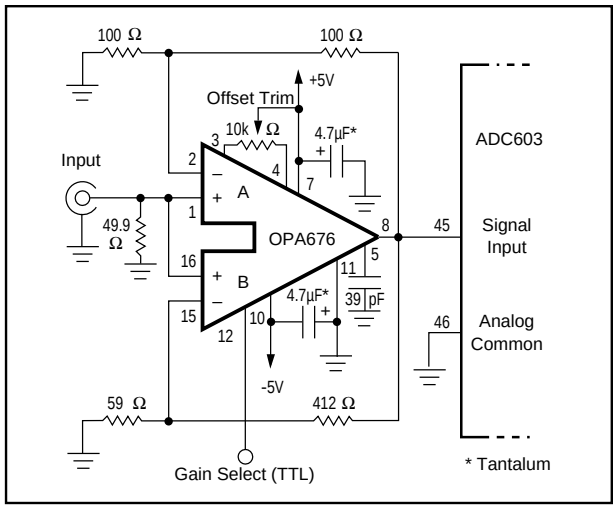


FIGURE 12. Programmable-Gain +2V/V (6dB) or +8V/V (18dB) Buffer Amplifier for Floating-Point Conversion.

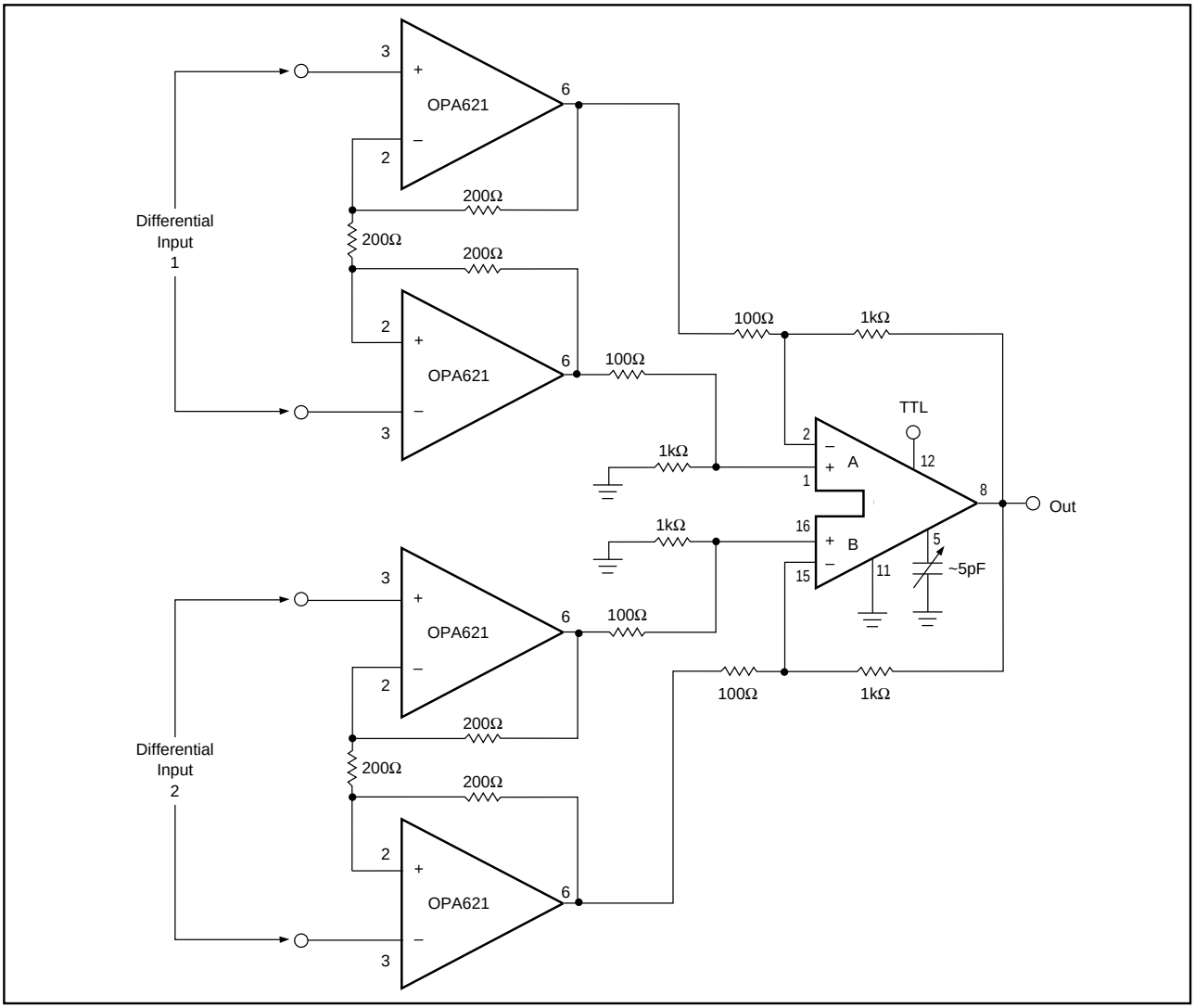


FIGURE 13. High Input Impedance Differential Input Multiplexer with Gain of 30V/V (30dB).

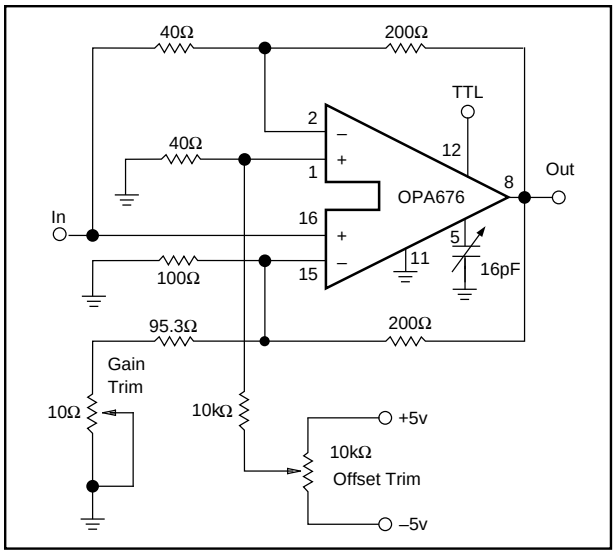


FIGURE 14. Synchronous Modulator/Demodulator with Carrier Balance Trim (Gain = ±5V/V).

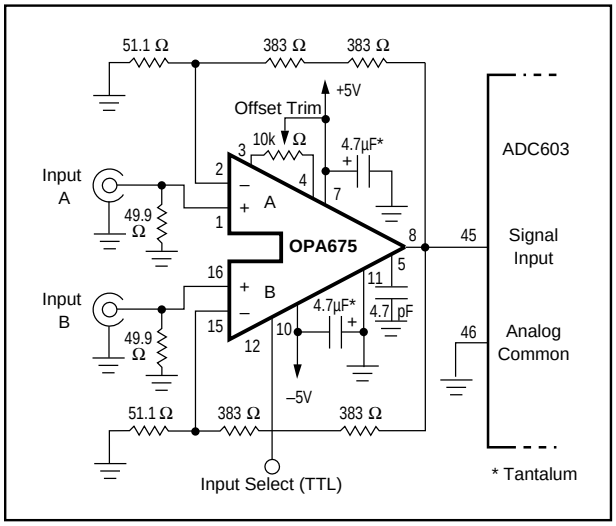


FIGURE 15. Multiplexed Input +16V/V Gain (24dB) Buffer Amplifier.

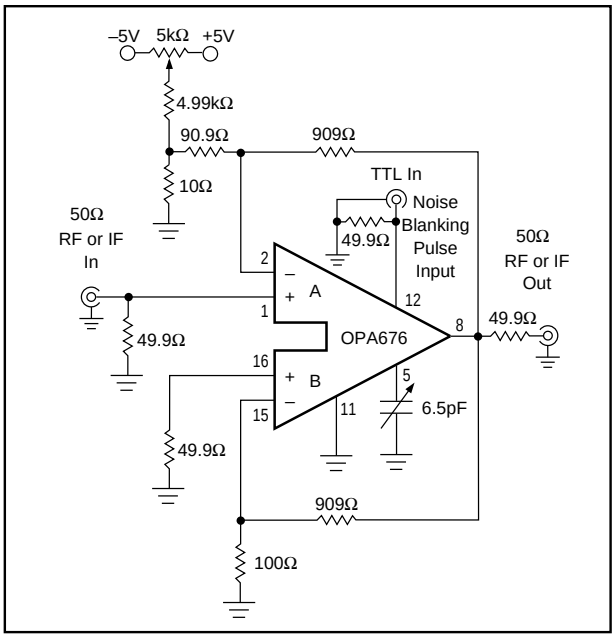


FIGURE 16. Receiver Noise Blanker: A Wideband Gated Video Amplifier.

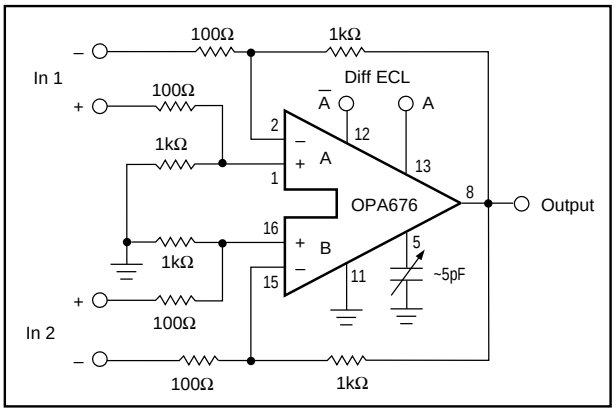
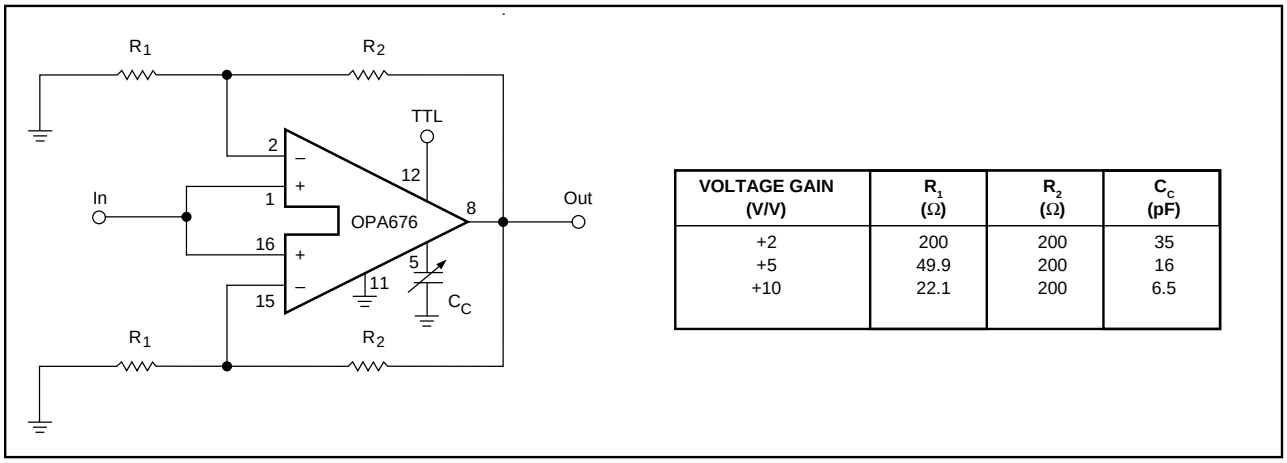


FIGURE 17. Differential Input Multiplexer with Gain of 10V/V (20dB).



VOLTAGE GAIN (V/V)	R_1 (Ω)	R_2 (Ω)	C_C (pF)
+2	200	200	35
+5	49.9	200	16
+10	22.1	200	6.5

FIGURE 18. Programmable-Gain Amplifier.

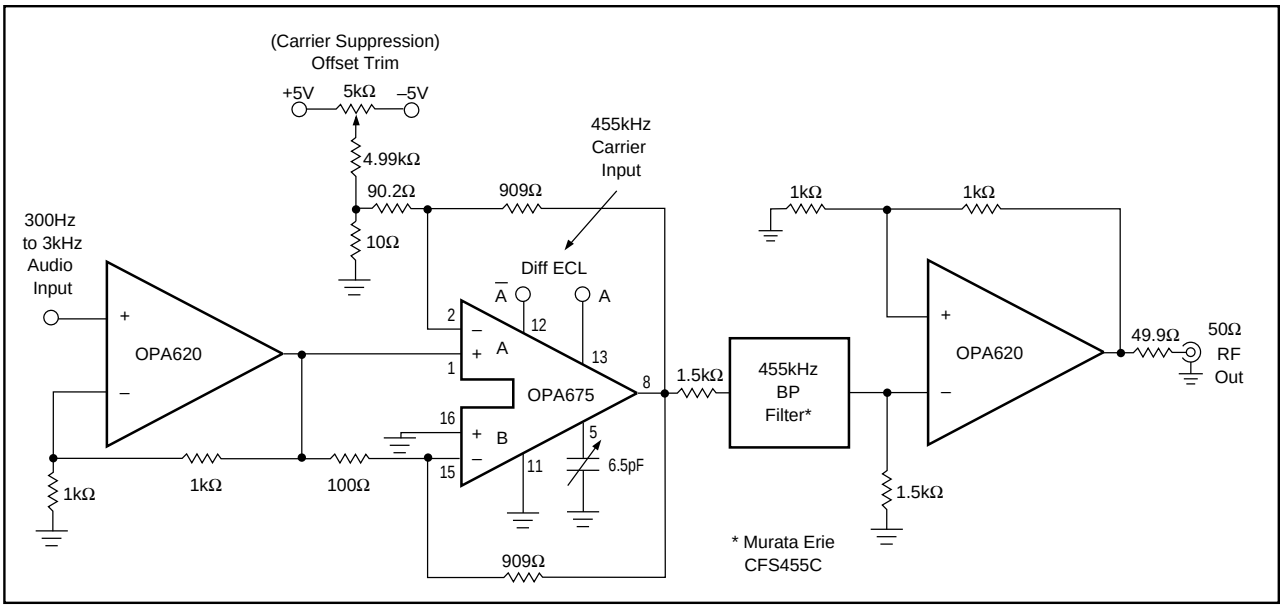
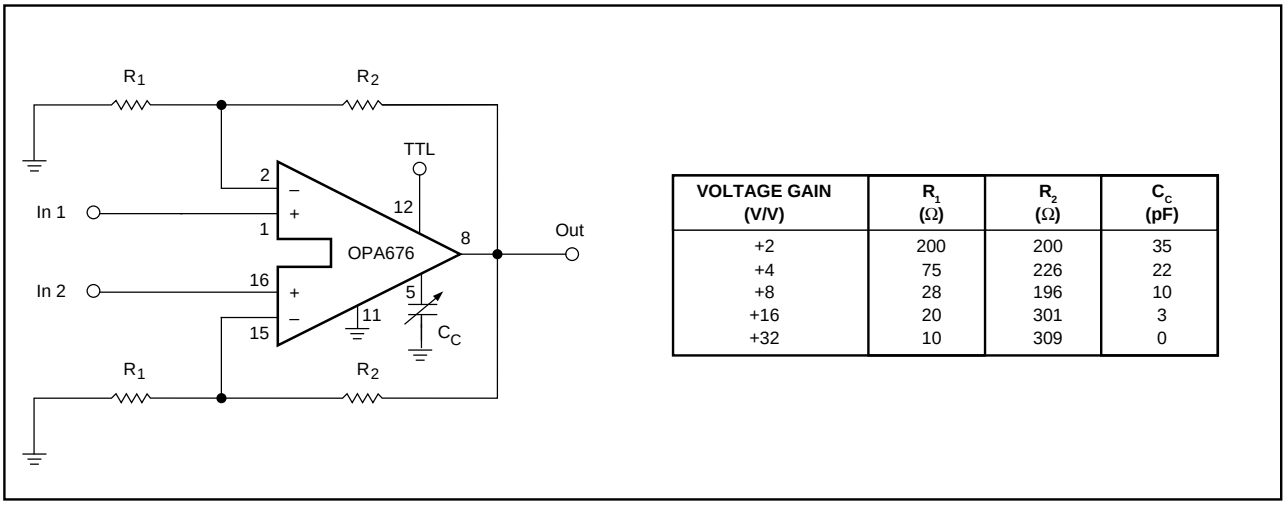
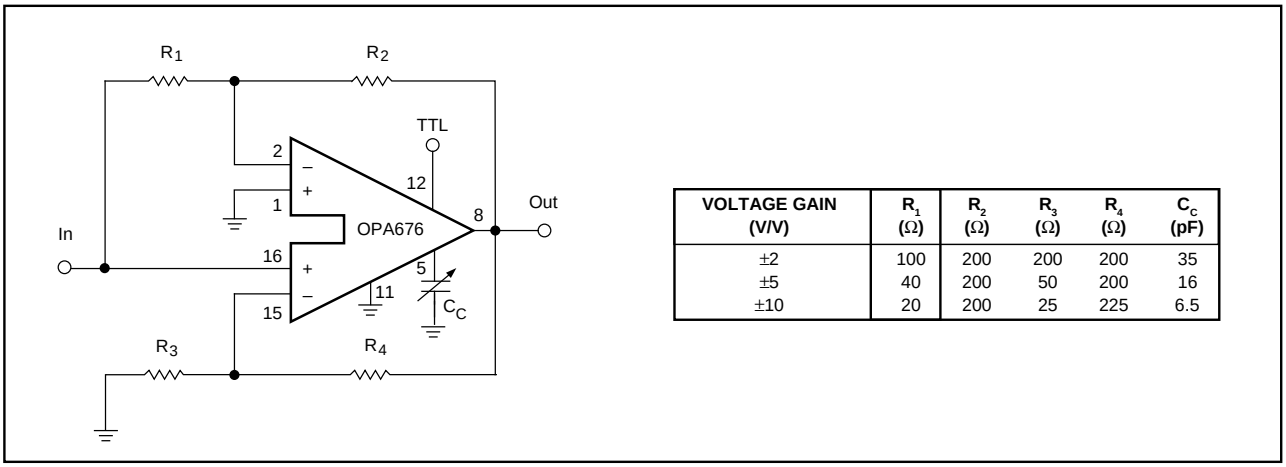


FIGURE 19. Single Sideband Suppressed Carrier Generator.



VOLTAGE GAIN (V/V)	R_1 (Ω)	R_2 (Ω)	C_C (pF)
+2	200	200	35
+4	75	226	22
+8	28	196	10
+16	20	301	3
+32	10	309	0

FIGURE 20. Two-Input Multiplexer (with gain).

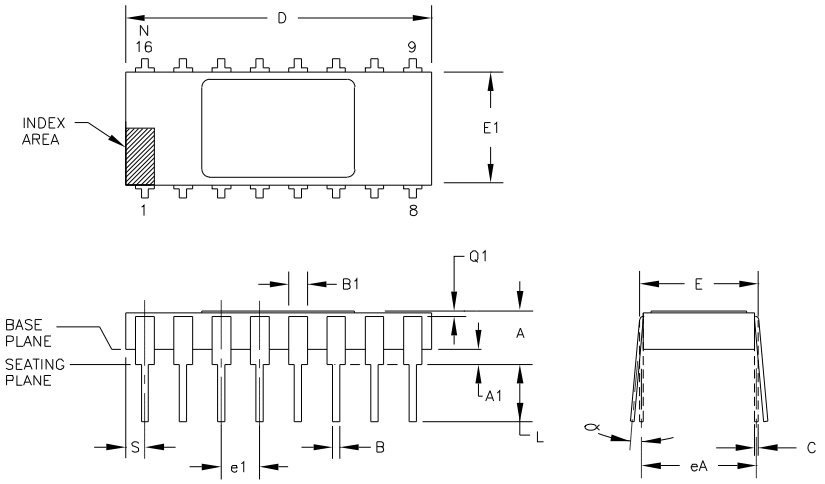


VOLTAGE GAIN (V/V)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	C_C (pF)
±2	100	200	200	200	35
±5	40	200	50	200	16
±10	20	200	25	225	6.5

FIGURE 21. Synchronous Modulator/Demodulator (with gain).

PACKAGE DRAWING

Package Number 109 - 16-Lead, Ceramic Side Braze DIP, .300 Wide



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.105	.175	2.67	4.45	
A1	.025	.055	0.64	1.40	
B	.015	.021	0.38	0.53	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	.770	.830	19.56	21.08	
E	.290	.325	7.37	8.26	
E1	.280	.310	7.11	7.87	6
e1	.100 TYP.		2.54 TYP.		2
eA	.300 TYP.		7.62 TYP.		2
L	.125	.175	3.18	4.45	
N	16		16		4
Q1	.010	--	0.25	--	
S	.020	.065	0.51	1.65	

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
α	0°	15°	0°	15°	3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ109	REV.: D
JEDEC NUMBER: MO-36-AD	