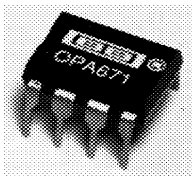
BURR - BROWN®



OPA671

Wide Bandwidth, Fast Settling *Difet®* OPERATIONAL AMPLIFIER

FEATURES

- WIDE GAIN-BANDWIDTH: 35MHz
- HIGH SLEW RATE: 100V/µs
- FAST SETTLING: 240ns to 0.01%
- FET INPUT: I_B = 50pA max
- HIGH OUTPUT CURRENT: 50mA
- WIDE SUPPLY RANGE: V_S = ±4.5 // ±18V

APPLICATIONS

- HIGH-SPEED DATA ACQUISITION
- OPTOELECTRONICS
- TRANSIMPEDANCE AMPLIFIER
- LINE DRIVER

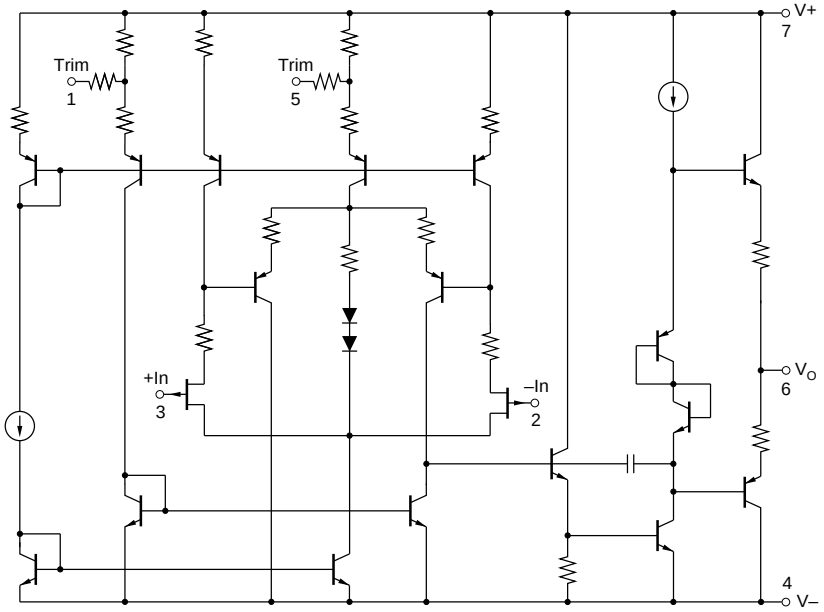
DESCRIPTION

The OPA671 is a FET-input monolithic operational amplifier featuring wide bandwidth and fast settling time. Fabricated using Burr-Brown's ***Difet***, complementary bipolar process, it provides an excellent combination of high speed, accuracy, and high output current.

The OPA671 is versatile, operating from ±4.5V to ±18V power supplies. It can deliver ±10V signals into a 200Ω load at slew rates of 100V/µs. OPA671's ***Difet*** input provides input bias current thousands of times lower than bipolar-input wideband op amps.

The OPA671 is internally compensated and is unity-gain stable, allowing use in the widest range of applications.

The OPA671 is available in an 8-pin plastic DIP, rated for the industrial temperature range.



Difet® Burr-Brown Corporation

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PDS-1120C
Printed in U.S.A.October, 1993

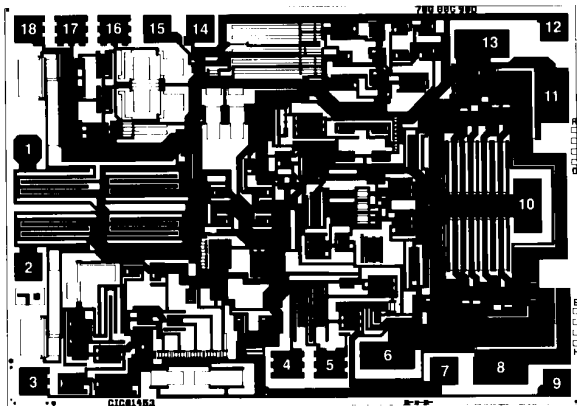
SPECIFICATIONS

At T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA671AP MIN	OPA671AP TYP	OPA671AP MAX	UNITS
OFFSET VOLTAGE					
Input Offset Voltage			±0.5	±5	mV
Average Drift			±10		µV/°C
Power Supply Rejection	V_S = ±4.5 to ±16.5V	72	94		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		5	50	pA
Input Offset Current	V_{CM} = 0V		2		pA
NOISE					
Input Voltage Noise					
Noise Density, f = 100Hz			24		nV/√Hz
f = 1kHz			15		nV/√Hz
f = 10kHz			12		nV/√Hz
f = 100kHz			10		nV/√Hz
Voltage Noise, BW = 10Hz to 1MHz			60		µVp-p
Input Bias Current Noise					
Current Noise Density, f = 10Hz to 1MHz			2		fA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±12	±13		V
Common-Mode Rejection	V_{CM} = ±10V	74	92		dB
INPUT IMPEDANCE					
Differential			10^{12} || 4.5		Ω || pF
Common-Mode			10^{12} || 6		Ω || pF
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 1kΩ		80		dB
	V_O = ±10V, R_L = 200Ω	74	78		dB
FREQUENCY RESPONSE					
Gain-Bandwidth Product			35		MHz
Slew Rate	G = –1, 10V Step		107		V/µs
Settling Time 0.01%	G = –1, 10V Step		240		ns
0.1%	G = –1, 10V Step		150		ns
1%	G = –1, 10V Step		85		ns
Total Harmonic Distortion	G = 1, f = 100kHz V_O = 3V, R_L = 200Ω		0.0006		%
OUTPUT					
Voltage Output	R_L = 200Ω	±10.5	±11.5		V
Current Output	V_O = ±10V		50		mA
Short Circuit Current			–90/+105		mA
Output Resistance, Open-Loop	DC		20		Ω
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5		±18	V
Quiescent Current			±14.8	±17	mA
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–40		+100	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

NOTE: (1) Tested without warmup at T_J = 25°C.

DIE INFORMATION

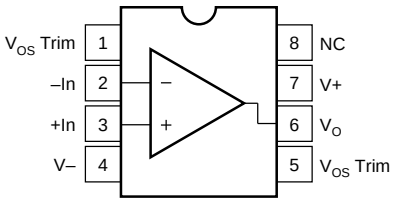


OPA671 DIE TOPOGRAPHY

PAD	FUNCTION
1	–In
2	+In
3	IQ
4	Comp In
5	Comp Out
6	–Short Circuit Bypass
7	–V
8	–V for O/P Stage
9	Balance 2A
10	Output
11	+V for O/P Stage
12	+V
13	+Short Circuit Bypass
14	Balance 2B
15	Balance 1
16	Slope
17	R_{CM}
18	R9

PIN CONFIGURATION

Top View **DIP**



NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	(V+) +1V to (V–) –1V
Operating Temperature	–40°C to +100°C
Storage Temperature	–40°C to +125°C
Output Short-Circuit to Ground	15s
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

An integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ORDERING INFORMATION

MODEL	PACKAGE	TEMP. RANGE
OPA671AP	8-Pin Plastic DIP	–25°C to +85°C

PACKAGE INFORMATION

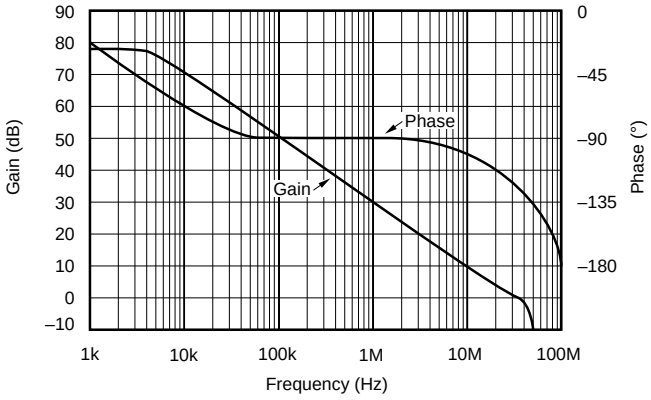
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA671AP	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

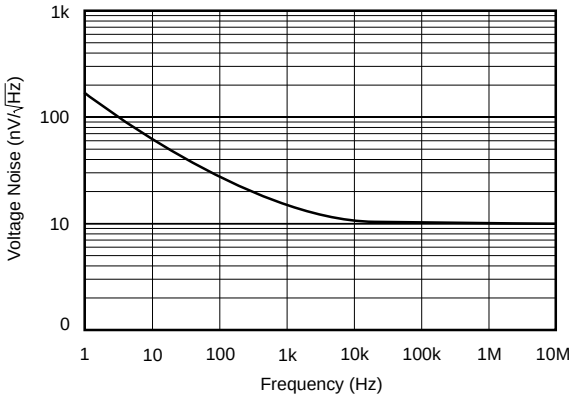
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

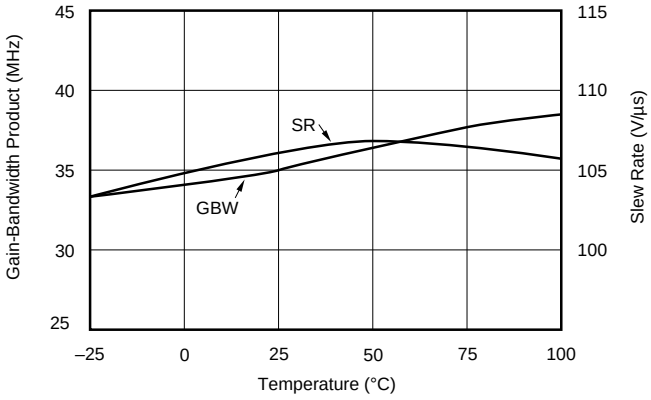
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



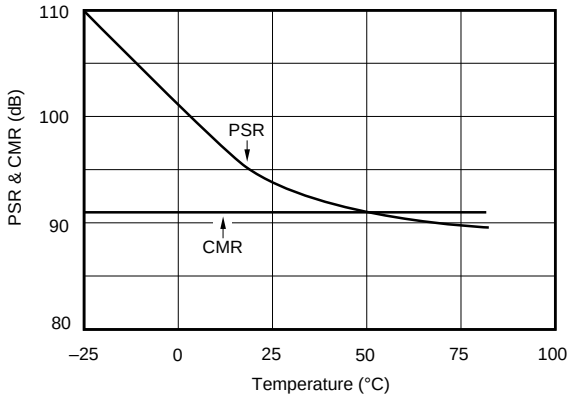
INPUT VOLTAGE NOISE SPECTRAL DENSITY



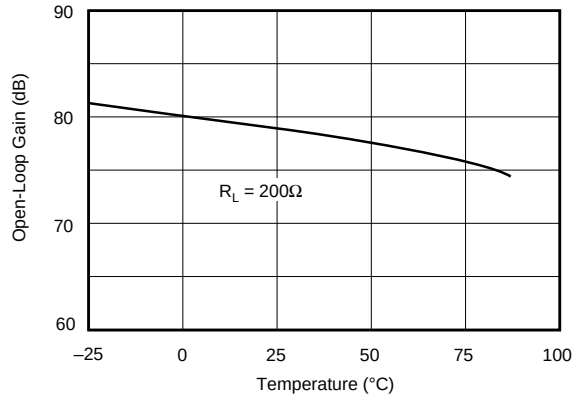
GAIN-BANDWIDTH PRODUCT AND SLEW RATE vs TEMPERATURE



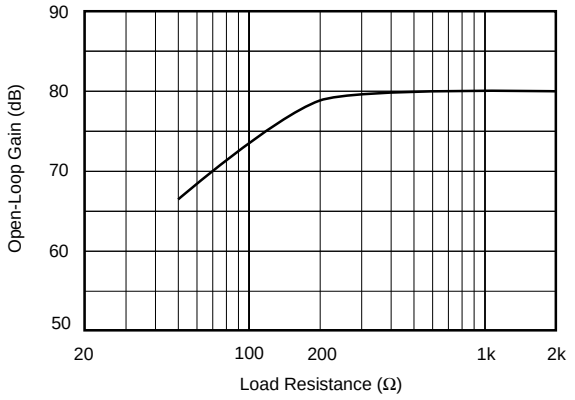
POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



OPEN-LOOP GAIN vs TEMPERATURE



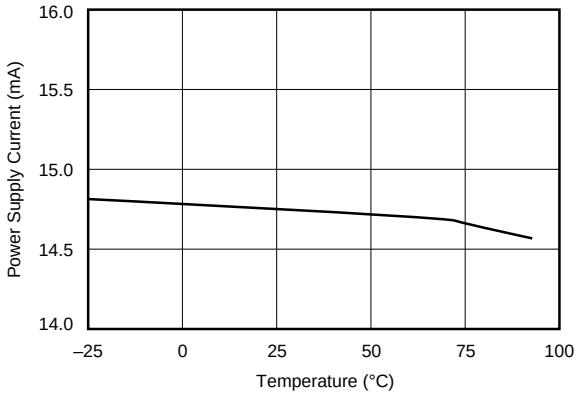
OPEN-LOOP GAIN vs LOAD RESISTANCE



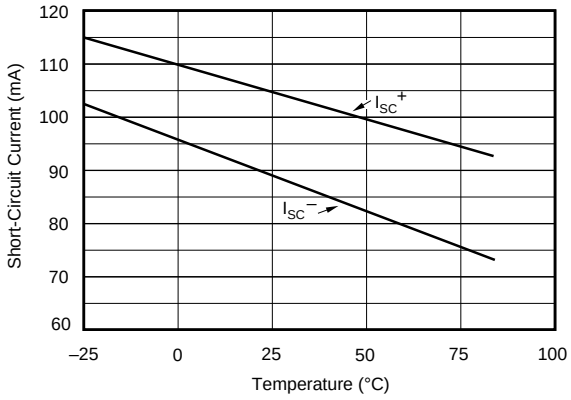
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

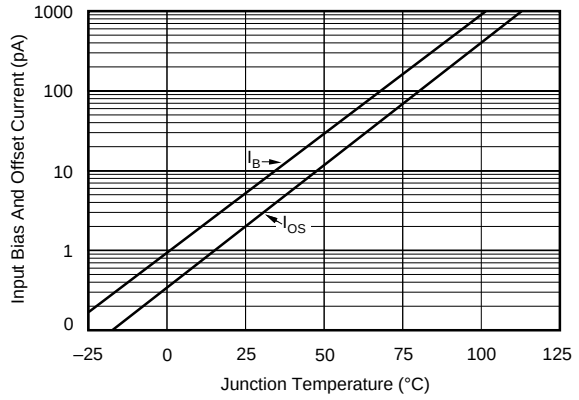
POWER SUPPLY CURRENT vs TEMPERATURE



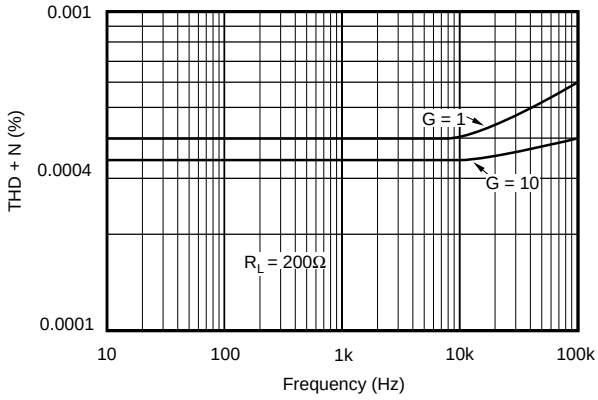
SHORT-CIRCUIT CURRENT vs TEMPERATURE



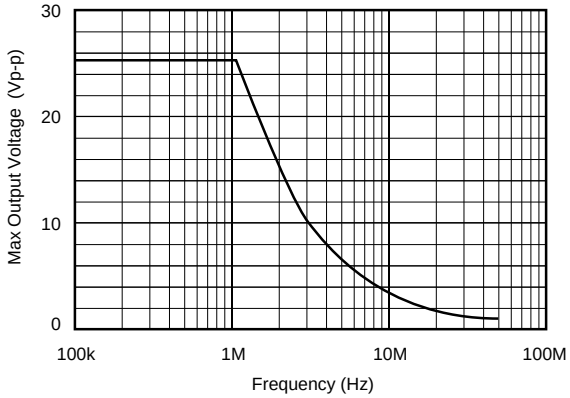
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs JUNCTION TEMPERATURE



TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



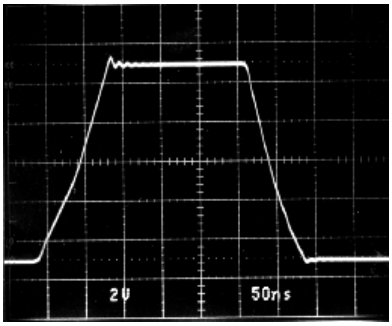
MAX OUTPUT VOLTAGE vs FREQUENCY



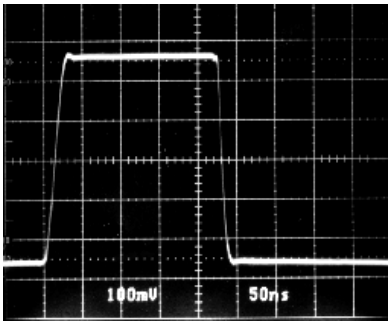
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

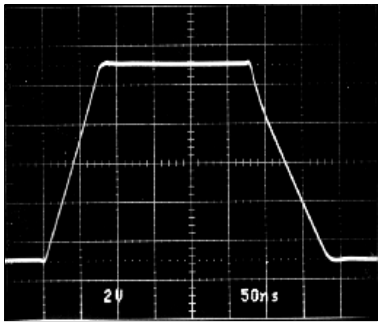
G = +1 LARGE SIGNAL RESPONSE



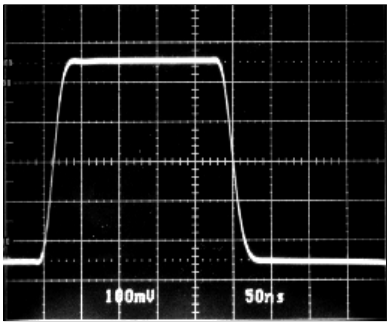
G = +1 SMALL SIGNAL RESPONSE



G = –1 LARGE SIGNAL RESPONSE



G = –1 SMALL SIGNAL RESPONSE



CIRCUIT LAYOUT

With any high-speed, wide-bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct circuit interconnections and avoid stray wiring capacitance—especially at the inverting input pin. A component-side ground plane will help ensure low ground impedance. Do not place the ground plane under or near the inputs and feedback network.

The power supply connections should be bypassed with good high-frequency capacitors positioned close to the op amp pins. In most cases, a 1µF solid tantalum capacitor for each power supply is adequate. The OPA671 can deliver peak load currents up to 100mA. Even if steady-state load currents are lower, signal transients may demand large current transients from the power supplies. It is the power supply bypass capacitors which must supply these current transients. Larger bypass capacitors such as 4.7µF solid tantalum capacitors may improve dynamic performance in some applications.

OFFSET ADJUSTMENT

Many applications require no external offset voltage adjustment. Figure 1 shows an optional circuit for trimming the offset voltage. Do not use this offset voltage adjustment to correct for offsets produced in other circuitry since this can introduce large offset voltage temperature drift.

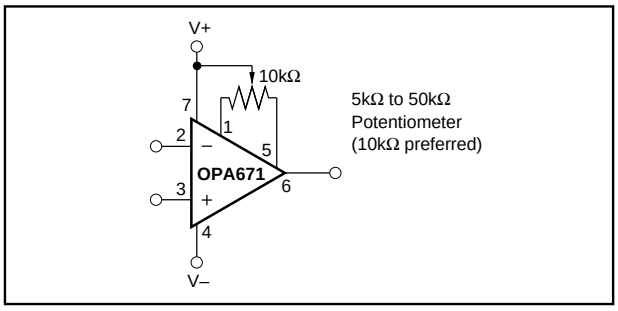


FIGURE 1. Optional Offset Voltage Trim Circuit.

CAPACITIVE LOADS

The OPA671 is internally compensated to be unity-gain stable with minimal capacitive load. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp's open-loop output resistance to form an additional pole in the feedback loop. With wideband op amps, load capacitance as low as 50pF can introduce enough phase shift to degrade dynamic performance. Figure 2 shows circuits which preserve phase margin with capacitive load. Request Application Bulletin AB-028 for details on various compensation circuits and analysis techniques.

POWER DISSIPATION

High output current can cause large internal power dissipation in the OPA671. Copper leadframe construction improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces close to the device pins. Limit the ambient temperature, load and signal to assure that the maximum junction temperature is not exceeded. The OPA671 may be operated at reduced power supply voltage to minimize power dissipation.

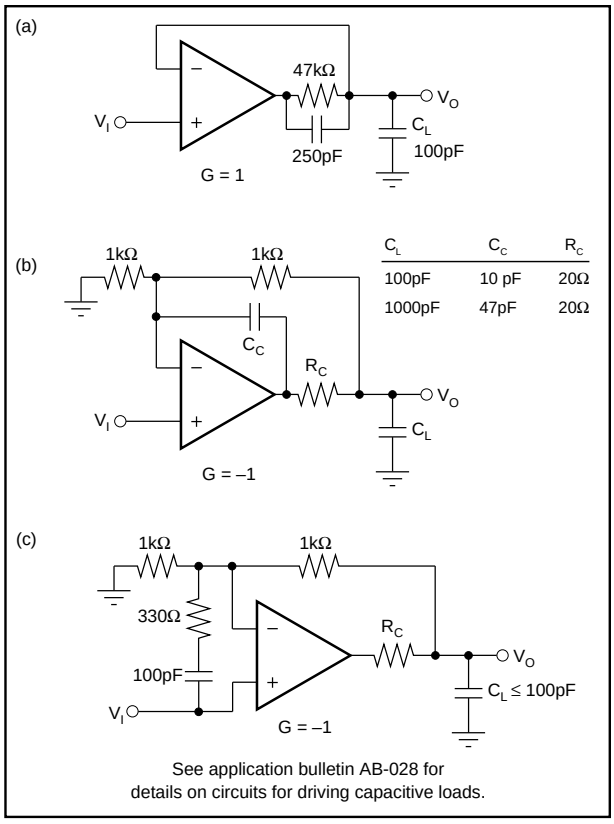


FIGURE 2. Compensation Circuits for Capacitive Loads.

OUTPUT CURRENT LIMIT

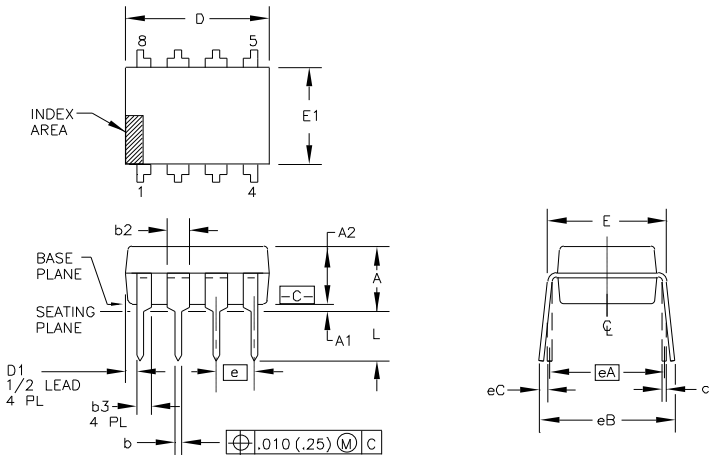
Output current is limited by internal circuitry to approximately 90mA at 25°C. The short-circuit limit current decreases with increasing junction temperature as shown in the typical curves. The current limit will protect the device from inadvertent short-circuits to ground. The power dissipation under this condition, however, is quite high so short-circuits should be avoided.

INPUT BIAS CURRENT

The OPA671 is fabricated with Burr-Brown's dielectrically isolated ***Difet*** process, giving it extremely low input bias current. As with other FET-input amplifiers, input bias current approximately doubles with every 10°C increase in junction temperature. Input bias current can be minimized by soldering the device to the circuit board to provided best heat dissipation. Reduced power supply voltage will also minimize input bias current by reducing internal power dissipation.

PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006	REV.: E
JEDEC NUMBER: MS-001-BA	