



OPA660

Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER AND BUFFER

FEATURES

- WIDE BANDWIDTH: 850MHz
- HIGH SLEW RATE: 3000V/μs
- LOW DIFFERENTIAL GAIN/PHASE ERROR: 0.06%/0.02°
- VERSATILE CIRCUIT FUNCTION
- EXTERNAL I_Q-CONTROL

DESCRIPTION

The OPA660 is a versatile monolithic component designed for wide-bandwidth systems including high performance video, RF and IF circuitry. It includes a wideband, bipolar integrated voltage-controlled current source and voltage buffer amplifier.

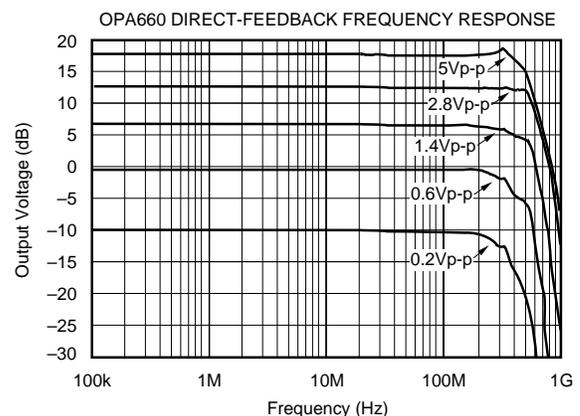
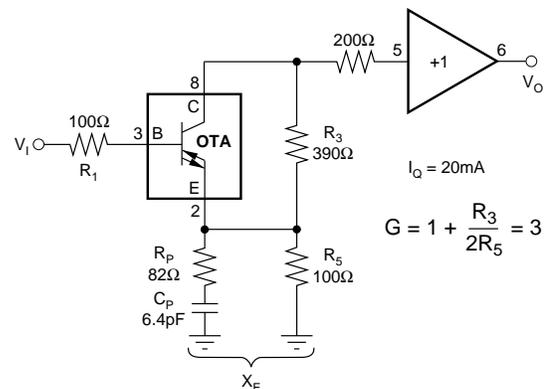
The voltage-controlled current source or Operational Transconductance Amplifier (OTA) can be viewed as an "ideal transistor." Like a transistor, it has three terminals—a high-impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OTA, however, is self-biased and bipolar. The output current is zero-for-zero differential input voltage. AC inputs centered about zero produce an output current which is bipolar and centered about zero. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current and gain trade-offs to be optimized.

The open-loop buffer amplifier provides 850MHz bandwidth and 3000V/μs slew rate. Used as a basic building block, the OPA660 simplifies the design of AGC amplifiers, LED driver circuits for Fiber Optic Transmission, integrators for fast pulses, fast control loop amplifiers, and control amplifiers for capacitive sensors and active filters.

The OPA660 is packaged in SO-8 surface-mount, and 8-pin plastic DIP, specified from -40°C to +85°C.

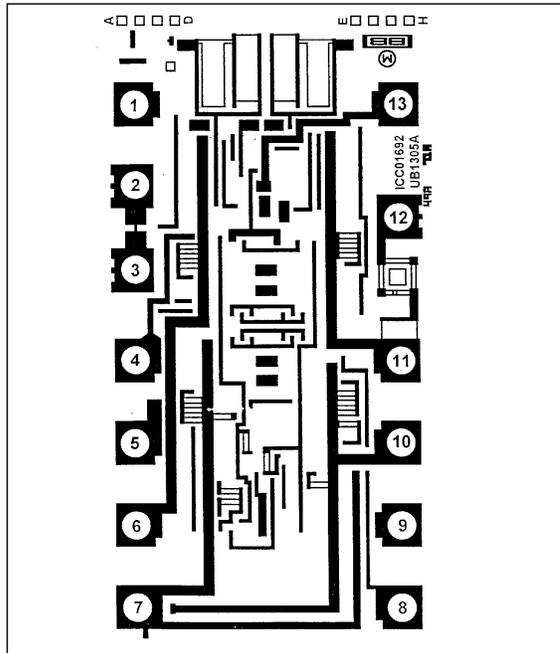
APPLICATIONS

- VIDEO/BROADCAST EQUIPMENT
- COMMUNICATIONS EQUIPMENT
- HIGH-SPEED DATA ACQUISITION
- WIDEBAND LED DRIVER
- DIRECT-FEEDBACK AMPLIFIER
- AGC-MULTIPLIER
- NS-PULSE INTEGRATOR
- CONTROL LOOP AMPLIFIER
- 400MHz DIFFERENTIAL INPUT AMPLIFIER



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DICE INFORMATION



OPA660 DIE TOPOGRAPHY

PAD	FUNCTION
1	Enable
2	NC
3	NC
4	OTA Input, Low Impedance
5	OTA Input, High Impedance
6	-5V Supply, Output
7	-5V Supply
8	Buffer Input
9	Buffer Output
10	+5V Supply
11	+5V Supply, Output
12	NC
13	OTA Output
14	NC

Substrate Bias: Negative Supply

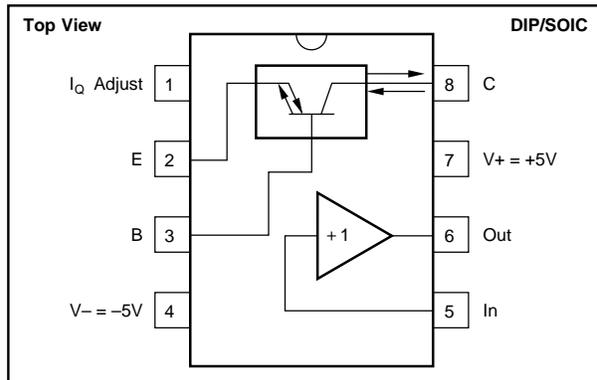
NC: No Connection

Wire Bonding: Gold wire bonding is recommended.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	41 x 77, ±5	1.05 x 1.95, ±0.13
Die Thickness	14 ±1	0.55, ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, -0.0	0.0005, +0.0013, -0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage ⁽¹⁾	±V _S ±0.7V
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to ±V_S.

PACKAGING INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA660AP	8-Pin Plastic DIP	006
OPA660AU	SO-8 Surface-Mount	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

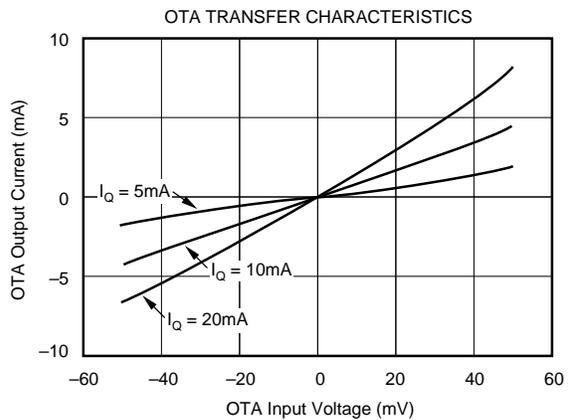
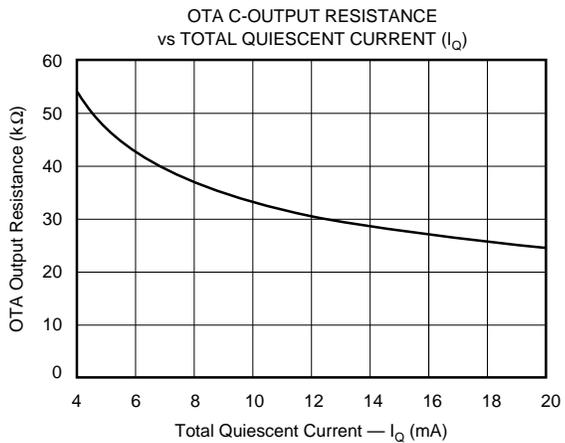
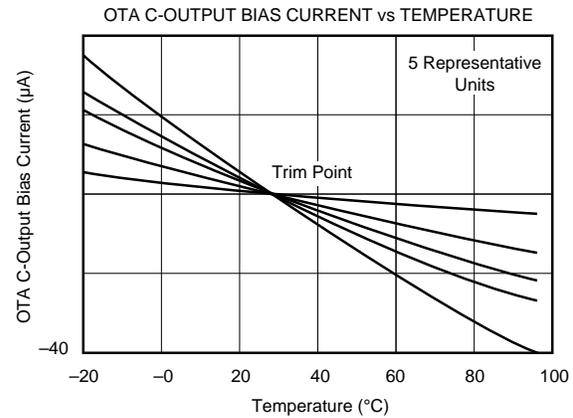
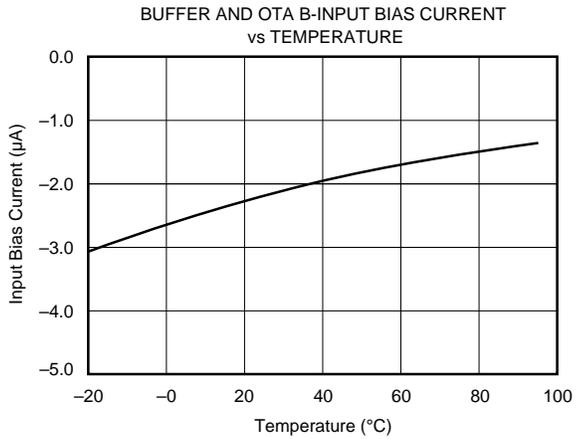
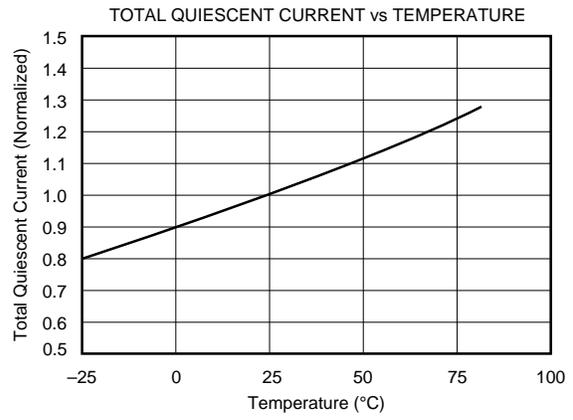
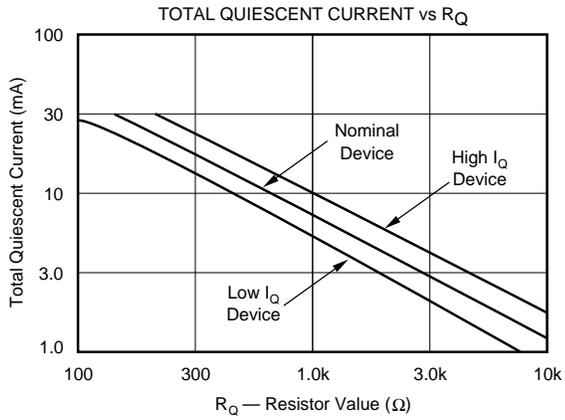
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ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA660AP	Plastic 8-Pin DIP	-25°C to +85°C
OPA660AU	SO-8 Surface-Mount	-25°C to +85°C

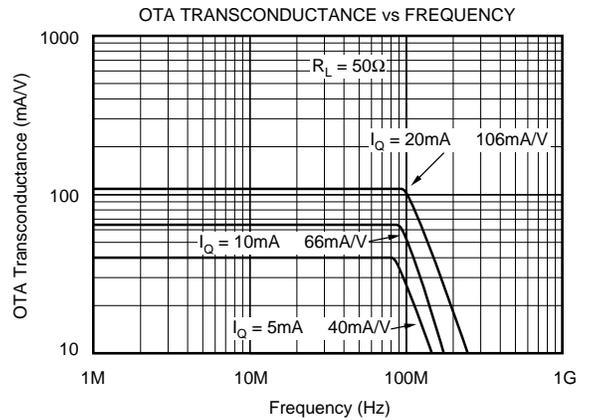
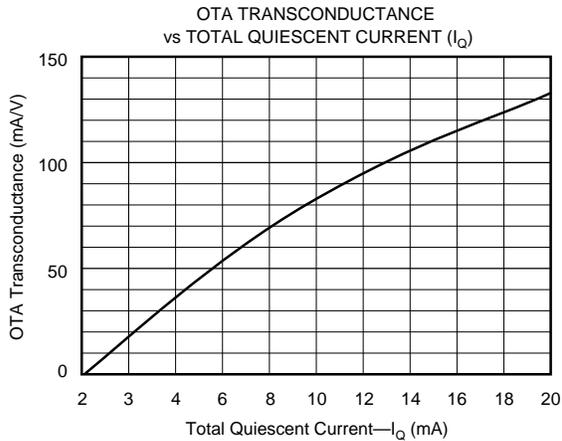
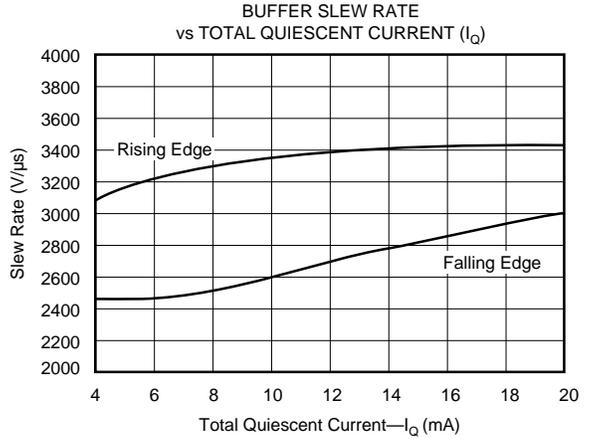
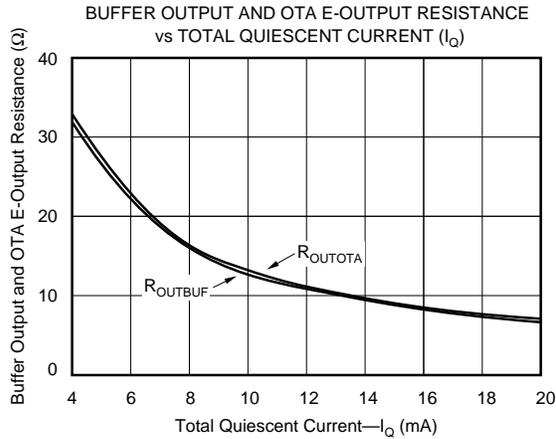
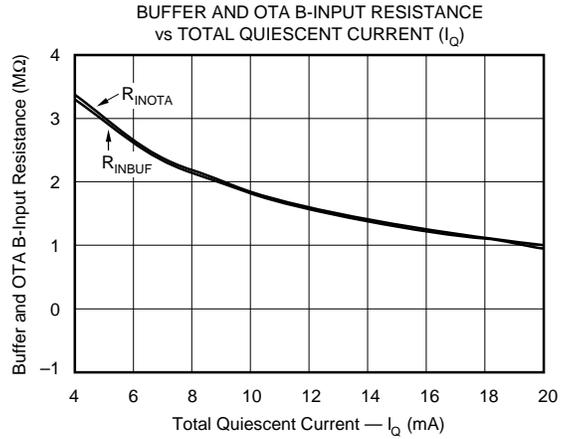
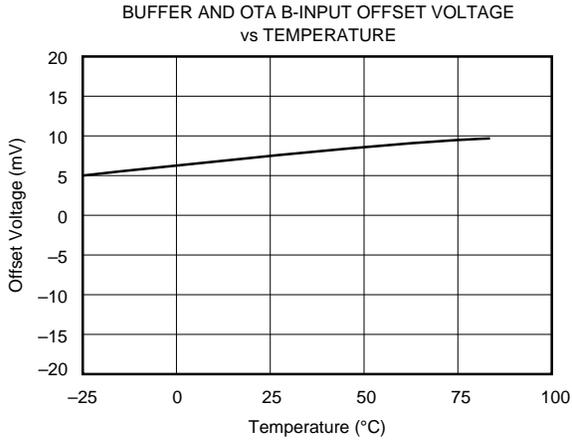
TYPICAL PERFORMANCE CURVES

$I_Q = 20\text{mA}$, $T_A = +25^\circ\text{C}$, and $V_S = \pm 5\text{V}$ unless otherwise noted.



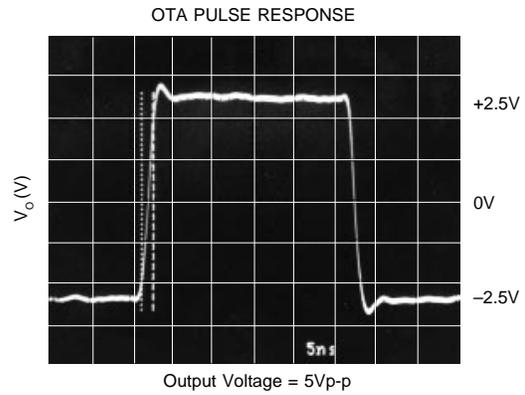
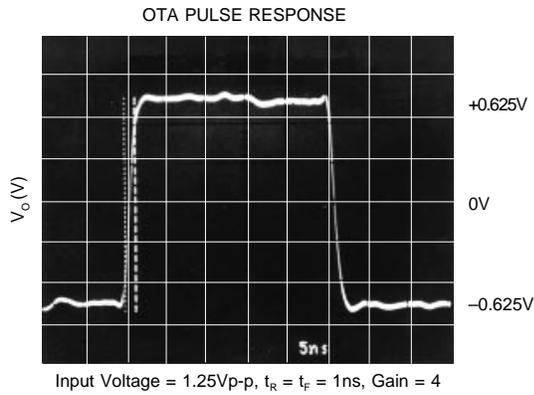
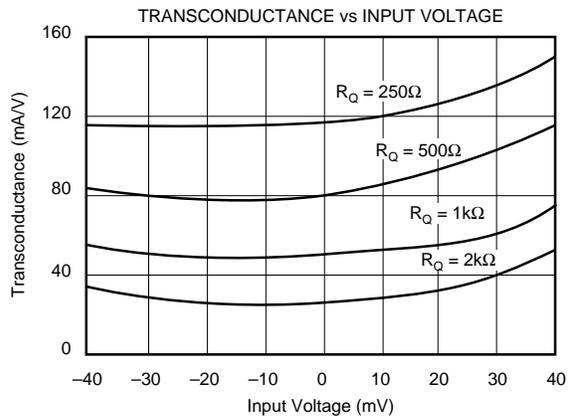
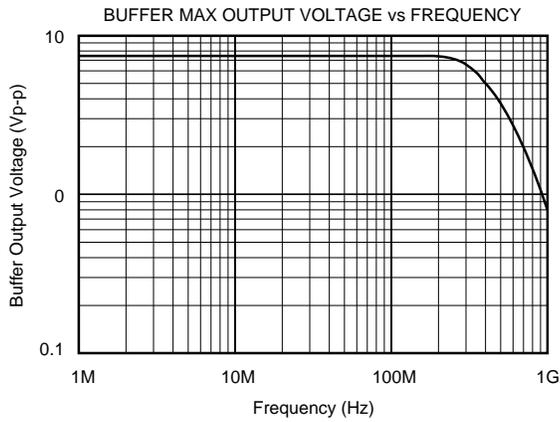
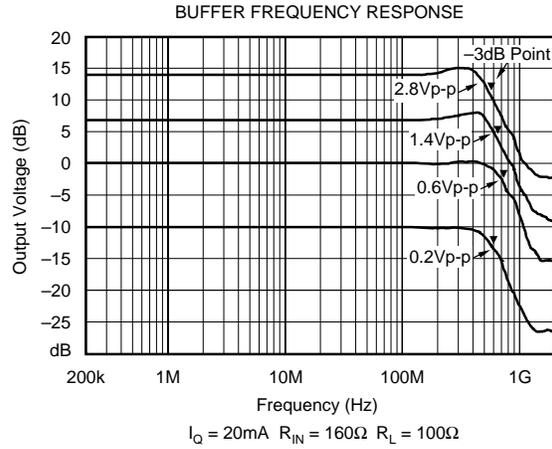
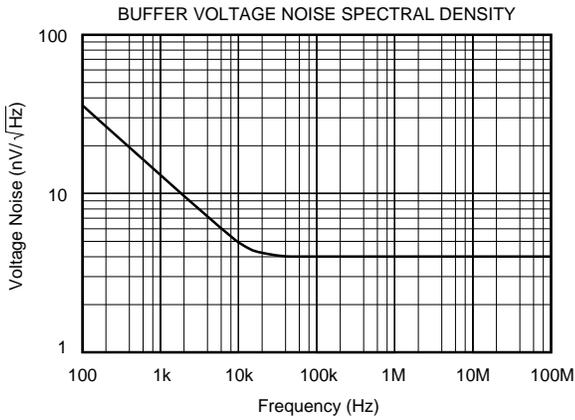
TYPICAL PERFORMANCE CURVES (CONT)

$I_Q = 20\text{mA}$, $T_A = +25^\circ\text{C}$, and $V_S = \pm 5\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

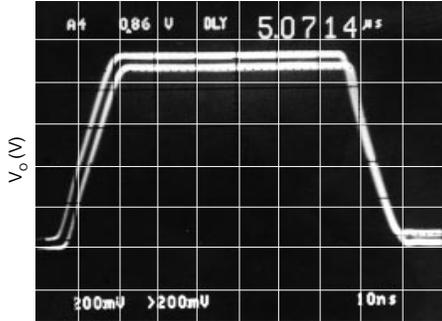
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TYPICAL PERFORMANCE CURVES (CONT)

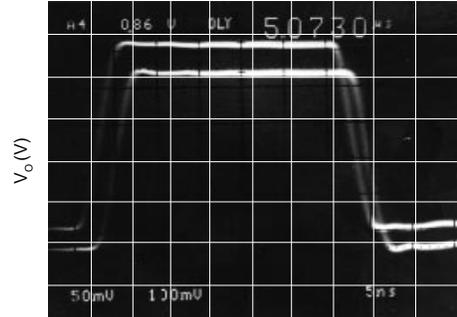
$I_Q = 20\text{mA}$, $T_A = +25^\circ\text{C}$, and $V_S = \pm 5\text{V}$ unless otherwise noted.

BUFFER LARGE SIGNAL PULSE RESPONSE

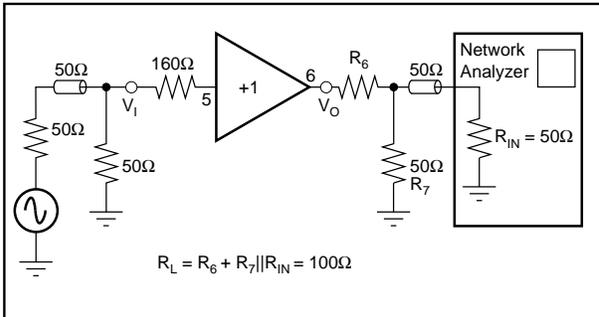


(HDTV Signal Pulse) $t_R = t_F = 10\text{ns}$, $V_O = 5\text{Vp-p}$

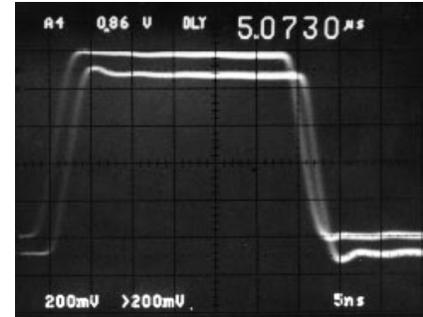
BUFFER LARGE SIGNAL PULSE RESPONSE



$t_R = t_F = 3\text{ns}$, $V_O = 5\text{Vp-p}$

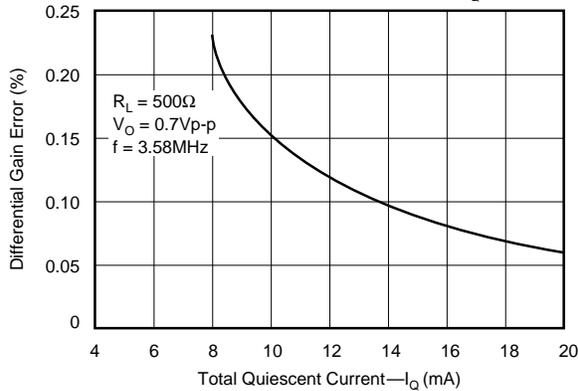


Test Circuit Buffer Pulse and Frequency Response

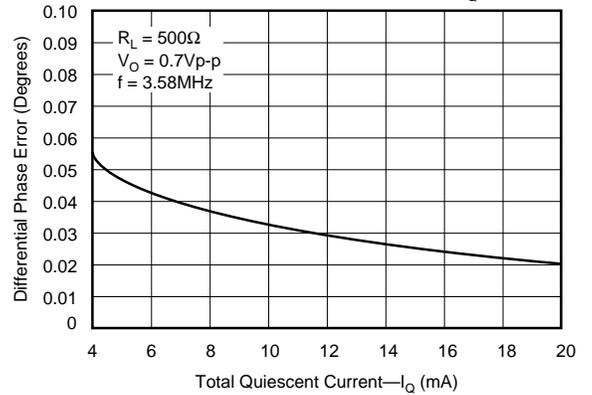


$t_R = t_F = 3\text{ns}$, $V_O = 0.2\text{Vp-p}$

BUFFER DIFFERENTIAL GAIN ERROR vs TOTAL QUIESCENT CURRENT (I_Q)

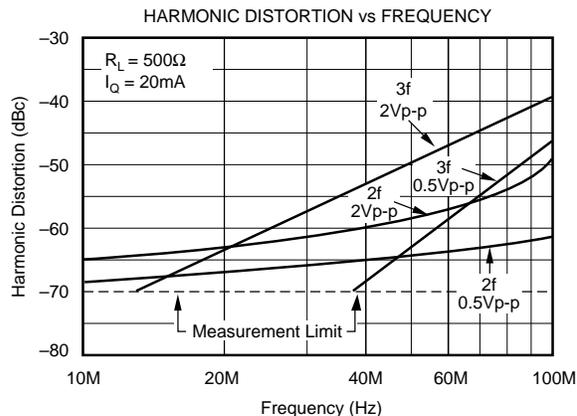
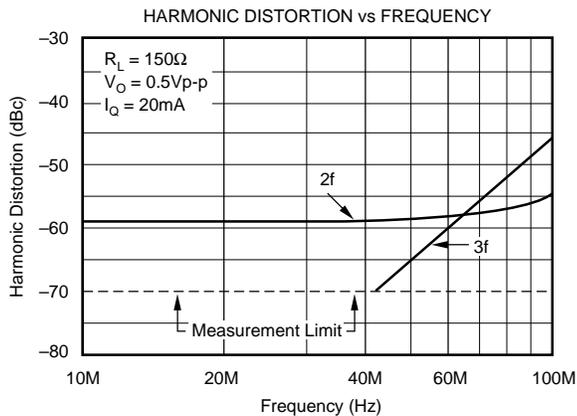


BUFFER DIFFERENTIAL PHASE ERROR vs TOTAL QUIESCENT CURRENT (I_Q)



TYPICAL PERFORMANCE CURVES (CONT)

$I_Q = 20\text{mA}$, $T_A = +25^\circ\text{C}$, and $V_S = \pm 5\text{V}$ unless otherwise noted.



APPLICATIONS INFORMATION

The OPA660 operates from $\pm 5\text{V}$ power supplies ($\pm 6\text{V}$ maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur.

Inputs of the OPA660 are protected with internal diode clamps as shown in the simplified schematic, Figure 1. These protection diodes can safely conduct 10mA , continuously (30mA peak). If input voltages can exceed the power supply voltages by 0.7V , the input signal current must be limited.

The buffer output is not current-limited or protected. If the output is shorted to ground, currents up to 60mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage. The same cautions apply to the OTA section when connected as a buffer (see Basic Applications Circuits, Figure 6b).

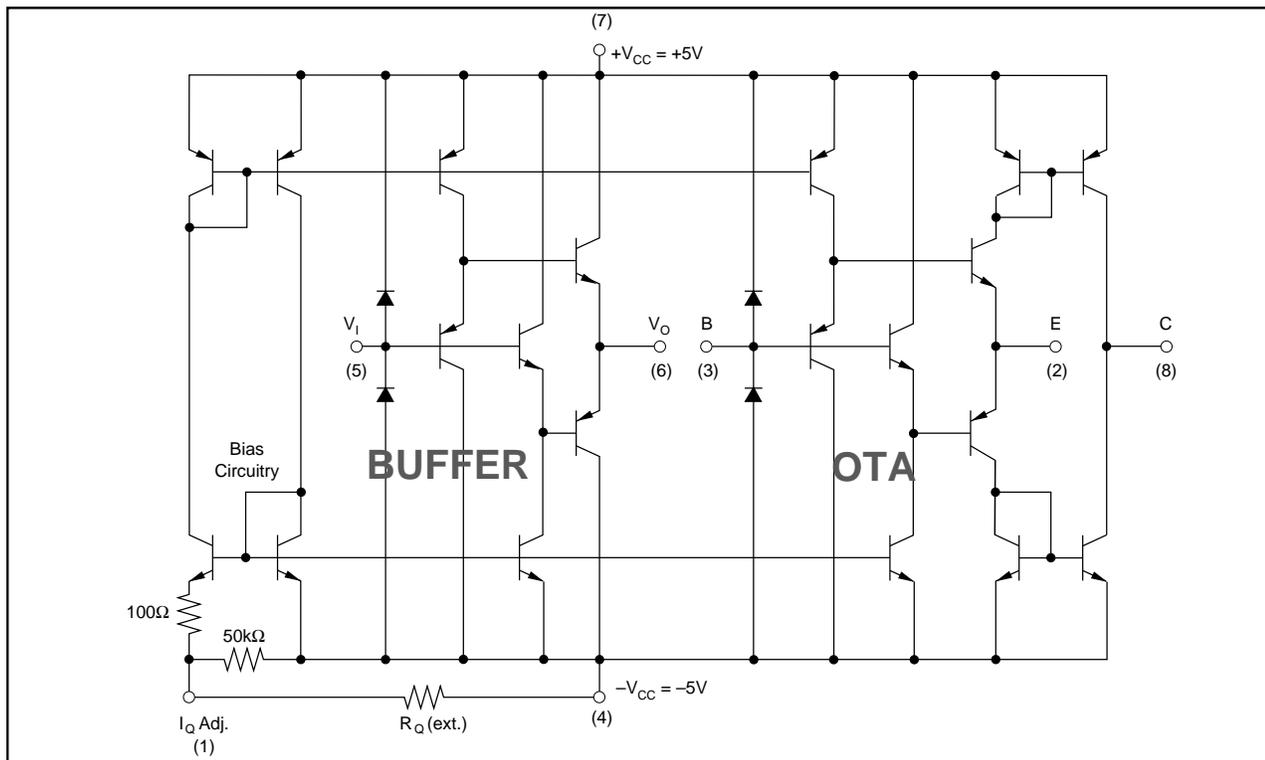


FIGURE 1. Simplified Circuit Diagram.

BUFFER SECTION—AN OVERVIEW

The buffer section of the OPA660 is an open-loop buffer consisting of complementary emitter-followers. It uses no feedback, so its low frequency gain is slightly less than unity and somewhat dependent on loading. It is designed primarily for interstage buffering. It is not designed for driving long cables or low impedance loads (although with small signals, it may be satisfactory for these applications).

TRANSCONDUCTANCE (OTA) SECTION—AN OVERVIEW

The symbol for the OTA section is similar to a transistor. Applications circuits for the OTA look and operate much like transistor circuits—the transistor, too, is a voltage-controlled current source. Not only does this simplify the understanding of applications circuits, but it aids the circuit optimization process. Many of the same intuitive techniques used with transistor designs apply to OTA circuits as well.

The three terminals of the OTA are labeled B, E, and C. This calls attention to its similarity to a transistor, yet draws distinction for clarity.

While it is similar to a transistor, one essential difference is the sense of the C output current. It flows out the C terminal for positive B-to-E input voltage and in the C terminal for negative B-to-E input voltage. The OTA offers many advantages over a discrete transistor. The OTA is self-biased, simplifying the design process and reducing component count. The OTA is far more linear than a transistor. Transconductance of the OTA is constant over a wide range of collector currents—this implies a fundamental improvement of linearity.

BASIC CONNECTIONS

Figure 2 shows basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best. See “Circuit Layout” at the end of the applications discussion and Figure 26 for further suggestions on layout.

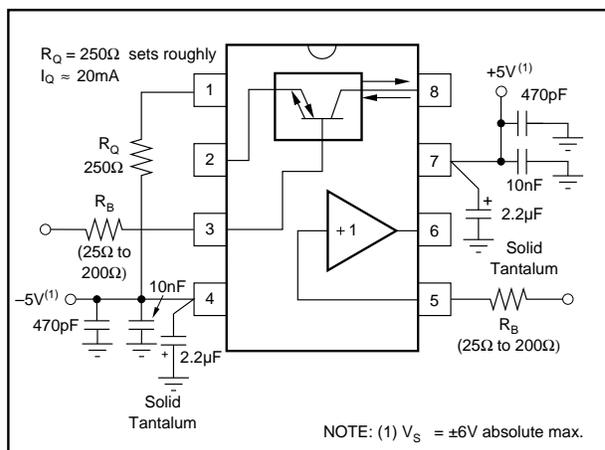


FIGURE 2. Basic Connections.

QUIESCENT CURRENT CONTROL PIN

The quiescent current of the OPA660 is set with a resistor, R_Q , connected from pin 1 to V_- . It affects the operating currents of both the buffer and OTA sections. This controls the bandwidth and AC behavior as well as the transconductance of the OTA section.

$R_Q = 250\Omega$ sets approximately 20mA total quiescent current at 25°C. With a fixed 250Ω resistor, process variations could cause this current to vary from approximately 16mA to 26mA. It may be appropriate in some applications to trim this resistor to achieve the desired quiescent current or AC performance.

Applications circuits generally do not show resistor, R_Q , but it is required for proper operation.

With a fixed R_Q resistor, quiescent current increases with temperature (see typical performance curve, Quiescent Current vs Temperature). This variation of current with temperature holds the transconductance, g_m , of the OTA relatively constant with temperature (another advantage over a transistor).

It is also possible to vary the quiescent current with a control signal. The control loop in Figure 3 shows a 1/2 of a REF200 current source used to develop 100mV on R_1 . The loop forces 100mV to appear on R_2 . Total quiescent current of the OPA660 is approximately $85 \cdot I_1$, where I_1 is the current made to flow out of pin 1.

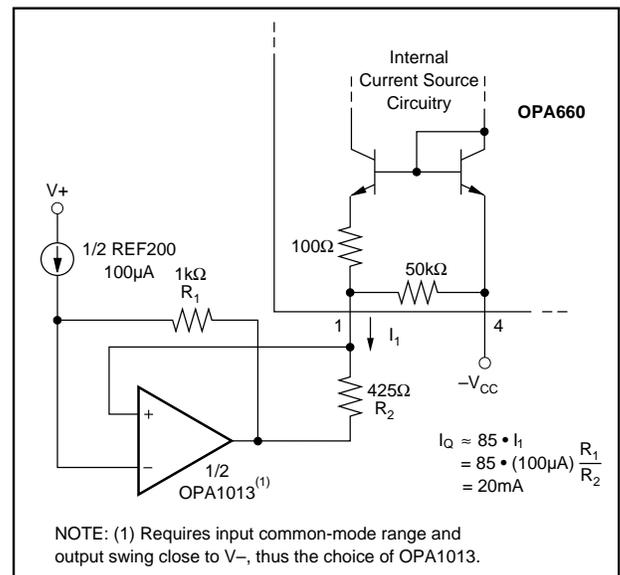


FIGURE 3. Optional Control Loop for Setting Quiescent Current.

With this control loop, quiescent current will be nearly constant with temperature. Since this differs from the temperature-dependent behavior of the internal current source, other temperature-dependent behavior may differ from that shown in typical performance curves.

The circuit of Figure 3 will control the I_Q of the OPA660 somewhat more accurately than with a fixed external resistor, R_Q . Otherwise, there is no fundamental advantage to

A positive voltage at the B, pin 3, causes a positive current to flow out of the C, pin 8. Figure 5b shows an amplifier connection of the OTA, the equivalent of a common-emitter transistor amplifier. Input and output can be ground-referenced without any biasing. Due to the sense of the output current, the amplifier is non-inverting. Figure 8 shows the amplifier with various gains and output voltages using this configuration.

Just as transistor circuits often use emitter degeneration, OTA circuits may also use degeneration. This can be used to reduce the effect that offset voltage and offset current might otherwise have on the DC operating point of the OTA. The E-degeneration resistor may be bypassed with a large capacitor to maintain high AC gain. Other circumstances may suggest a smaller value capacitor used to extend or optimize high-frequency performance.

The transconductance of the OTA with degeneration can be calculated by—

$$g_m' = \frac{1}{\frac{1}{g_m} + R_E}$$

Figure 6b shows the OTA connected as an E-follower—a voltage buffer. The buffer formed by this connection performs virtually the same as the buffer section of the OPA660 (the actual signal path is identical).

It is recommended to use a low value resistor in series with the B OTA and buffer inputs. This reduces any tendency to oscillate and controls frequency response peaking. Values from 25Ω to 200Ω are typical.

Figure 7 shows the Common-B amplifier. This configuration produces an inverting gain, and a low impedance input. This low impedance can be converted to a high impedance by inserting the buffer amplifier in series.

CIRCUIT LAYOUT

The high frequency performance of the OPA660 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not dogma.

- Bypass power supplies very close to the device pins. Use a combination between tantalum capacitors (approximately 2.2μF) and polyester capacitors. Surface-mount types are best because they provide lowest inductance.
- Make short, wide interconnection traces to minimize series inductance.
- Use a large ground plane to assure that a low impedance ground is available throughout the layout.
- Do not extend the ground plane under high impedance nodes sensitive to stray capacitance.
- Sockets are not recommended because they add significant inductance.

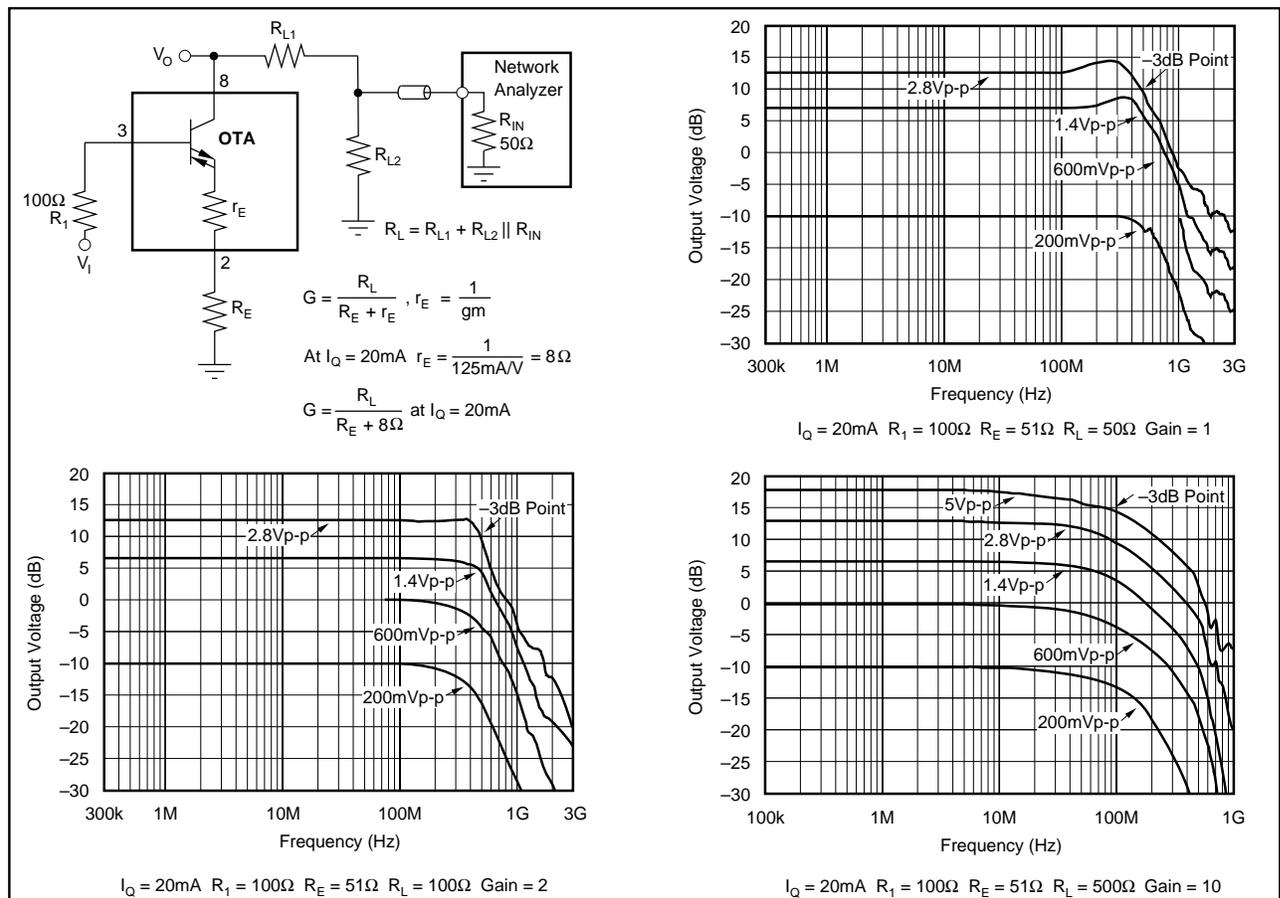


FIGURE 8. Common-E Amplifier Performance.

- Use low-inductance components. Some film resistors are trimmed with spiral cuts which increase inductance.
- Use surface-mount components—they generally provide the lowest inductance.

- A resistor (25Ω to 200Ω) in series with the buffer and/or B input may help reduce oscillations and peaking.
- Use series resistors in the supply lines to decouple multiple devices.

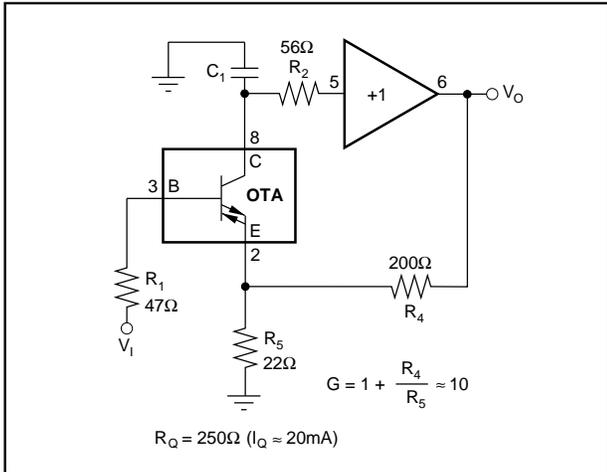


FIGURE 9. Current-Feedback Amplifier.

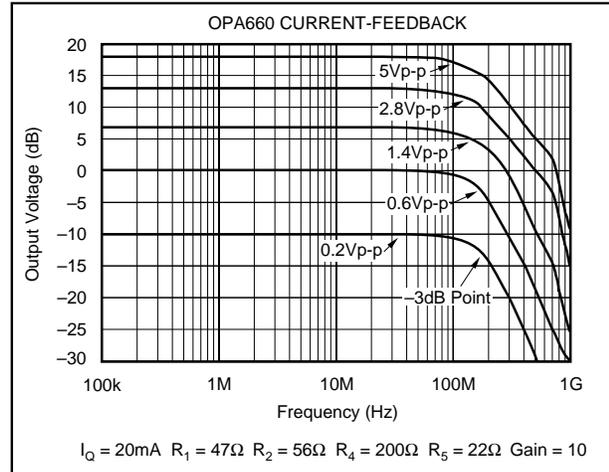


FIGURE 10. Current-Feedback Amplifier Frequency Response, $G = 10$.

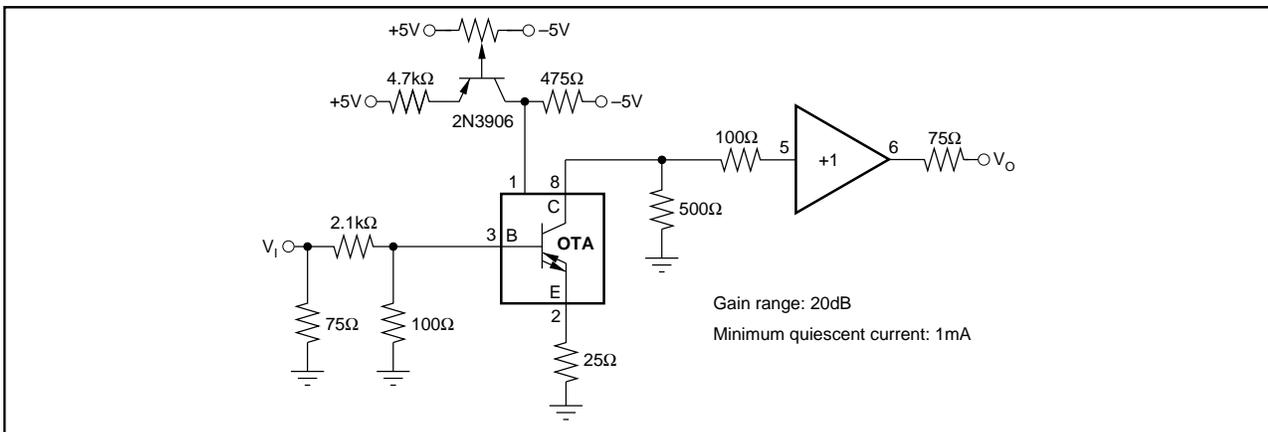


FIGURE 11. Variable Gain Amplifier (Luminance).

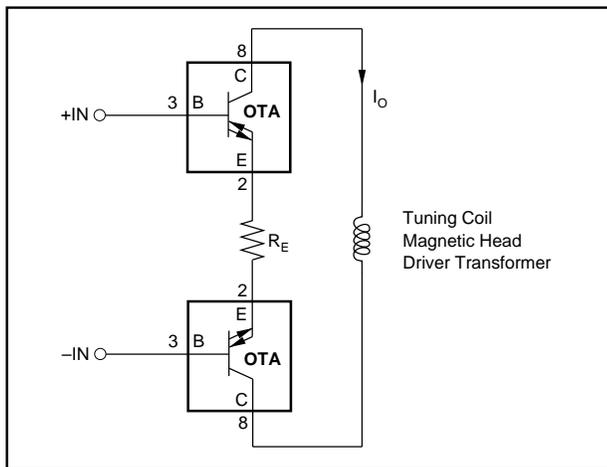


FIGURE 12. High Speed Current Driver (bridge combination for increased output voltage capability).

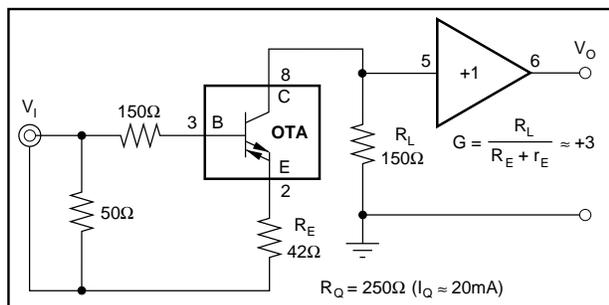


FIGURE 13. Cable Amplifier.

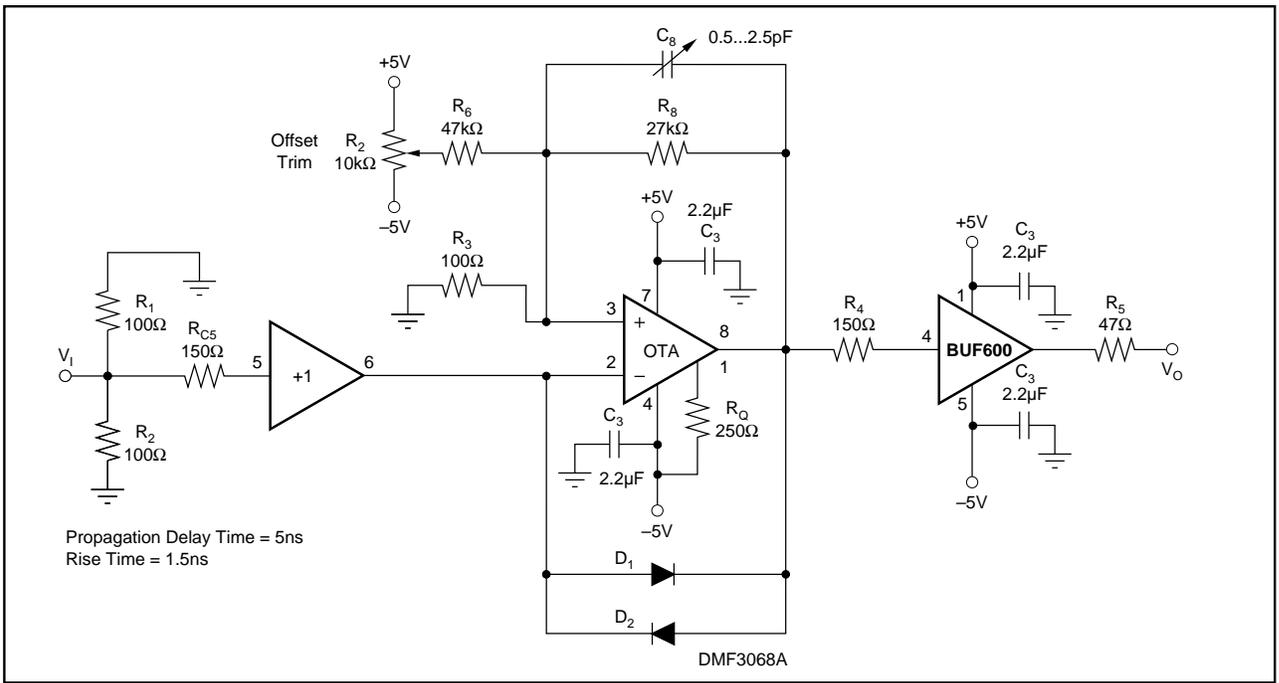


FIGURE 14. Comparator (Low Jitter).

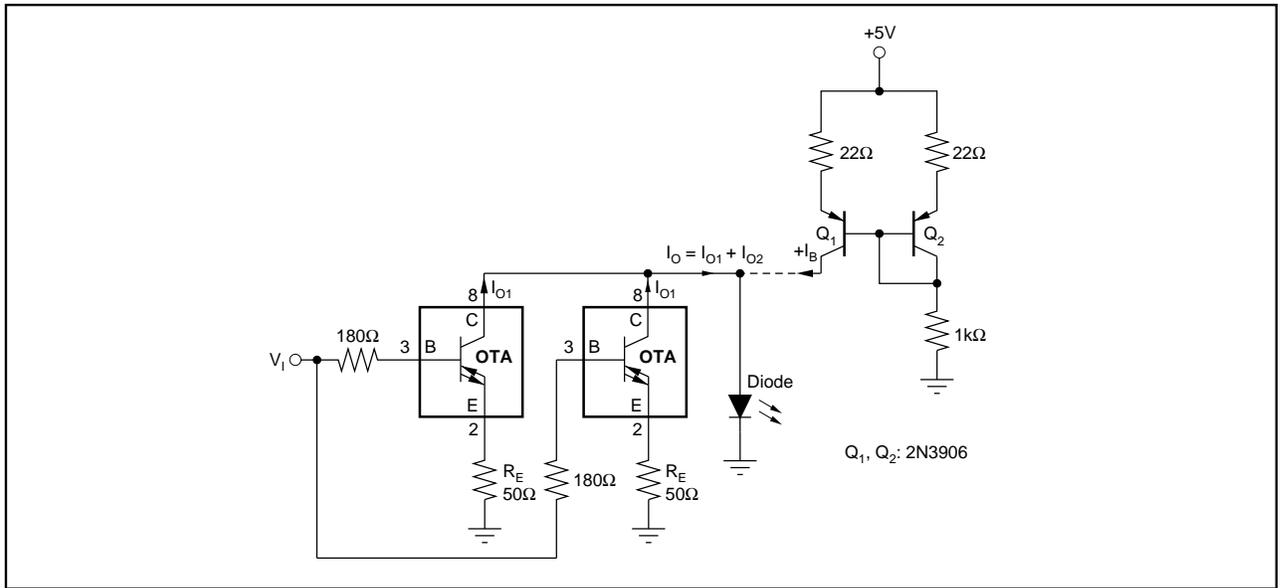


FIGURE 15. High Speed Current Driver.

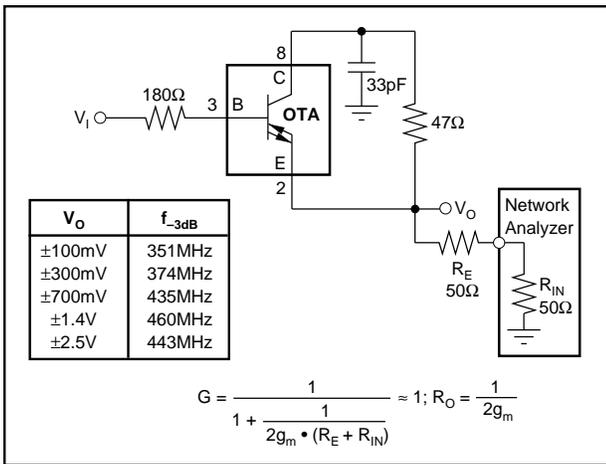


FIGURE 16. Voltage Buffer with Doubled-Output Current.

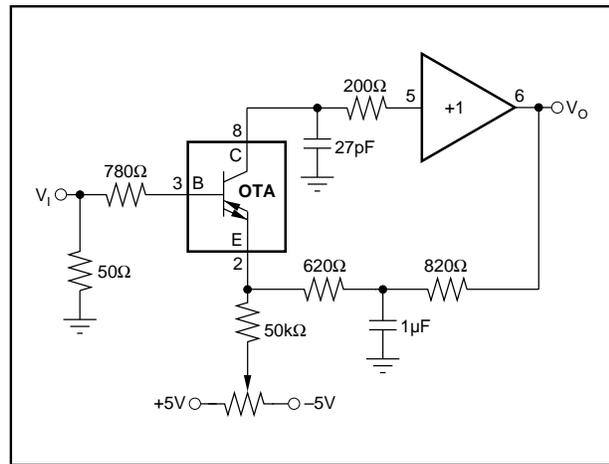


FIGURE 17. Integrator for ns-pulses.

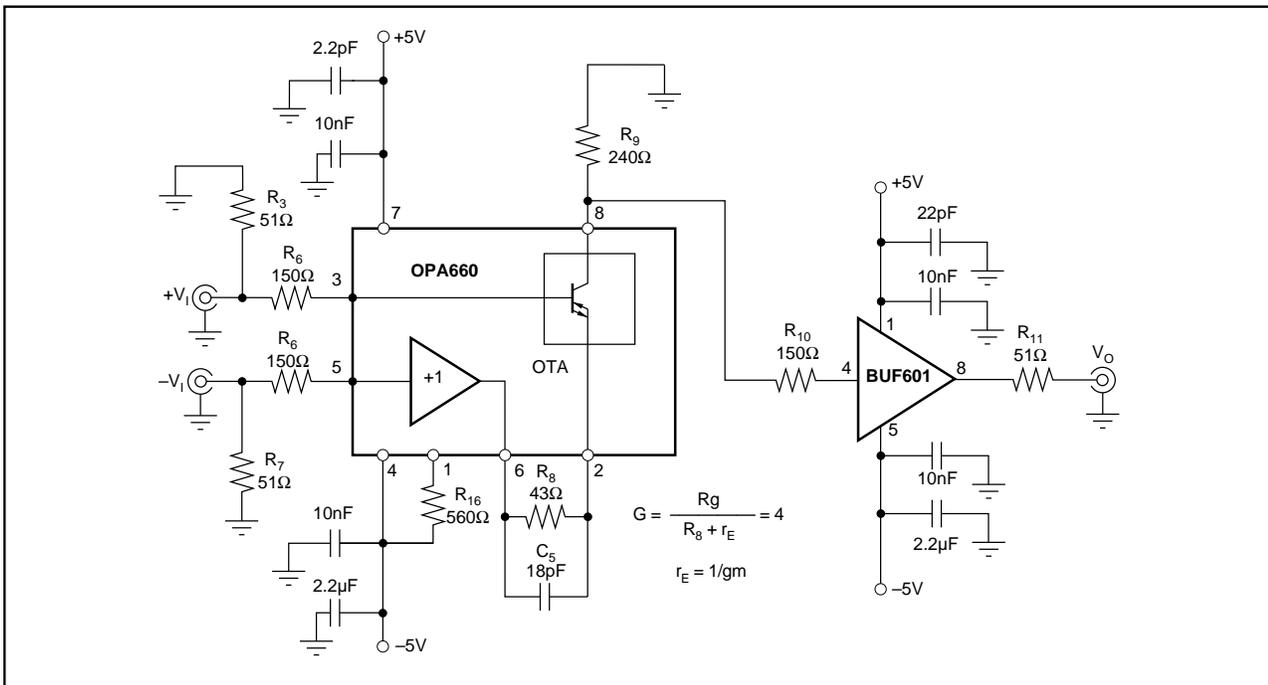


FIGURE 18. 400MHz Differential Amplifier

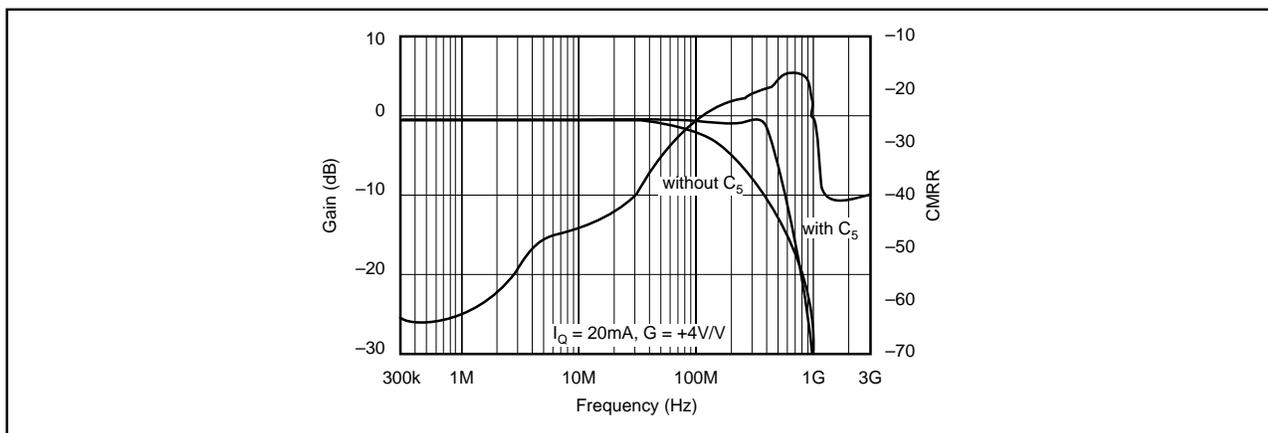


FIGURE 19. CMRR and Bandwidth of the Differential Amplifier

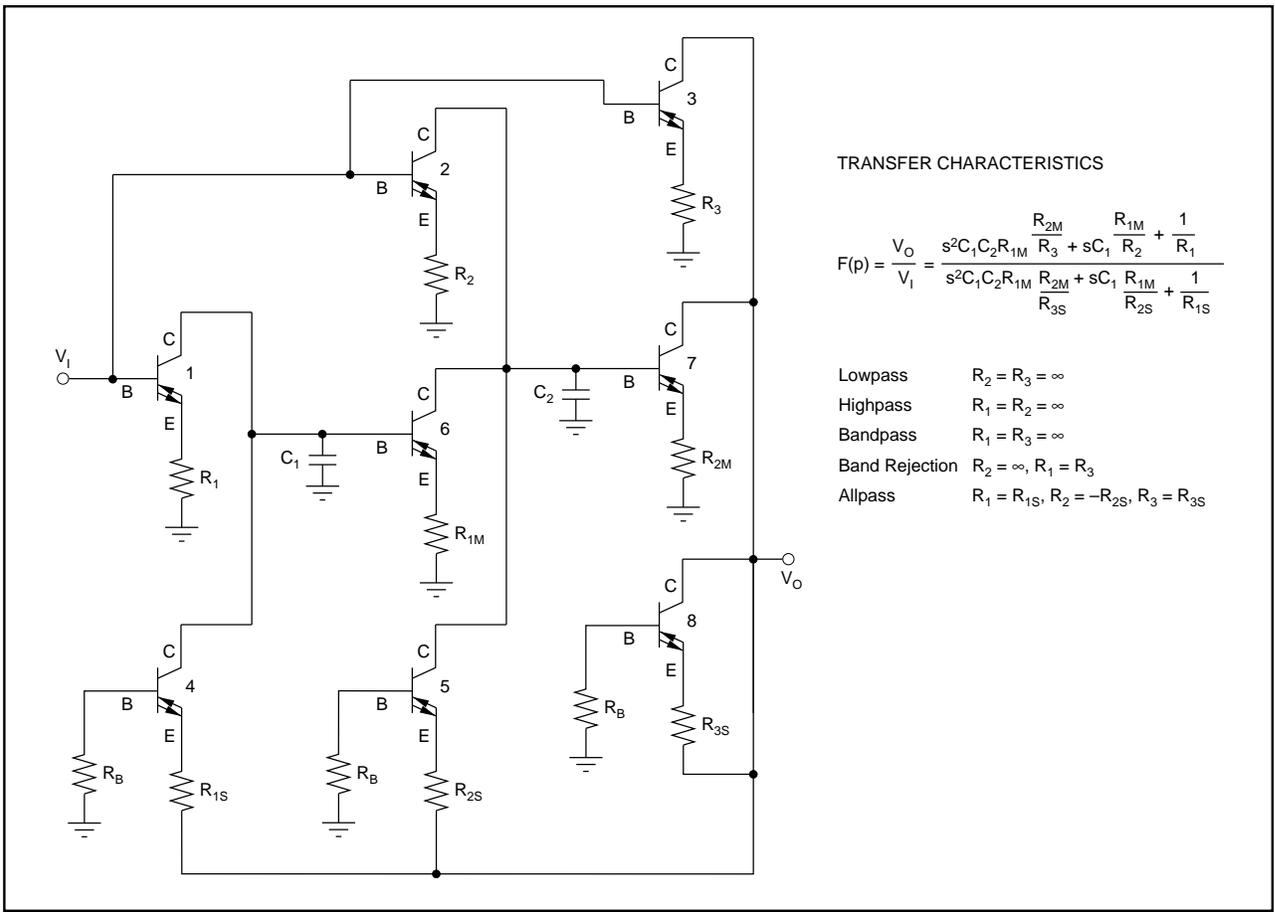


FIGURE 20. High Frequency Universal Active Filter.

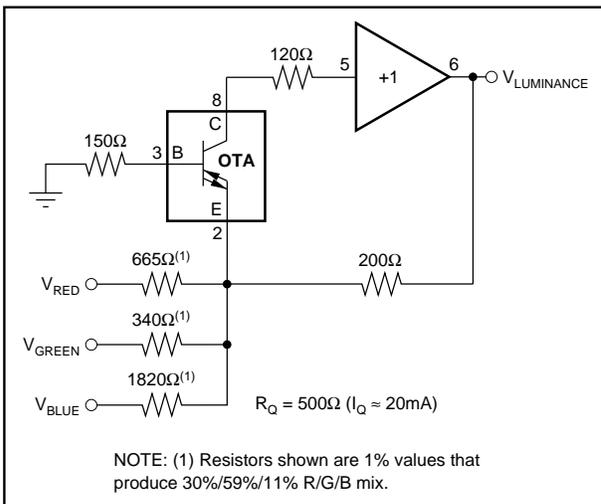


FIGURE 21. Video Luminance Matrix.

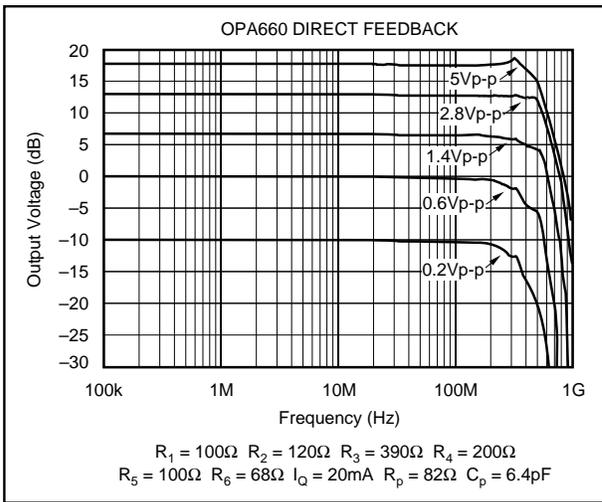


FIGURE 24. Frequency Response Direct-Feedback Amplifier.

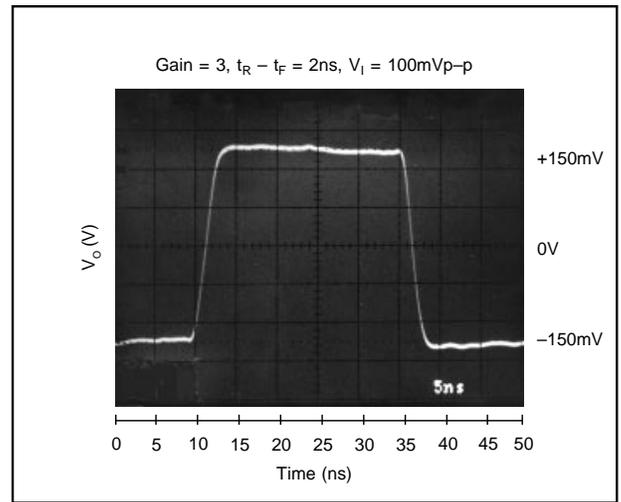


FIGURE 25. Direct-Feedback Amplifier Small-Signal Pulse Response.

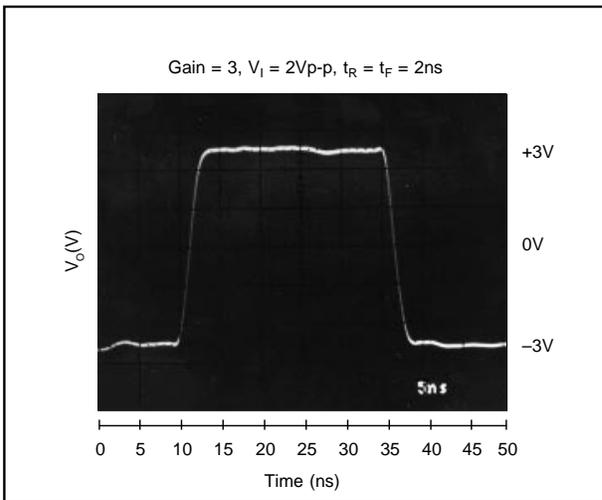


FIGURE 26. Direct-Feedback Amplifier Large-Signal Pulse Response.

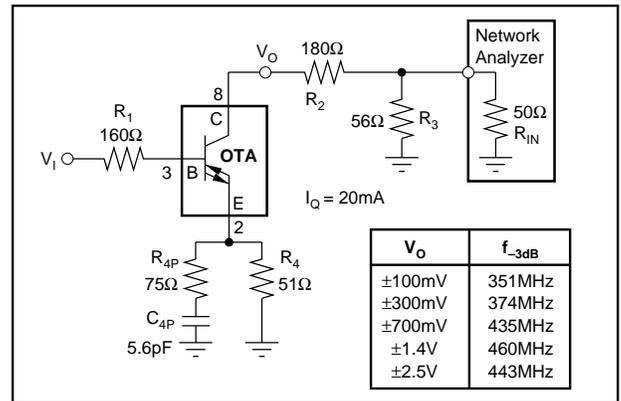


FIGURE 27. Forward Amplifier.

SPICE MODELS

Computer simulation using SPICE models is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits, where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available from Burr-Brown.

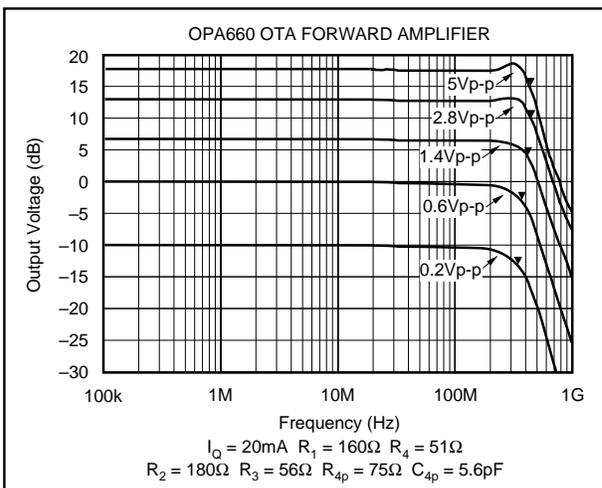
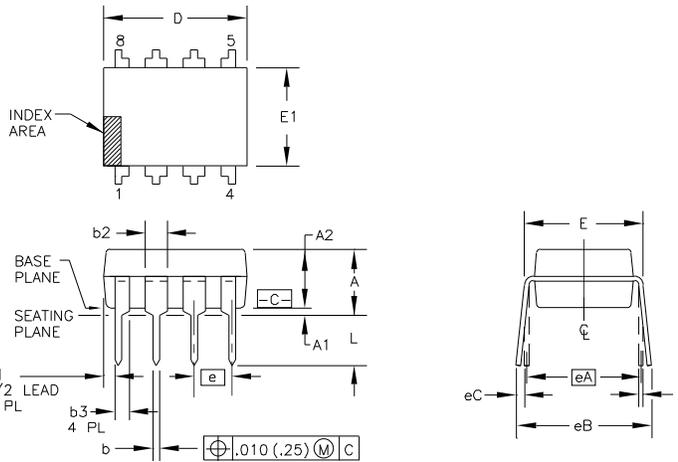


FIGURE 28. Frequency Response Forward Amplifier.

PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		N	E	DIM	INCHES		MILLIMETERS		N	E
	MIN.	MAX.	MIN.	MAX.				MIN.	MAX.	MIN.	MAX.		
A	--	.210	--	5.33	3		eC	.000	.060	0.00	1.52	6	
A1	.015	--	0.38	--	3		L	.115	.150	2.92	3.81	3	
A2	.115	.195	2.92	4.95			N	8		8		7	
b	.014	.022	0.36	0.56									
b2	.045	.070	1.14	1.78	9								
b3	.030	.045	0.76	1.14	9								
c	.008	.014	0.20	0.36									
D	.355	.400	9.02	10.16	4								
D1	.005	--	0.13	--	4								
E	.300	.325	7.62	8.26	5								
E1	.240	.280	6.10	7.11	4								
e	.100	BASIC	2.54	BASIC									
eA	.300	BASIC	7.63	BASIC	5								
eB	--	.430	--	10.92	6								

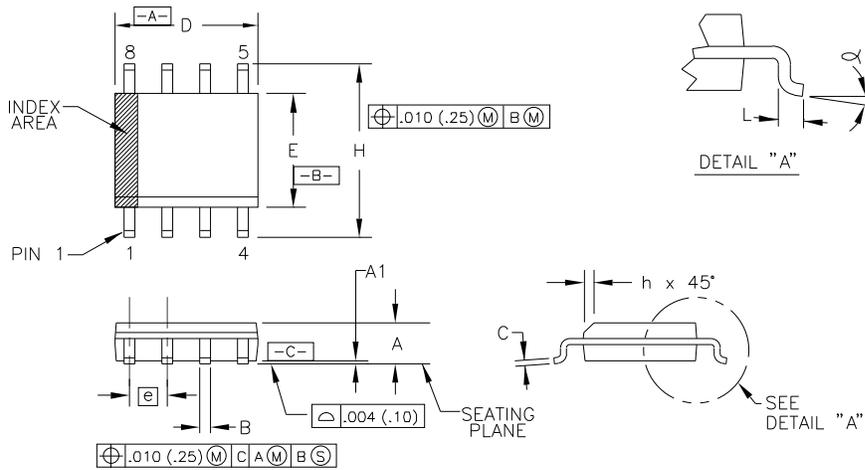
NOTES:

- ALL DIMENSIONS ARE IN INCHES.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
- D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
- E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM [-C-].
- eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
- N IS THE MAXIMUM OF TERMINAL POSITIONS.

- POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
- b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
- DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
- A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
- FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 REV.: E
JEDEC NUMBER: MS-001-BA

Package Number 182 - 8-Lead SOIC



DIM	INCHES		MILLIMETERS		N	E	DIM	INCHES		MILLIMETERS		N	E
	MIN.	MAX.	MIN.	MAX.				MIN.	MAX.	MIN.	MAX.		
A	.0532	.0688	1.35	1.75									
A1	.004	.0098	0.10	0.23									
B	.013	.020	0.33	0.51	7								
C	.0075	.0098	0.20	0.25									
D	.189	.1968	4.80	4.98	2								
E	.1497	.1574	3.80	4.00	3								
e	.050	BASIC	1.27	BASIC									
H	.2284	.244	5.80	6.20									
h	.0099	.0196	0.25	0.50									
L	.016	.050	0.41	1.27	5								
N	8		8		6								
α	0°	8°	0°	8°									

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
- DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
- THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT,

A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

- "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- "N" IS THE NUMBER OF TERMINAL POSITIONS.
- THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
- LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 REV.: G
JEDEC NUMBER: MS-012-AA