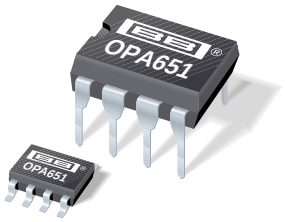
BURR-BROWN®



OPA651

Wideband, Low Power Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- STABLE IN GAINS: ≥ 2V/V
- LOW POWER: 50mW
- GAIN-BANDWIDTH: 940MHz at G = 2
- FAST SETTLING TIME: 16ns to 0.01%
- LOW HARMONICS: –78dB at 5MHz
- LOW INPUT BIAS CURRENT: 4μA
- DIFFERENTIAL GAIN/PHASE ERROR: 0.01%/0.025°
- LOW CURRENT NOISE DENSITY: 1.1pA/$\sqrt{\text{Hz}}$
- PACKAGE: 8-pin DIP and SO-8 Surface-Mount

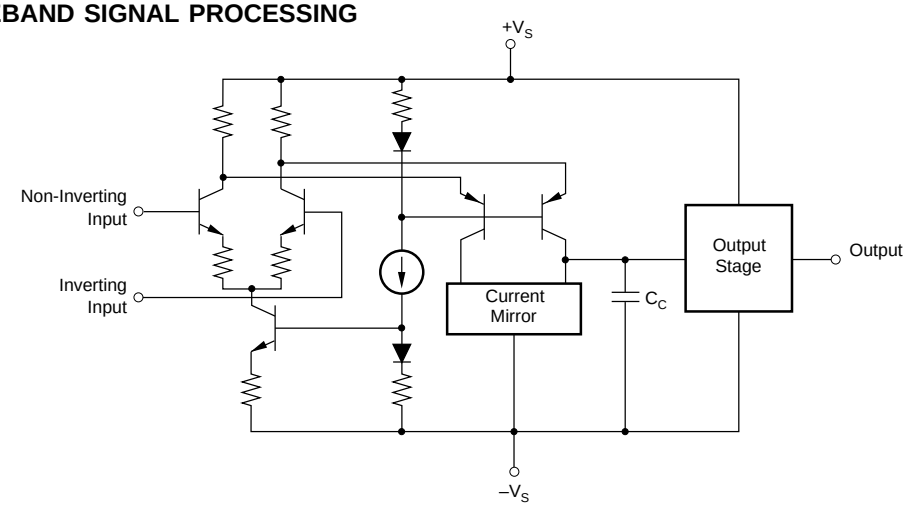
APPLICATIONS

- HIGH RESOLUTION VIDEO
- MONITOR PREAMPLIFIER
- CCD IMAGING AMPLIFIER
- ULTRASOUND SIGNAL PROCESSING
- ADC/DAC GAIN AMPLIFIER
- BASEBAND SIGNAL PROCESSING

DESCRIPTION

The OPA651 is a low power, wideband voltage feedback operational amplifier. It features a bandwidth of 470MHz as well as a 12-bit settling time of only 16ns. The wide bandwidth and true differential input stage make it suitable for use in a variety of applications. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA651 is decompensated for stability in gains of two or more, differentiating it from the unity gain stable OPA650. Its unusual combination of speed, accuracy and low power make it an outstanding choice for many portable, multi-channel and other high speed applications, where power is at a premium.



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PDS-1265A
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SPECIFICATIONS

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω unless otherwise noted.

PARAMETER	CONDITIONS	OPA651P, U MIN	OPA651P, U TYP	OPA651P, U MAX	OPA651PB, UB MIN	OPA651PB, UB TYP	OPA651PB, UB MAX	UNITS
FREQUENCY RESPONSE								
Closed-Loop Bandwidth[1]	G = +2		470			*[2]		MHz
	G = +5		70			*		MHz
	G = +10		34			*		MHz
Slew Rate[3]	G = +2, V_O = 2V step		300			*		V/µs
Over Specified Temperature			275			*		V/µs
Rise Time			4.5			*		ns
Fall Time			6.0			*		ns
Settling Time 0.01%	G = +2, V_O = 2V step		16.2			*		ns
0.1%	G = +2, V_O = 2V step		11.5			*		ns
1%	G = +2, V_O = 2V step		7.2			*		ns
Spurious Free Dynamic Range	G = +2, f = 5.0 MHz, V_O = 2Vp-p,							
	R_L = 100Ω		67			*		dBc
	R_L = 400Ω		78			*		dBc
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.01			*		%
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, R_L = 150Ω		0.025			*		Degrees
Bandwidth For 0.1dB Flatness	G = +2		43			*		MHz
INPUT OFFSET VOLTAGE								
Input Offset Voltage			±1	±5.0		0.6	±2.0	mV
Average Drift			±3			*		µV/°C
Power Supply Rejection (+V_S)	V_S = ±4.5V to ±5.5V	60	96		70	*		dB
(–V_S)		50	59		50	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		4	20		4	10	µA
Over Temperature			6	30		6	20	µA
Input Offset Current	V_{CM} = 0V		0.4	1.5		*	*	µA
Over Temperature			0.9	3.0		*	*	µA
INPUT NOISE								
Input Voltage Noise								
Noise Density, f = 100Hz			13			*		nV/√Hz
f = 10kHz			4.6			*		nV/√Hz
f = 1MHz			4.6			*		nV/√Hz
Voltage Noise, BW = 10Hz to 100MHz			46			*		µVrms
Input Bias Current Noise								
Current Noise Density, f = 0.1Hz to 20kHz			1.1			*		pA/√Hz
Noise Figure (NF)	R_S = 10kΩ		3.2			*		dB
	R_S = 50Ω		14			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range			±3.5			*		V
Over Specified Temperature		±2.5			*			V
Common-Mode Rejection	V_{CM} = ±0.5V	80	90		90	110		dB
	V_{CM} = ±1V		63			65		dB
INPUT IMPEDANCE								
Differential			60 || 1			*		kΩ || pF
Common-Mode			2.6 || 1			*		MΩ || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	42	50		45	51		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	40	49		42	50		dB
OUTPUT								
Voltage Output								
Over Specified Temperature	No Load	±2.2	±2.6		±2.4	*		V
	R_L = 250Ω	±2.2	±2.6		±2.4	*		V
	R_L = 100Ω	±2.0	±2.4		±2.1	*		V
Current Output	+25°C to Max Temperature	±40	+45/–55		±45	+47/–60		mA
Over Specified Temperature		±30	+42/–53		±35	+45/–56		mA
Short Circuit Current			60			*		mA
Output Resistance	1MHz, G = +2		0.03			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current			±5.1	±7.75		±5.1	±6.5	mA
Over Specified Temperature			±5.4	±8.75		±5.2	±7.5	mA
TEMPERATURE RANGE								
Specification: P, U, PB, UB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P			120			*		°C/W
U			170			*		°C/W

NOTES: (1) Bandwidth can be negatively affected by a non-optimal PC board layout. Refer to the demonstration board layout for details. (2) An asterisk (*) specifies the same value as the grade to the left. (3) Slew rate is rate of change from 10% to 90% of output voltage step.

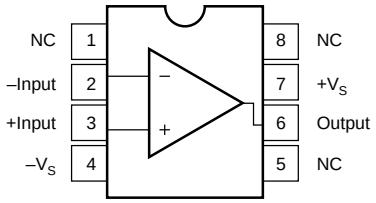
ABSOLUTE MAXIMUM RATINGS

Supply	±5.5V
Internal Power Dissipation[1]	See Thermal Considerations
Differential Input Voltage	Total V_S
Input Voltage Range	±5V
Storage Temperature Range: P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SO-8 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PIN CONFIGURATION

Top View **8-Pin DIP/SO-8**



PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
OPA651U	SO-8 Surface-Mount	182
OPA651UB	SO-8 Surface-Mount	182
OPA651P	8-Pin Plastic DIP	006
OPA651PB	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION[1]

MODEL	PACKAGE	TEMPERATURE RANGE
OPA651U	SO-8 Surface-Mount	–40°C to +85°C
OPA651UB	SO-8 Surface-Mount	–40°C to +85°C
OPA651P	8-Pin Plastic DIP	–40°C to +85°C
OPA651PB	8-Pin Plastic DIP	–40°C to +85°C

NOTE: (1) The "B" grade of the SO-8 package will be marked with a "B" by pin 8. Refer to mechanical section for the location.

ELECTROSTATIC DISCHARGE SENSITIVITY

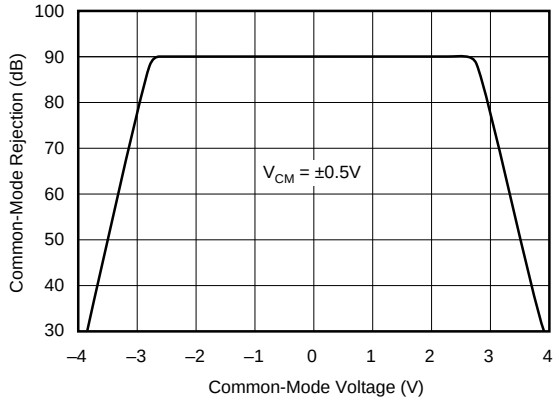
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

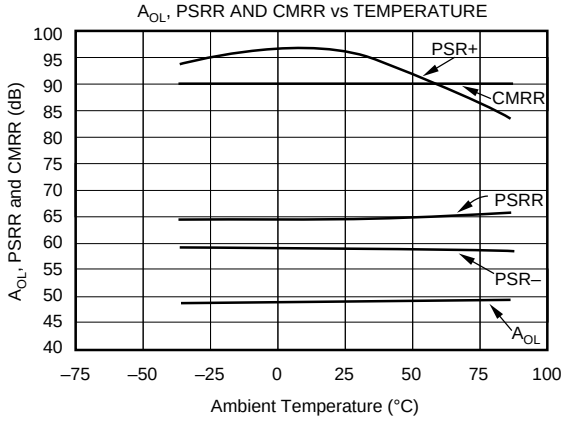
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, G = +2 unless otherwise noted.

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE



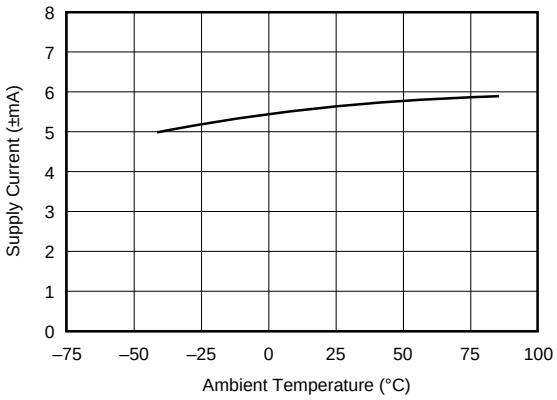
A_{OL}, PSRR AND CMRR vs TEMPERATURE



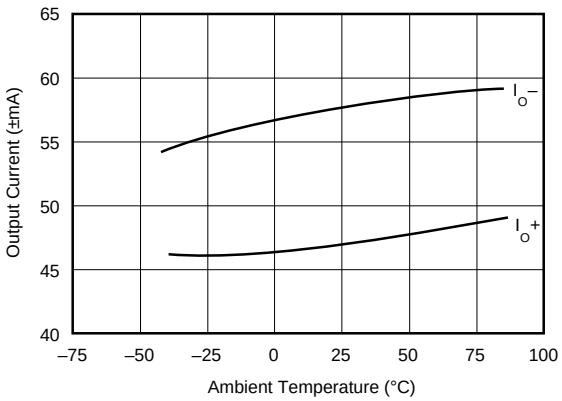
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, G = +2 unless otherwise noted.

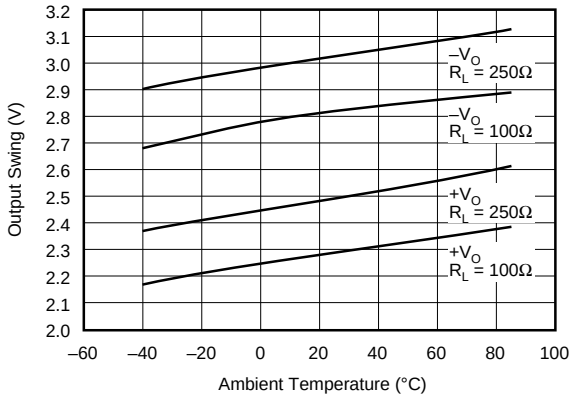
SUPPLY CURRENT vs TEMPERATURE



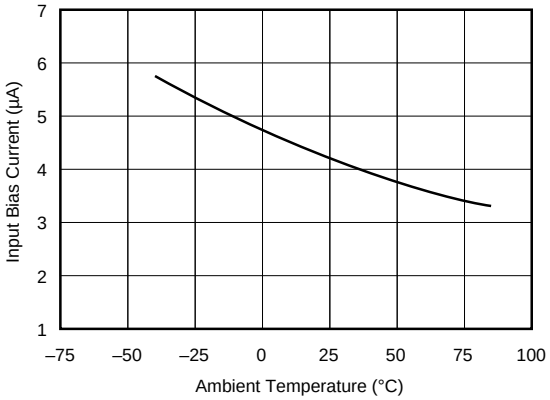
OUTPUT CURRENT vs TEMPERATURE



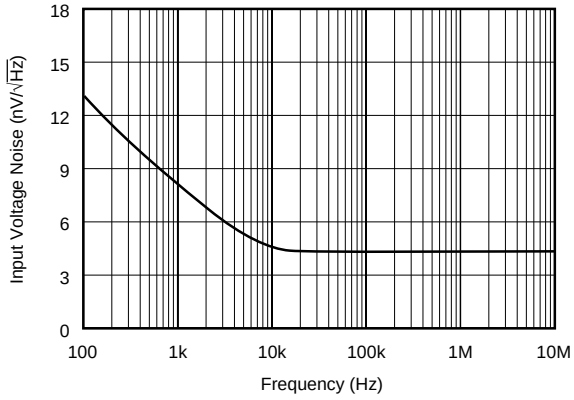
OUTPUT SWING vs TEMPERATURE



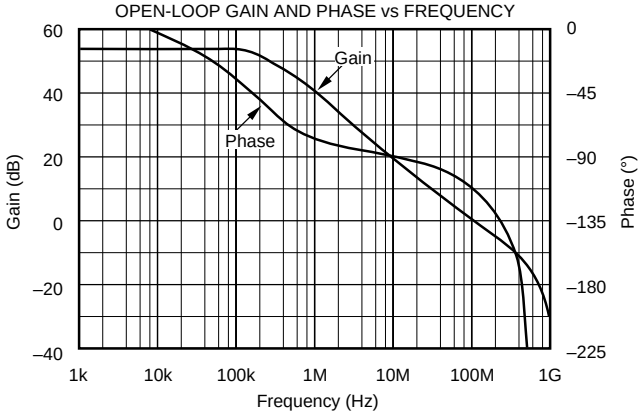
INPUT BIAS CURRENT vs TEMPERATURE



INPUT VOLTAGE NOISE DENSITY vs FREQUENCY



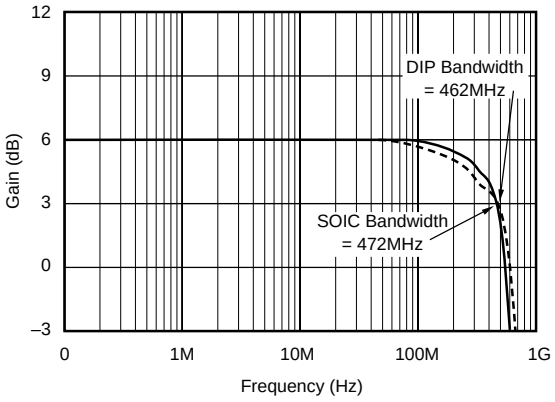
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



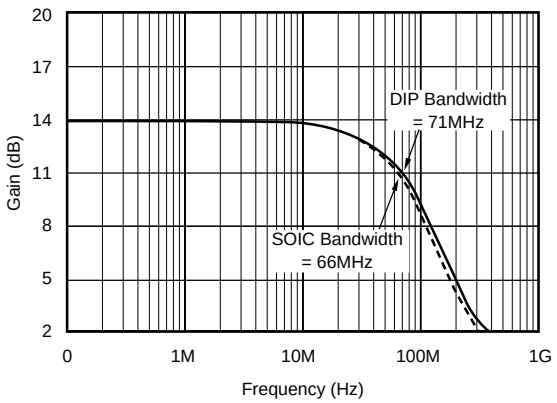
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, G = +2 unless otherwise noted.

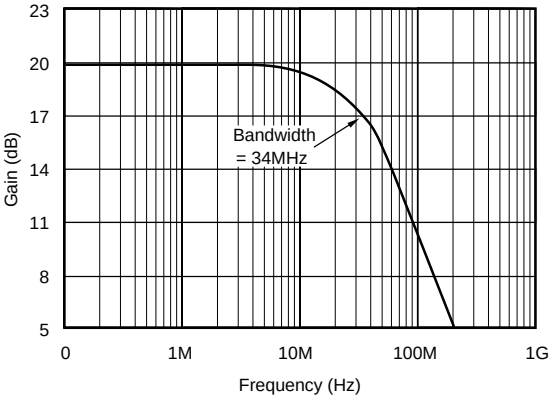
SMALL SIGNAL BANDWIDTH
G = +2 CLOSED-LOOP



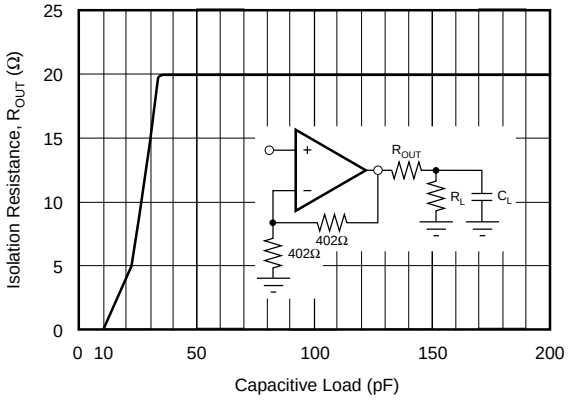
SMALL SIGNAL BANDWIDTH
G = +5 CLOSED-LOOP



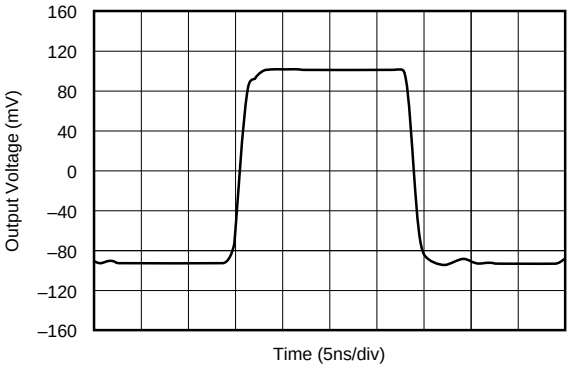
SMALL SIGNAL BANDWIDTH
G = +10 CLOSED-LOOP



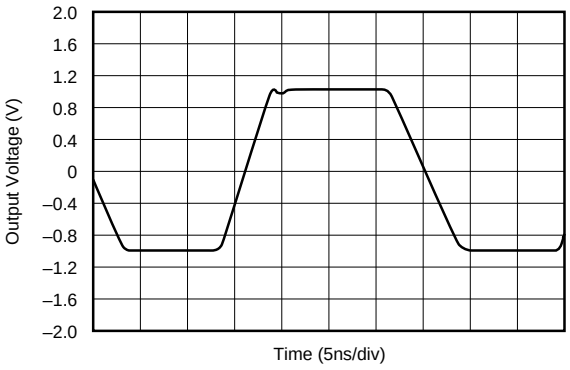
RECOMMENDED ISOLATION RESISTANCE
vs CAPACITIVE LOAD



SMALL SIGNAL TRANSIENT RESPONSE
(G = +2)



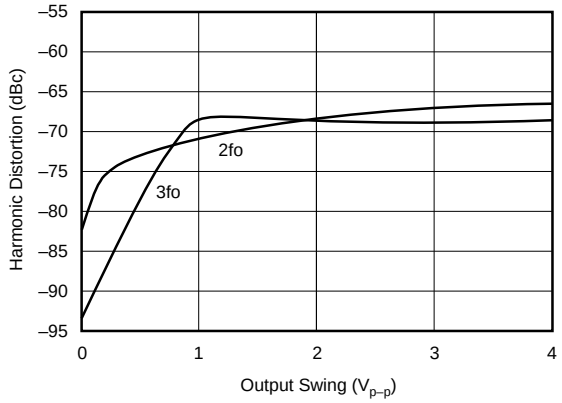
LARGE SIGNAL TRANSIENT RESPONSE
(G = +2)



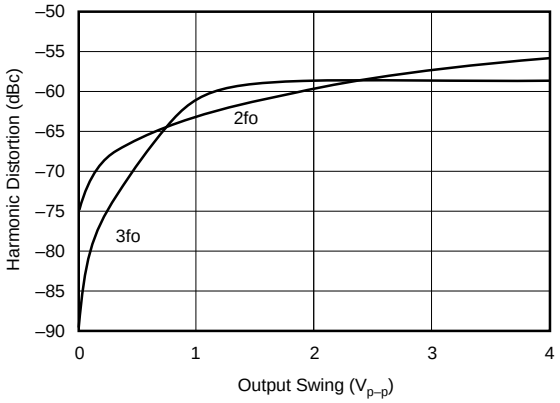
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, G = +2 unless otherwise noted.

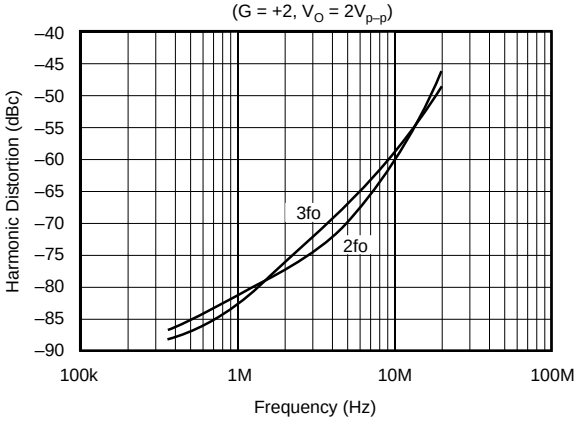
5MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = +2)



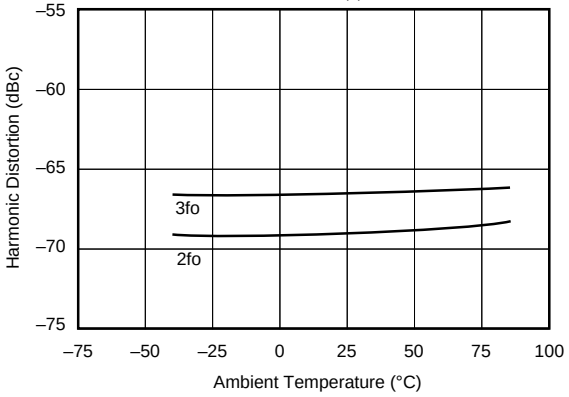
10MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = +2)



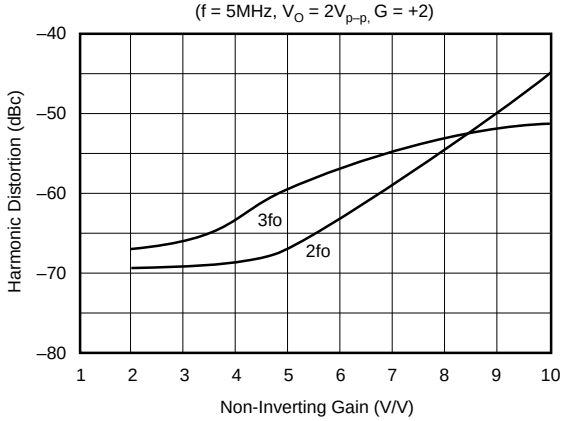
HARMONIC DISTORTION vs FREQUENCY
(G = +2, V_O = $2V_{p–p}$)



HARMONIC DISTORTION vs TEMPERATURE
(f = 5MHz, V_O = $2V_{p-p}$, G = +2)



HARMONIC DISTORTION vs GAIN
(f = 5MHz, V_O = $2V_{p–p,}$ G = +2)



DISCUSSION OF PERFORMANCE

The OPA651 is a low power, voltage feedback operational amplifier which is stable in noise gains of two or greater. The design of the OPA651 uses a conventional voltage-feedback architecture with a true high impedance differential input stage. This allows it to be used in all traditional operational amplifier applications, while giving fast settling times and low current noise.

For applications requiring low power and unity gain, refer to the voltage-feedback OPA650.

WIRING PRECAUTIONS/CIRCUIT LAYOUT

Maximizing the OPA651's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low impedance signal paths, and should be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray parasitic circuits.

As with all high frequency circuits, grounding is the most important application consideration for the OPA651. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (1 ounce copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low impedance common return path for signal and power, and conduct heat from active circuit package pins into ambient air by convection. However, do not place the ground plane under or near the inputs.

Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2µF tantalum electrolytic in parallel with a 0.1µF ceramic capacitor is recommended, particularly if the leads are kept as short as possible. Surface-mount bypass capacitors are best due to their low lead inductance. If necessary, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Power supply bypassing with 0.1µF and 2.2µF surface mount capacitors on the topside of the PC Board is recommended. It is essential to keep the 0.1µF capacitor very close to the power supply pins. Refer to the demonstration board layout in Figures 7a through 7d.

2) Use surface-mount components, whenever possible. Do not use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if wires must be used, very short and direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface-mount feedback network components on the back side of PC board. Good component selection is essential. Capacitors used in critical locations should be low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary p-n diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA651 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 402Ω) in a gain of +2V/V or greater for the best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "noninductive" types) are **unacceptable** in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the back side of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the data sheet. A longer feedback path than this will decrease the realized bandwidth substantially.

6) As mentioned above, surface mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA651U (SO-8 package) will offer the best AC performance. The parasitic package inductance and capacitance for the SO-8 is lower than the 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that the amplifier must drive its own feedback network as well as the load. Lowest distortion is achieved with high impedance loads.

8) The OPA651 is designed for ±5V supplies. Although they will operate well with +5V and –5.2V, use of ±15V supplies will destroy them.

9) Standard commercial test equipment has not been designed to test devices in the OPA651's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission

line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards are not satisfactory. A clean layout using RF techniques is essential.

ESD PROTECTION

ESD damage has been well recognized for MOSFET devices, but any semiconductor device is vulnerable to this potentially damaging source. This is particularly true for very high speed, fine geometry processes.

ESD damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, ESD handling precautions are strongly recommended when handling the OPA651.

OUTPUT DRIVE CAPABILITY

The OPA651 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive a 2Vp-p into a 75Ω load. This drive capability makes the OPA651 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as driving A/D converters require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitance at the input of flash A/D converters. As shown in Figure 1, the OPA651 maintains very low-closed loop output impedance over frequency. Closed-loop output impedance increases with frequency as loop gain decreases.

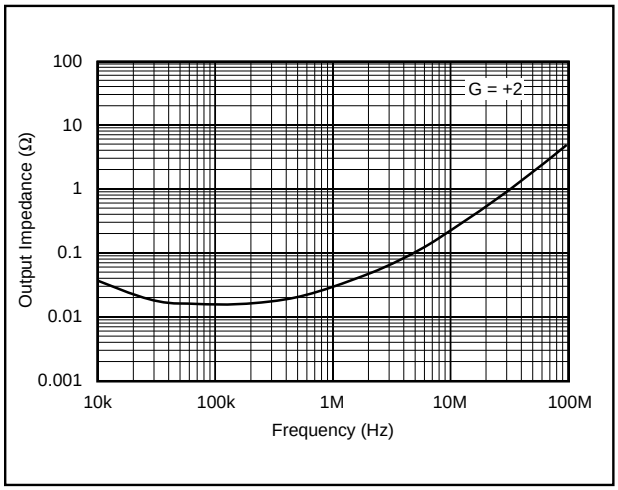


FIGURE 1. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA651 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_S = \pm 5V$, P_{DQ} = 10V x 8.75mA = 87.5mW, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_S/2$, and is equal to P_{DL}, max = $(\pm V_S)^2/4R_L$. Note that it is the voltage across the output transistor, not the load, that determines the power dissipated in the output stage.

CAPACITIVE LOADS

The OPA651's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be isolated by connecting a small resistance, usually 5Ω to 20Ω, in series with the output as shown in Figure 2. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +2 will improve the capacitive load drive due to increased phase margin.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

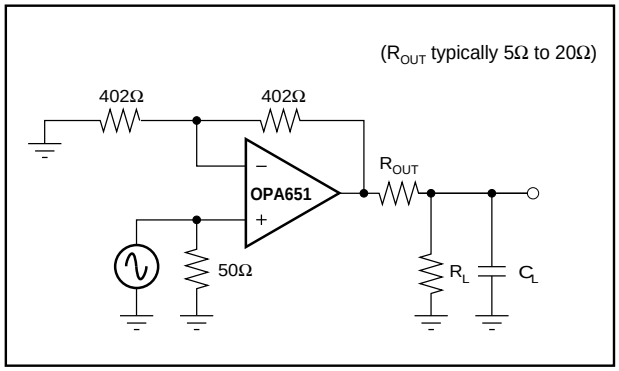


FIGURE 2. Driving Capacitive Loads.

COMPENSATION

The OPA651 is a decompensated version of the OPA650 and is stable in noise gains greater than or equal to two with a phase margin of approximately 70°. Using the OPA651 in a gain of two or greater improves phase margin and reduces the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Therefore, if unity gain is required, it is advised that the OPA650 be used in place of the OPA651. Gain and phase response for other gains are shown in the Typical Performance Curves.

The high frequency response of the OPA651 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high-frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed loop gains are required, a three-resistor attenuator (tee-network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of two, occurs in only 16ns to 0.01% for a 2 volt output step, making the OPA651 one of the faster settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions."

Settling time measurements on the OPA651 can be very difficult to perform. Accurate measurement requires special test equipment. A fast flat-top pulse generator and high speed oscilloscope are needed. Unfortunately, fast flat-top pulse generators, which settle to 0.01% in sufficient time, are expensive. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is the percentage change in closed-loop gain over a specified change in output voltage level. DP is defined as the phase change (in degrees) of the same output voltage change. DG and DP are both specified at the NTSC subcarrier frequency of 3.58MHz. DG and DP increase closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA651's Harmonic Distortion characteristics into a 100Ω load are shown versus frequency and power output in the typical performance curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 3. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

NOISE FIGURE

The OPA651 voltage noise spectral density is specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA651's Noise Figure vs Source Resistance is shown in Figure 4.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE macro models are available for the OPA651. Contact Burr-Brown Applications Department to receive a SPICE diskette.

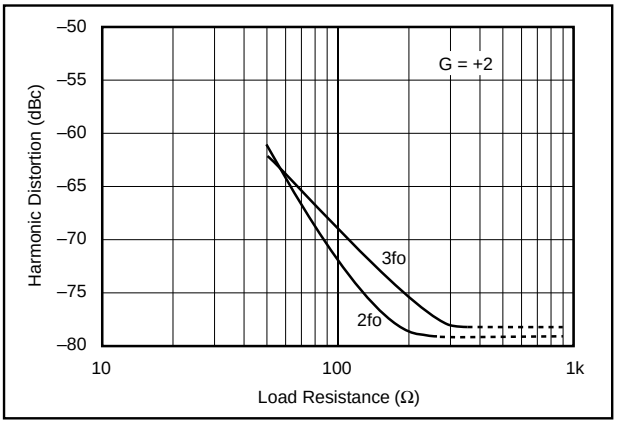


FIGURE 3. 5MHz Harmonic Distortion vs Load Resistance.

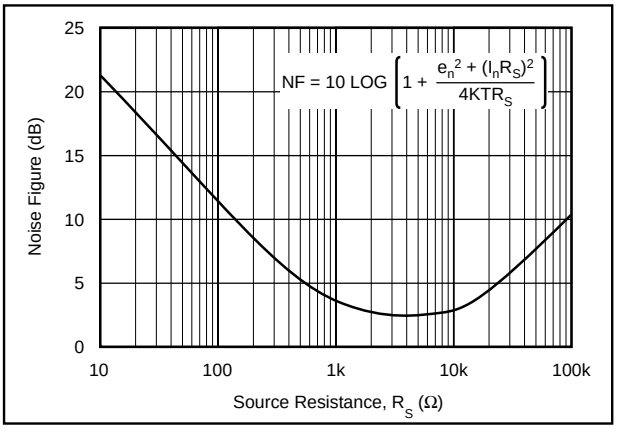


FIGURE 4. Noise Figure vs Source Resistance.

TYPICAL APPLICATION

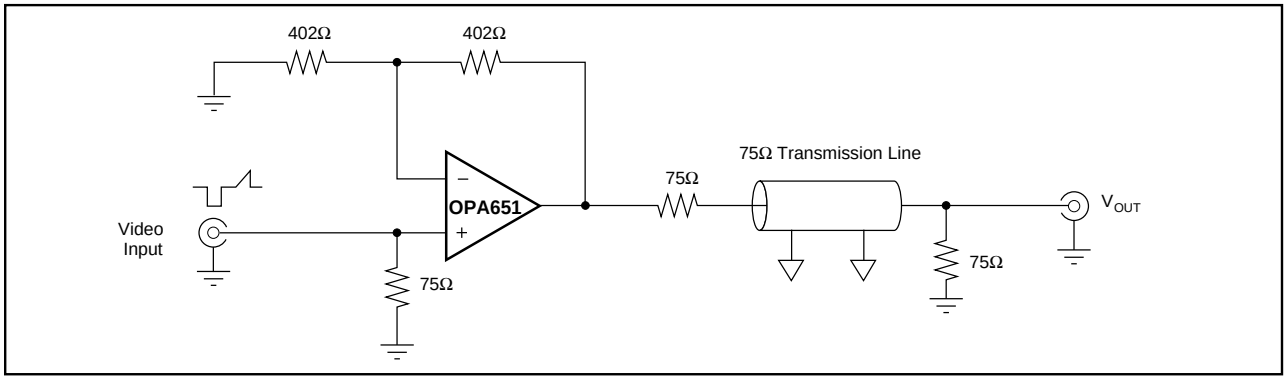
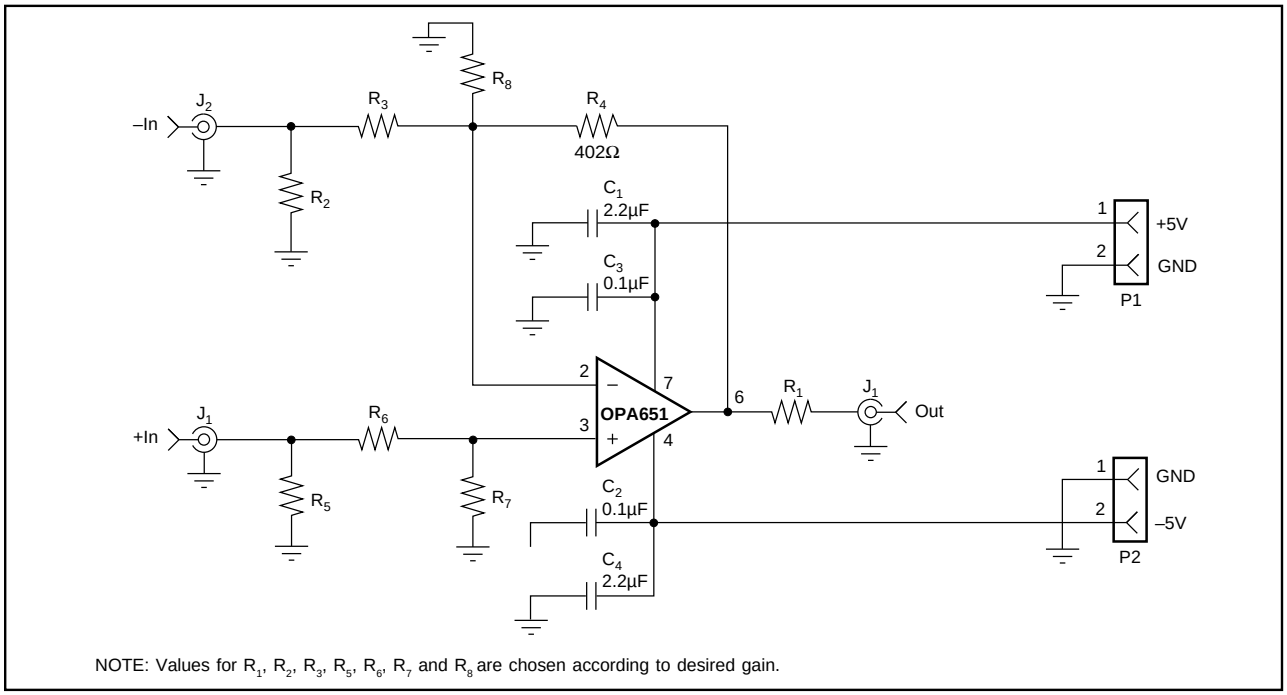


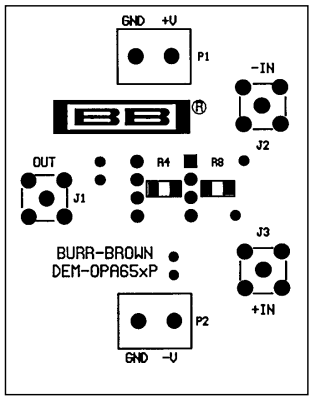
FIGURE 5. Low Distortion Video Amplifier.



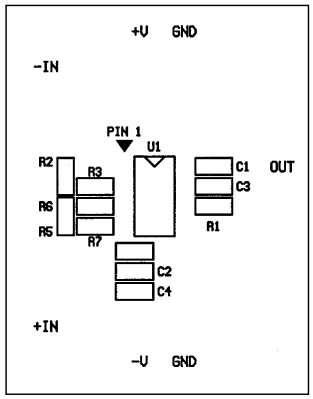
NOTE: Values for R_1, R_2, R_3, R_5, R_6, R_7 and R_8 are chosen according to desired gain.

FIGURE 6. Layout Detail For DEM-OPA65X Demonstration Board.

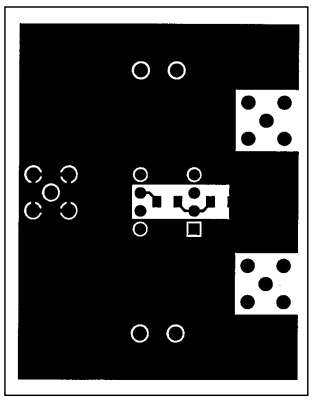
DEM-OPA65XP Demonstration Board Layout



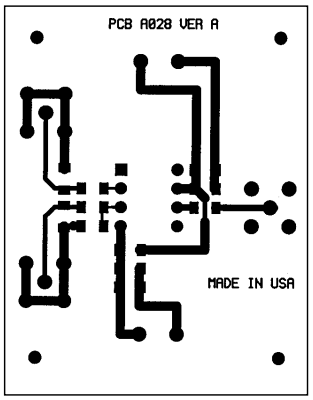
(A)



(B)



(C)

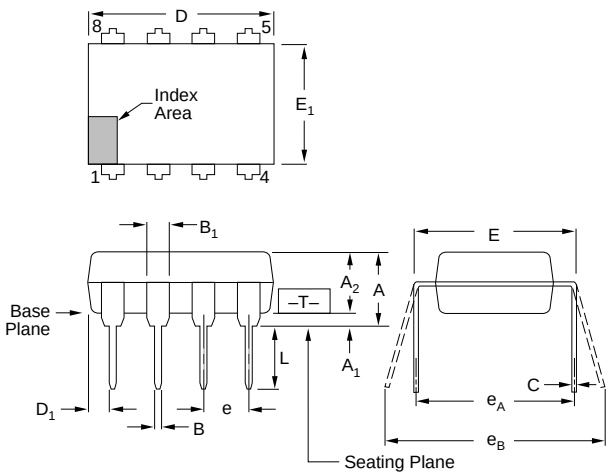


(D)

FIGURE 7a. Evaluation Board Silkscreen (Solder Side). 7b. Evaluation Board Silkscreen (Component Side). 7c. Evaluation Board Layout (Solder Side). 7d. Evaluation Board Layout (Component Side).

PACKAGE DRAWINGS

Package Number 006 — 8-Pin Plastic Single-Wide DIP

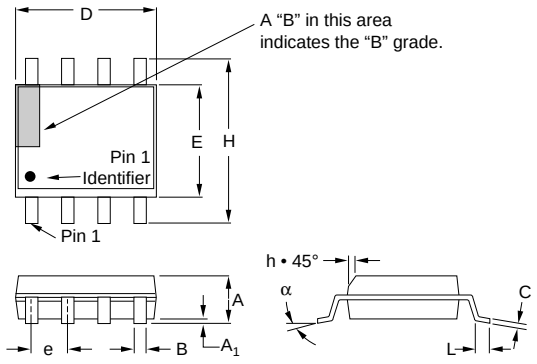


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A (3)	—	.210	—	5.33
A_1 (3)	.015	—	0.38	—
A_2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B_1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D (4)	.348	.430	8.84	10.92
D_1	.005	—	0.13	—
E (5)	.300	.325	7.62	8.26
E_1 (4)	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
e_A (5)	.300 BASIC		7.63 BASIC	
e_B (6)	—	.430	—	10.92
L (3)	.115	.160	2.92	4.06
N (7)	8		8	

(1) Controlling dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.

(2) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(3) Dimensions A, A_1, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(4) D and E_1 dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E and eA measured with the leads constrained to be perpendicular to plane T.
(6) eB is measured at the lead tips with the leads unconstrained.
(7) N is the maximum number of terminal positions.
(8) Corner leads (1, 4, 5, and 8) may be configured as shown in Figure 2.
(9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines.

Package Number 182 — 8-Pin SO-8 Surface Mount



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.054	.068	1.37	1.73
A_1	.004	.009	0.10	0.23
B	.014	.019	0.36	0.48
C	.008	.0098	0.20	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
H	.229	.244	5.82	6.20
h	.010	.019	0.25	0.48
L	.016	.050	0.41	1.27
N	8		8	
α	0°	8°	0°	8°

NOTES:
1. Dimensioning and tolerancing per ANSI Y14.5M–1982.
2. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.086 in.)
3. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
4. "L" is the length of the terminal for soldering to a substrate.
5. "N" is the number of terminal positions.