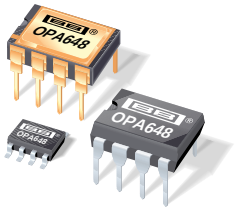
BURR-BROWN®



OPA648

ULTRA-WIDEBAND CURRENT FEEDBACK OPERATIONAL AMPLIFIER

FEATURES

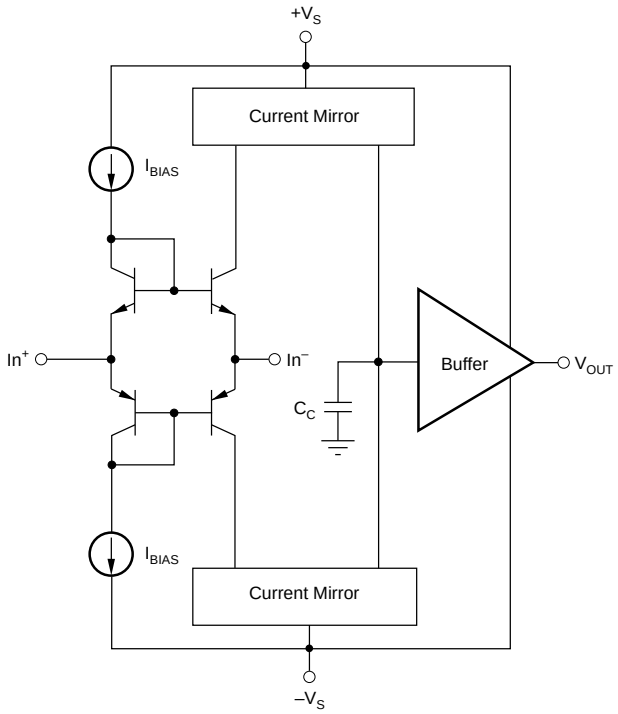
- WIDE BANDWIDTH: 1GHz
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.02%/0.02°
- GAIN FLATNESS: 0.1dB to 100MHz
- FAST SLEW RATE: 1200V/µs
- CLEAN PULSE RESPONSE
- UNITY GAIN STABLE

APPLICATIONS

- HIGH-SPEED SIGNAL PROCESSING
- HIGH-RESOLUTION CRT PREAMP
- HIGH-RESOLUTION VIDEO
- PULSE AMPLIFICATION
- IF SIGNAL PROCESSING
- DAC I/V CONVERSION
- ADC BUFFER

DESCRIPTION

The OPA648 is an ultra high bandwidth current feedback operational amplifier. The current feedback architecture also allows for a very high slew rate, which gives excellent large signal bandwidth, even at high gains. The high slew rate and well-behaved pulse response allow for superior large signal amplification in a variety of RF, video and other signal processing applications. Fabricated on an advanced complementary bipolar process, the OPA648 offers exceptional performance in monolithic form.



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Printed in U.S.A June, 1995

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 243Ω unless otherwise noted.

PARAMETER	CONDITIONS	OPA648H, P, U			
		MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
Small Signal Bandwidth[1]	G = +1		1.0		GHz
	G = +2		600		MHz
Slew Rate[2]	G = +2, 1V Step		1200		V/µs
Settling Time					
0.01%	G = +2, 1V Step		20		ns
0.1%	G = +2, 1V Step		9		ns
1%	G = +2, 1V Step		3		ns
Spurious Free Dynamic Range	G = +2, f = 5.0MHz, V_O = 2Vp-p		60		dBc
	G = +2, f = 20.0MHz, V_O = 2Vp-p		51		dBc
Differential Gain, G = +2	3.58MHz, V_O = 1.4Vp-p, R_L = 150Ω		0.02		%
Differential Phase, G = +2	3.58MHz, V_O = 1.4Vp-p, R_L = 150Ω		0.02		degrees
Gain Flatness	DC to 100MHz		0.1		dB
OFFSET VOLTAGE					
Input Offset Voltage			±2	±6	mV
Average Drift			±10		µV/°C
Power Supply Rejection Ratio	V_S = ±4.5 to ±5.5V	45	58		dB
INPUT BIAS CURRENT					
Non-Inverting			±12	±65	µA
Over Specified Temperature			±30	±95	µA
Inverting			±20	±65	µA
Over Specified Temperature			±50	±95	µA
NOISE					
Input Voltage Noise					
Noise Density, f = 100Hz			10.4		nV/√Hz
f = 1kHz			2.3		nV/√Hz
f = 10kHz			2.3		nV/√Hz
f = 1MHz			2.3		nV/√Hz
Voltage Noise, BW = 10Hz to 200MHz			32.5		µVrms
Input Bias Current Noise					
Current Noise Density, f = 0.1Hz to 20kHz			15		pA/√Hz
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±2	±2.25		V
Common-Mode Rejection	V_{CM} = ±0.5V	35	55		dB
INPUT IMPEDANCE					
Non-inverting			22 || 0.75		kΩ || pF
Inverting			20		Ω
OPEN-LOOP TRANSIMPEDANCE					
Open-Loop Transimpedance	V_O = ±2V, R_L = 1kΩ	100	165		kΩ
OUTPUT					
Current Output		33	45		mA
Over Specified Temperature		25	40		mA
Voltage Output	No Load				
Over Specified Temperature		±2.75	±3.0		V
Voltage Output	R_L = 150Ω	±2.2	±2.5		V
Over Specified Temperature		±2.0	±2.3		V
Short-Circuit Current			75		mA
Output Resistance	1MHz, G = +2V/V		0.08		Ω
POWER SUPPLY					
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	V
Quiescent Current			±13	±20	mA
Over Specified Temperature			±15	±23	mA
TEMPERATURE RANGE					
Specification	Ambient	–40		+85	°C
Storage	Ambient	–55		+150	°C
Thermal Resistance, θ_{JA}					
P			120		°C/W
U			170		°C/W
H			120		°C/W

NOTES: (1) Bandwidth can be degraded by a non-optimal PC board layout. Refer to the DEM-OPA64X datasheet for layout recommendations. (2) Slew rate is the rate of change from 10% to 90% of the output voltage step.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation[1]	See Thermal Considerations
Differential Input Voltage	Total V_S
Input Voltage Range	±5V
Storage Temperature Range: H	–65°C to +150°C
P	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SO-8 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA648H	8-Pin Ceramic Sidebraze DIP	157
OPA648P	8-Pin Plastic Single-Wide DIP	006
OPA648U	8-Pin Surface Mount	182

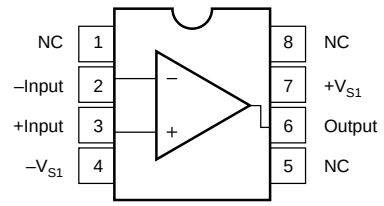
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA648H	8-Pin Ceramic Sidebraze DIP	–40°C to +85°C
OPA648P	8-Pin Plastic Single-Wide DIP	–40°C to +85°C
OPA648U	8-Pin Surface Mount	–40°C to +85°C

PIN CONFIGURATION (All Packages)

Top View **8-Pin Ceramic/DIP/SO-8**



ELECTROSTATIC DISCHARGE SENSITIVITY

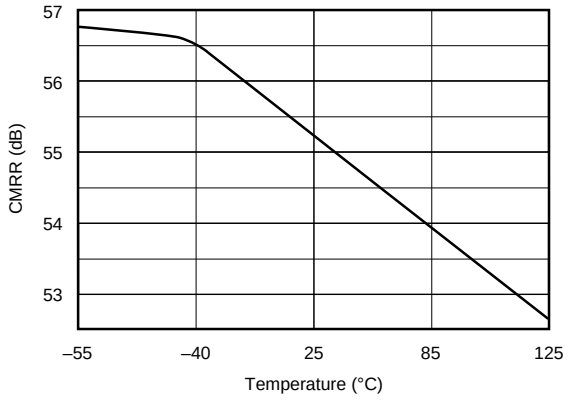
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

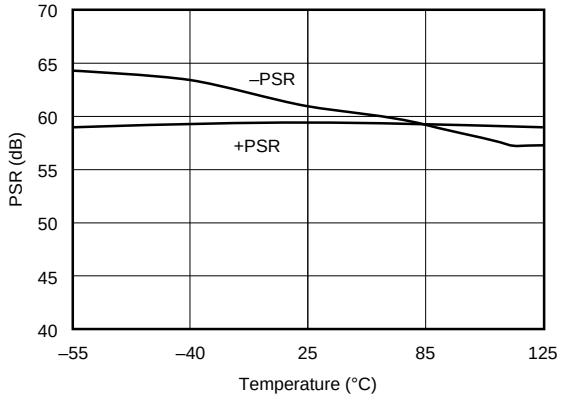
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 243Ω unless otherwise noted.

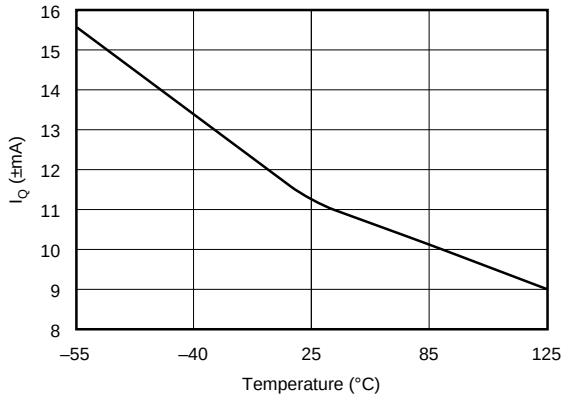
COMMON-MODE REJECTION vs TEMPERATURE



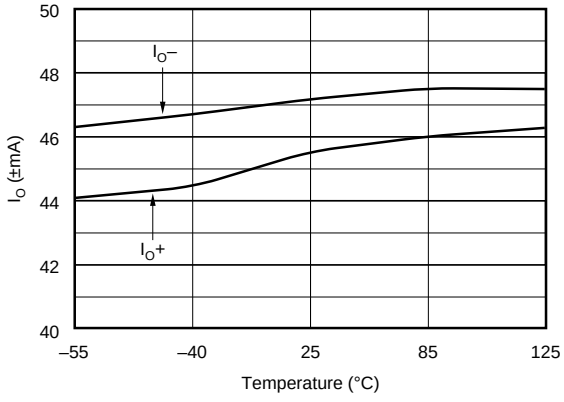
POWER SUPPLY REJECTION vs TEMPERATURE



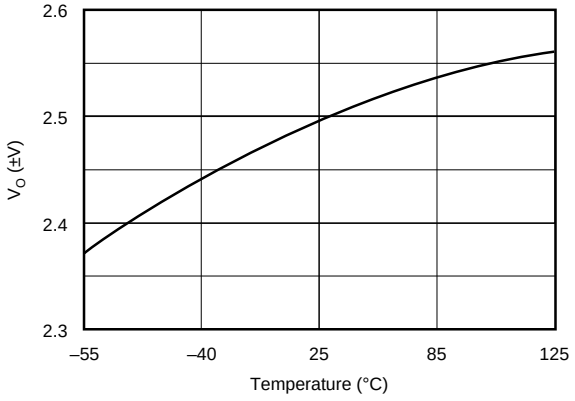
SUPPLY CURRENT vs TEMPERATURE



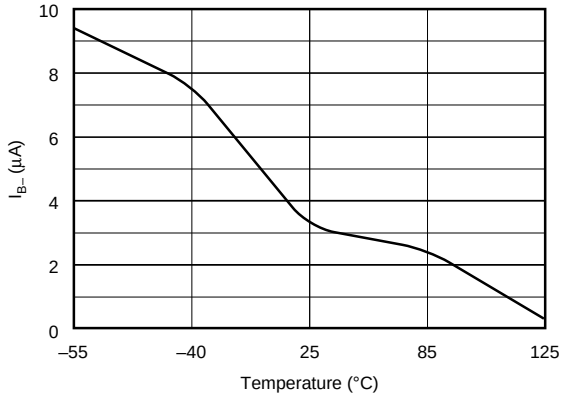
OUTPUT CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING
vs TEMPERATURE (R_L = 150Ω)



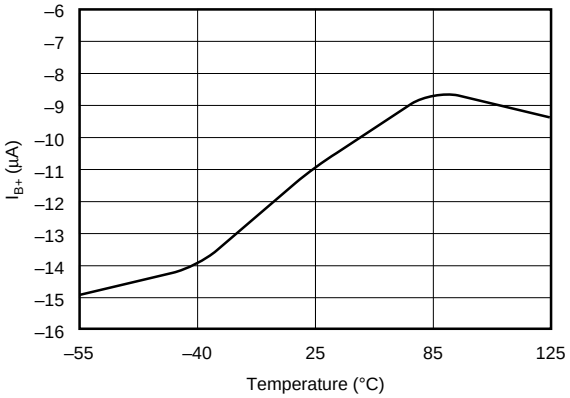
INVERTING INPUT BIAS CURRENT vs TEMPERATURE



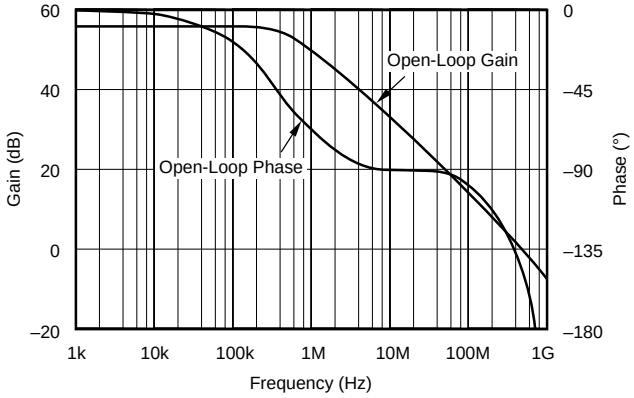
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 243Ω unless otherwise noted.

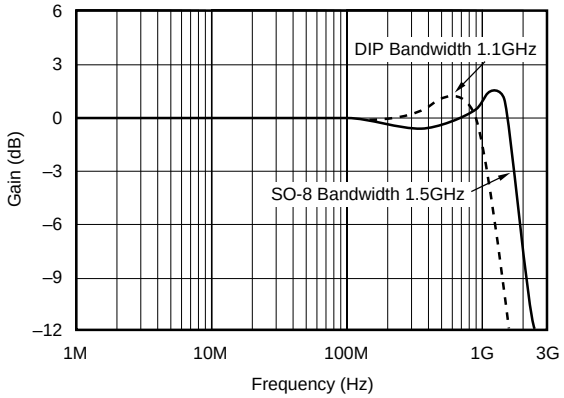
NON-INVERTING INPUT BIAS CURRENT vs TEMPERATURE



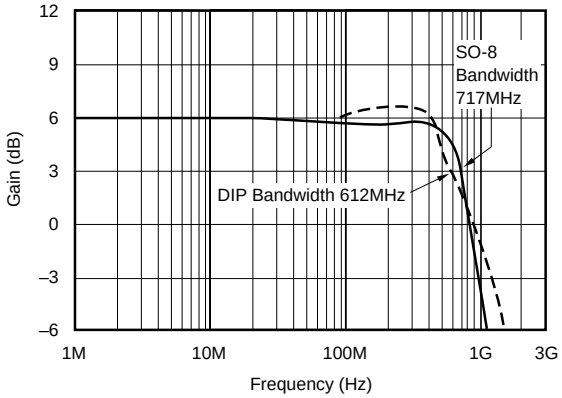
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



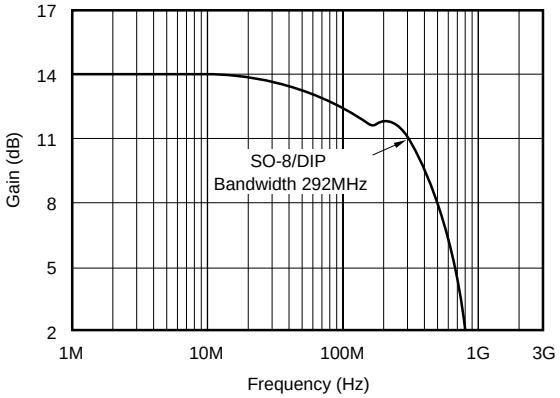
G = +1 CLOSED-LOOP BANDWIDTH



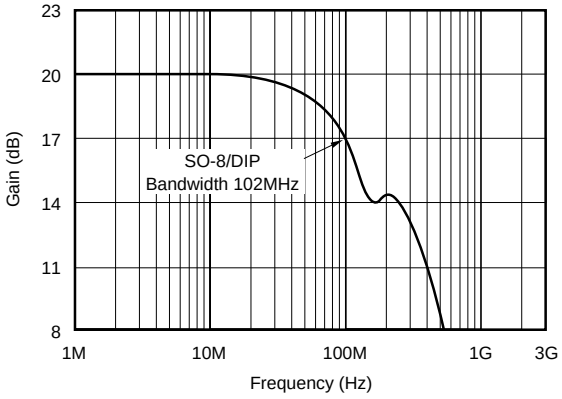
G = +2 CLOSED-LOOP BANDWIDTH



G = +5 CLOSED-LOOP BANDWIDTH



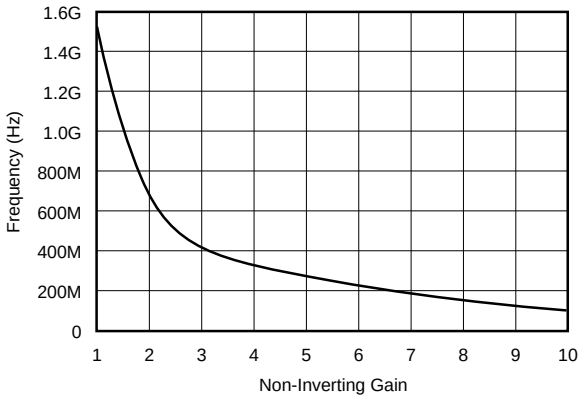
G = +10 CLOSED-LOOP BANDWIDTH



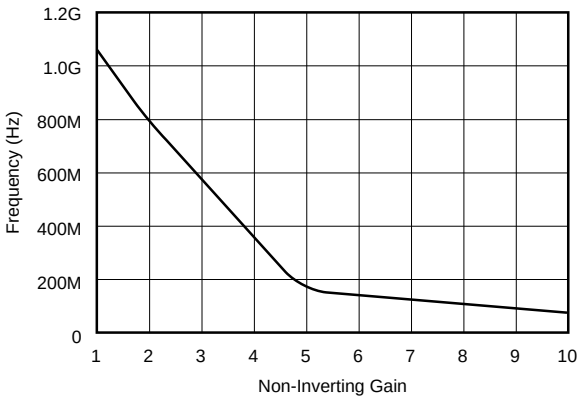
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 243Ω unless otherwise noted.

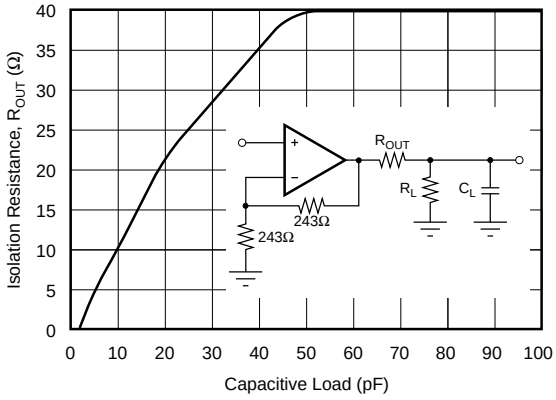
SO-8 CLOSED-LOOP BANDWIDTH vs GAIN



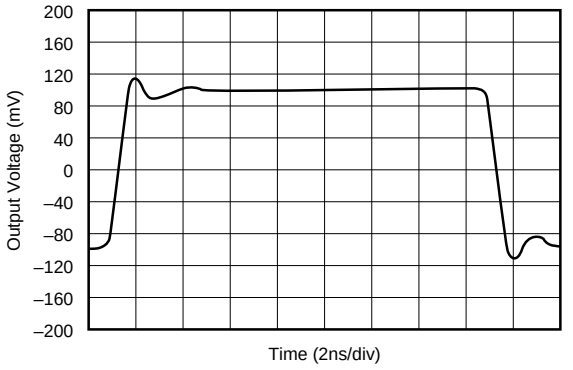
DIP CLOSED-LOOP BANDWIDTH vs GAIN



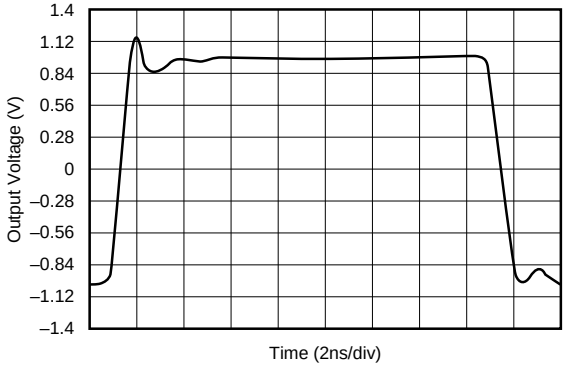
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD (G = +2)



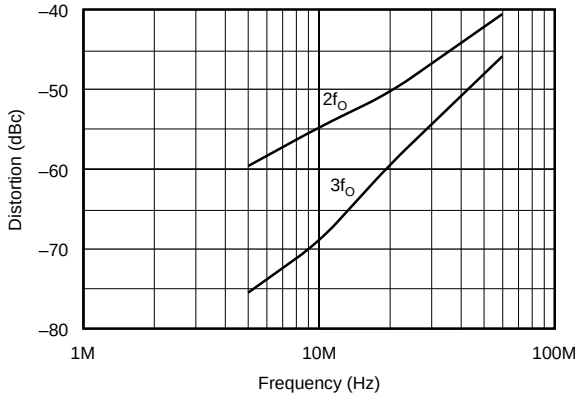
SMALL SIGNAL TRANSIENT RESPONSE (G = +2)



LARGE SIGNAL TRANSIENT RESPONSE (G = +2)



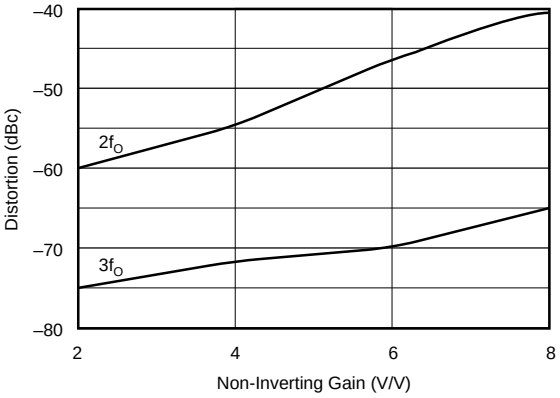
DISTORTION vs FREQUENCY (G = +2, V_O = 2Vp-p)



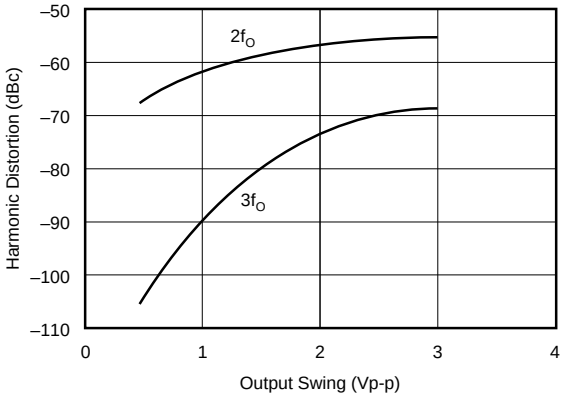
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, and R_{FB} = 243Ω unless otherwise noted.

DISTORTION vs GAIN
(f_O = 5MHz, V_O = 2Vp-p)



10MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = +2)



APPLICATIONS INFORMATION

THEORY OF OPERATION

This current feedback architecture offers the following important advantages over voltage feedback architectures: (1) the high slew rate allows the large signal performance to approach the small signal performance, and: (2) there is less bandwidth degradation at higher gain settings.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open-loop transimpedance gain (T_O). The output signal generated is equal to T_O X I_E. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

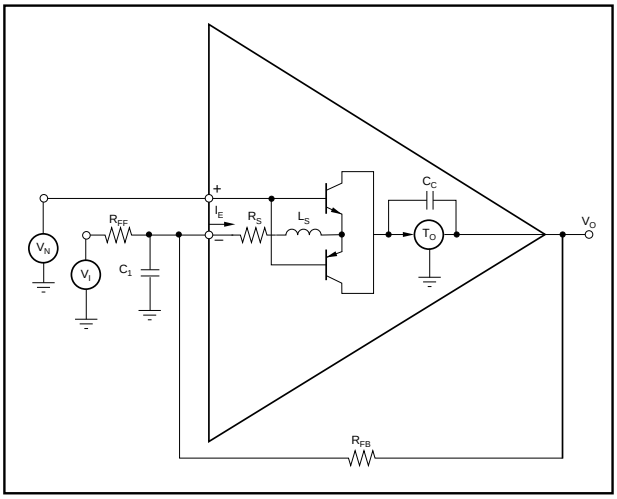


FIGURE 1. Equivalent Circuit.

For non-inverting operation, the input signal is applied to the non-inverting (high impedance buffer) input. The output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is (1 + R_{FB}/R_{FF}).

Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current feedback amplifier has a low inverting (buffer output) impedance and a high non-inverting (buffer input) impedance.

The closed-loop gain for the OPA648 can be calculated using the following equations:

$$\text{Inverting Gain} = \frac{-\left(\frac{R_{FB}}{R_{FF}}\right)}{1+\frac{1}{\text{Loop Gain}}} \quad (1)$$

$$\text{Non–Inverting Gain} = \frac{\left[1+\frac{R_{FB}}{R_{FF}}\right]}{1+\frac{1}{\text{Loop Gain}}} \quad (2)$$

$$\text{where Loop Gain} = \left[\frac{T_O}{R_{FB}+R_S\left(1+\frac{R_{FB}}{R_{FF}}\right)}\right]$$

At higher gains the small value inverting input impedance causes an apparent loss in bandwidth. This can be seen from the equation:

$$f_{\text{ACTUAL BW}} = \frac{f_{\text{IDEAL BW}}}{\left[1+\left(\frac{R_S}{R_{FB}}\right)\times\left(1+\frac{R_{FB}}{R_{FF}}\right)\right]} \quad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 243Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input voltage and current sources that influence DC operation. The output offset is calculated by the following equation:

$$\text{Output Offset Voltage} = \pm Ib_N \times R_N (1 + R_{FB}/R_G) \pm V_{IO} \quad (4)$$
$$(1 + R_{FB}/R_G) \pm Ib_I \times R_{FB}$$

If all terms are divided by the gain $(1 + R_F/R_G)$, it can be observed that input referred offsets improve as gain increases.

The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of equation 4 and applying the spectral noise values found in the Typical Performance Curve–graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed-loop gain increases (by keeping R_F fixed and reducing R_I with $R_N = 0\Omega$).

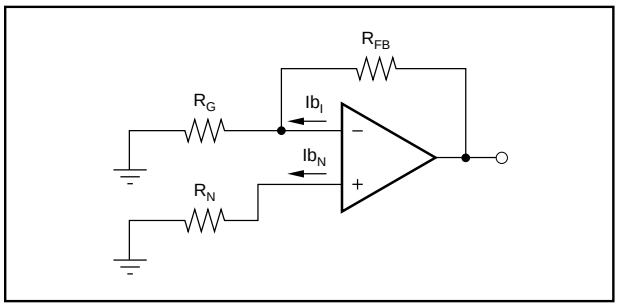


FIGURE 2. Output Offset Voltage Equivalent Circuit.

WIRING PRECAUTIONS

Maximizing the OPA648's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA648, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (1oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.1µF ceramic must also be added. Surface-mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply inductance seen by the input and output stages. This will improve the AC performance including lower distortion. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface mount capacitors is recommended. It is essential to keep the 0.1µF capacitor very close to the power supply pins. Refer to the demonstration board figure in the DEM-OPA64X datasheet for the recommended layout and component placements. (2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on the backside of the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA648 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 243Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are abso-

lutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. A longer feedback path than this will decrease the realized bandwidth substantially. Refer to the demonstration board layout at the end of the datasheet.

6) Surface-mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA648U (SO-8 package) will offer the best AC performance. The parasitic package impedance for the SO-8 is lower than the both the 8-pin Ceramic and 8-pin Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA648's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA648 incorporates on-chip ESD protection diodes as shown in Figure 3. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

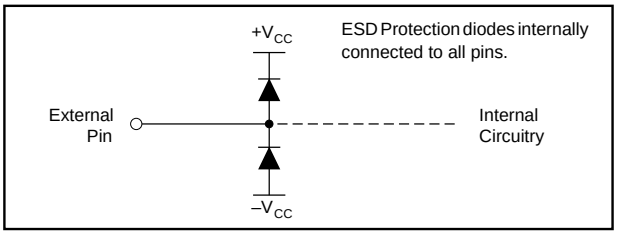


FIGURE 3. Internal ESD Protection.

All pins on the OPA648 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

The OPA648 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the machine model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA648.

OUTPUT DRIVE CAPABILITY

The OPA648 has been optimized to drive 75Ω and 100Ω resistive loads. This high-output drive capability makes the OPA648 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 4, the OPA648 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

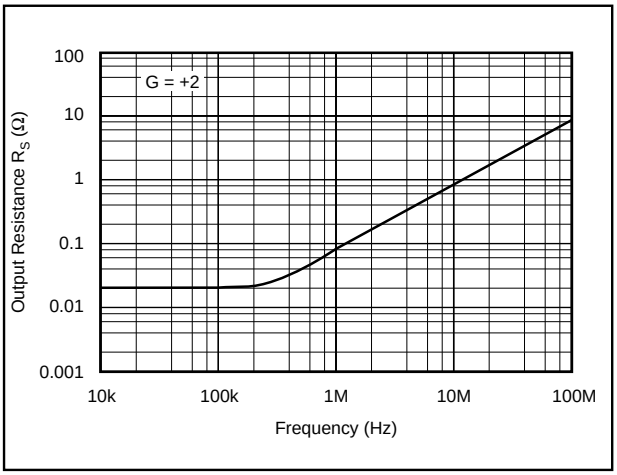


FIGURE 4. Output Resistance vs Frequency.

THERMAL CONSIDERATIONS

The OPA648 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_S = \pm 5V$, $P_{DQ} = 10V \times 23mA = 230mW$,

max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$), the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_S/2$, and is equal to P_{DL}, max = $(\pm V_S)^2 / 4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA648's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 40Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters.

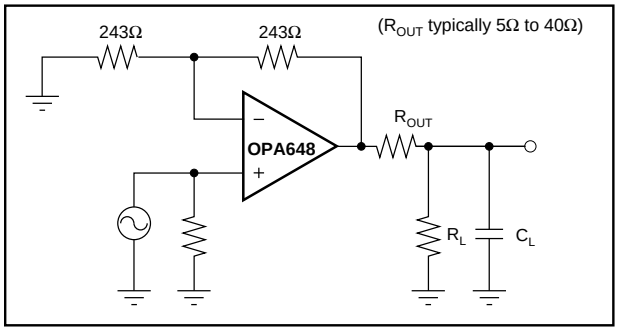


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA648 is internally compensated and is stable in unity gain with a phase margin of approximately 68°. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA648 in a good layout is very flat with frequency.

DISTORTION

The OPA648's harmonic distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

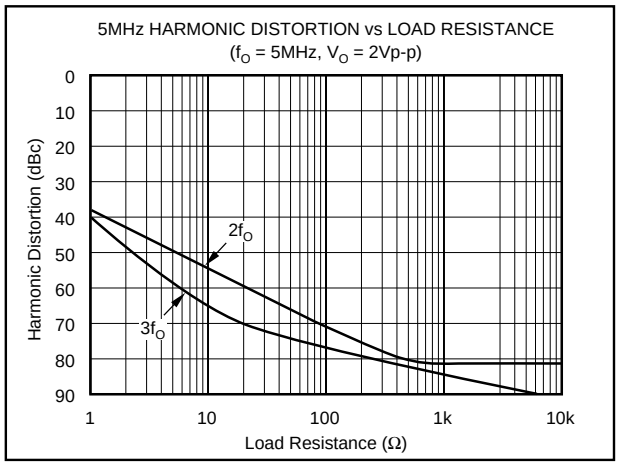


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

DG and DP of the OPA648 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 7 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to

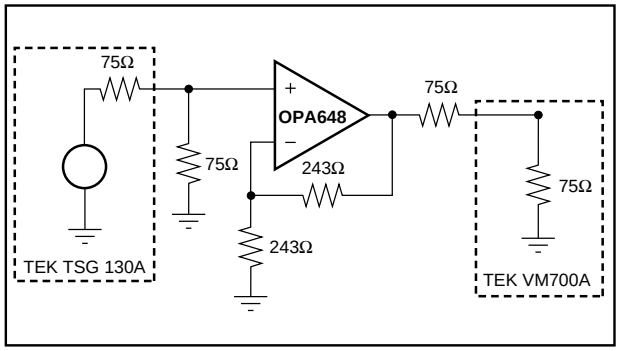


FIGURE 7. Configuration for Testing Differential Gain/Phase.

eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA648 is 0.02% differential gain and 0.02° differential phase to both NTSC and PAL standards.

NOISE FIGURE

For RF applications, Noise Figure (NF) is often the preferred noise specification instead of Noise Spectral Density since it allows system noise performance to be more easily calculated. The OPA648's Noise Figure vs Source Resistance is shown in Figure 8.

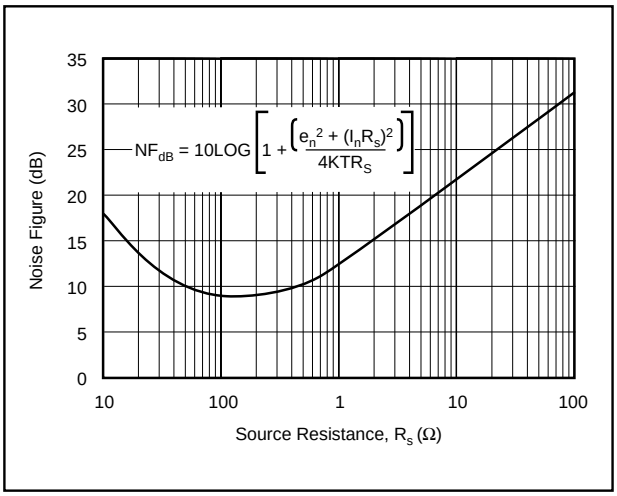


FIGURE 8. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE Macromodels using PSpice are available for the OPA648. Contract Burr-Brown applications departments to receive a SPICE Diskette.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X (LI-445) data sheet for details.

APPLICATIONS

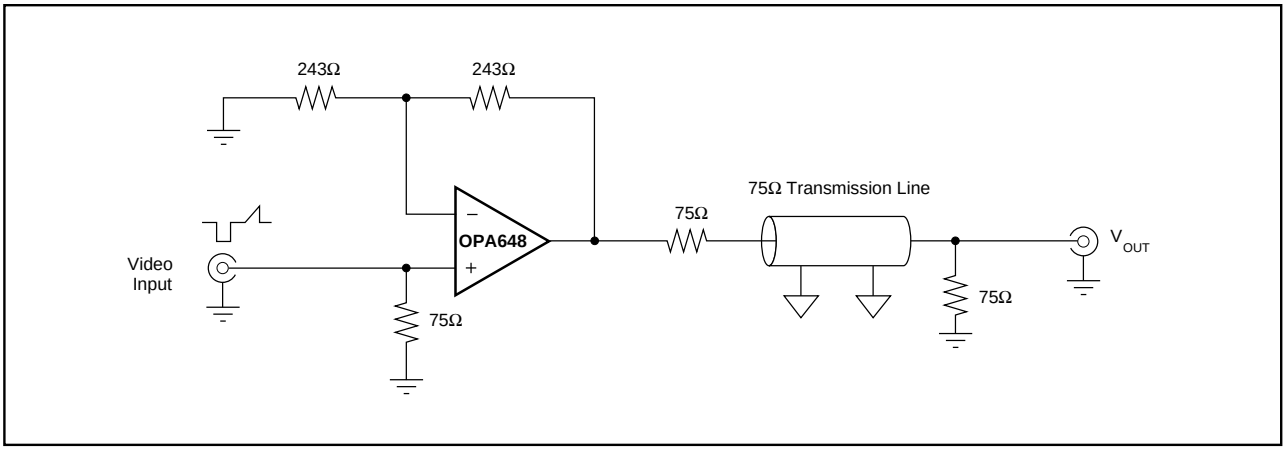
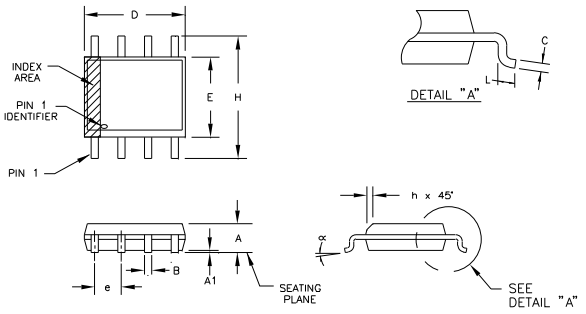


FIGURE 9. Low Distortion Video Amplifier.

PACKAGE DRAWINGS

Package Number 182 - 8-Lead SO-8 Surface Mount

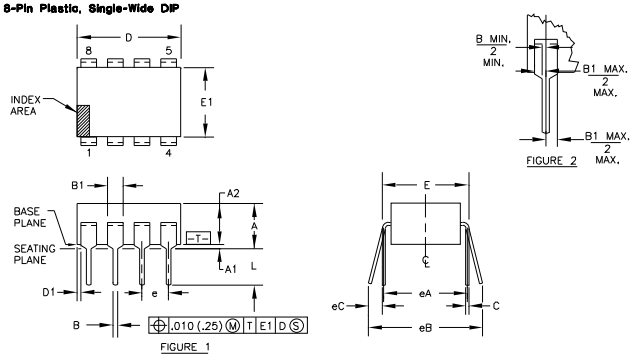


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.054	.068	1.37	1.73	
A1	.004	.009	0.10	0.23	
B	.014	.019	0.36	0.48	
C	.008	.0098	0.20	0.25	
D	.189	.196	4.80	4.98	
E	.150	.157	3.81	3.99	
e	.050 BASIC		1.27 BASIC		
H	.229	.244	5.82	6.20	
h	.010	.019	0.25	0.48	
L	.016	.050	0.41	1.27	
N	8		8		
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.086 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 | REV.: F
JEDEC NUMBER: MS-012

Package Number 006 - 8-Pin Plastic, Single-Wide DIP

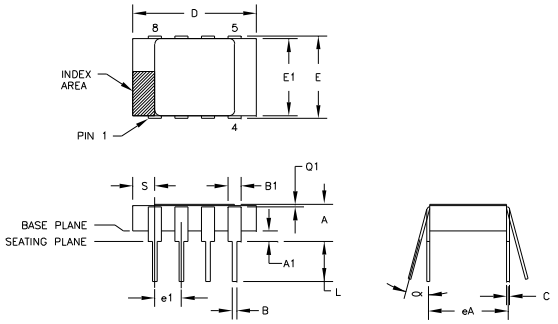


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
B	.014	.022	0.36	0.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	0.20	0.38	
D	.348	.430	8.84	10.92	4
D1	.005	--	0.13	--	
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
L	.115	.160	2.92	4.06	3
N	8		8		7

NOTES:
1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 4, 5, AND 8) MAY BE CONFIGURED AS SHOWN IN FIGURE 2.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 | REV.: D
JEDEC NUMBER: MS-001

Package Number 157 - 8-Pin Ceramic, Side-Braze DIP



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45	
A1	.025	.055	0.64	1.40	
B	.015	.021	0.38	0.53	
B1	.038	.060	0.97	1.52	
C	.008	.012	0.20	0.30	
D	.380	.550	9.65	13.97	
E	.290	.325	7.37	8.26	
E1	.280	.310	7.11	7.87	6
e1	.100 TYP.		2.54 TYP.		2
eA	.300 TYP.		7.62 TYP.		2
L	.125	.175	3.18	4.45	
N	8		8		4
Q1	.010	--	2.54	--	
S	.030	.120	0.76	3.05	
α	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .13mm (.005) RADIUS OF TRUE POSITION (TP) WITH MAXIMUM MATERIAL CONDITION.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE BASE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKAGE MATERIALS.
7. CONTROLLING DIMENSION: INCH.

PACKAGE NUMBER: ZZ157 | REV.: B
JEDEC NUMBER: MO-036