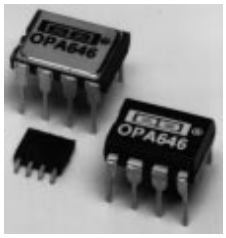
BURR-BROWN®



OPA646

Low Power, Wide Bandwidth OPERATIONAL AMPLIFIER

FEATURES

- LOW POWER: 55mW
- UNITY-GAIN BANDWIDTH: 650MHz
- UNITY-GAIN STABLE
- FAST 12-BIT SETTLING: 15ns (0.01%)
- LOW INPUT BIAS CURRENT: 2μA
- LOW HARMONICS: –82dBc at 5MHz
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.025%/0.08°

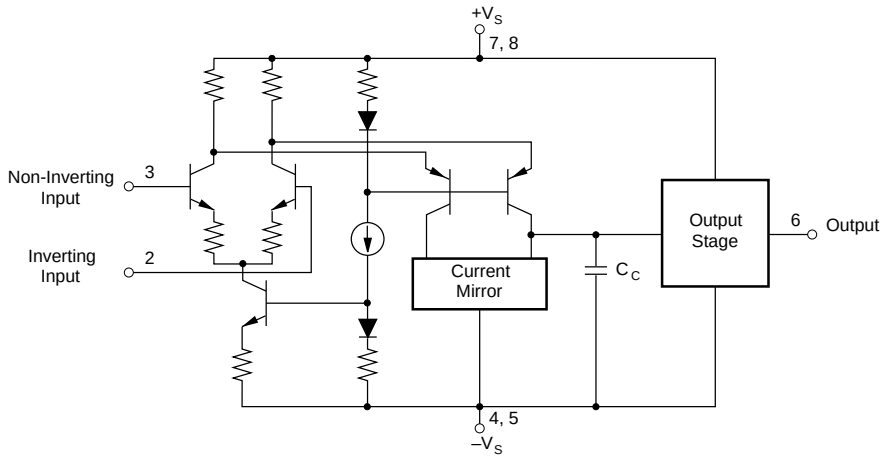
APPLICATIONS

- TELECOMMUNICATIONS
- MEDICAL IMAGING
- CCD IMAGING
- PORTABLE EQUIPMENT
- ACTIVE FILTERS
- VIDEO AMPLIFICATION
- ADC/DAC GAIN AMPLIFIER
- HIGH SPEED INTEGRATORS

DESCRIPTION

The OPA646 is a low power, wideband voltage feedback operational amplifier. It features a high bandwidth of 650MHz as well as a 12-bit settling time of only 15ns. Its low input bias current and wide bandwidth allows it to be used for high speed integrator and active filter designs. Its low distortion gives exceptional performance for telecommunications, medical imaging and video applications.

The OPA646 is internally compensated for unity-gain stability. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Its unusual combination of speed, accuracy and low power make it an ideal choice for many portable, multichannel and other high speed applications where power is at a premium.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA646H, P, U			OPA646HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			±3	±8		±1	±2.5	mV
Average Drift			±20			±12		µV/°C
HSQ Grade Over Temperature						±5	±8	mV
Power Supply Rejection (+V_S)	V_S = ±4.5 to ±5.5V	50	70		60	*		dB
(–V_S)		45	55		48	*		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		2	5		*	3.5	µA
Over Specified Temperature			3	7		*	*	µA
HSQ Grade Over Temperature						4	10	µA
Input Offset Current	V_{CM} = 0V		0.4	1.5		*	*	µA
Over Specified Temperature			0.9	3.0		*	*	µA
HSQ Grade Over Temperature						1.5	5.0	µA
NOISE								
Input Voltage Noise								
Noise Density: f = 100Hz			23.2			*		nV/√Hz
f = 10kHz			7.5			*		nV/√Hz
f = 1MHz			7.1			*		nV/√Hz
f = 1MHz to 100MHz			7.2			*		nV/√Hz
Voltage Noise, BW = 100Hz to 100MHz			141			*		µVrms
Input Bias Current Noise								
Current Noise Density, f = 0.1Hz to 20kHz			1.1			*		pA/√Hz
Noise Figure (NF)								
R_S = 10kΩ			3.0			*		dB
R_S = 50Ω			19.1			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.5	±3.0		*	*		V
Over Specified Temperature		±2.5	±3.0		*	*		V
Common-Mode Rejection	V_{CM} = ±0.5V	60	80		75	90		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		kΩ || pF
Common-Mode			1.6 || 1			*		MΩ || pF
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	45	51		47	55		dB
Over Specified Temperature		43	49		45	53		dB
FREQUENCY RESPONSE, R_{FB} = 402Ω	All Four Power Pins Used							
Closed-Loop Bandwidth	G = +1V/V		650			*		MHz
	G = +2V/V		160			*		MHz
	G = +5V/V		45			*		MHz
	G = +10V/V		22			*		MHz
Slew Rate[1]	G = +1, 2V Step		180			*		V/µs
At Minimum Specified Temperature			155			*		V/µs
Rise Time	1V Step		5.3			*		ns
Fall Time	1V Step		5.9			*		ns
Settling Time: 0.01%	G = +1, 2V Step		15			*		ns
0.1%	G = +1, 2V Step		11.5			*		ns
1%	G = +1, 2V Step		6			*		ns
Over-Voltage Recovery[2]			65					ns
Spurious Free Dynamic Range	G = +1, f = 5.0MHz		82			*		dBc
	V_O = 2Vp-p, R_L = 402Ω							
Differential Gain Error at 3.58MHz	G = +2V/V, V_O = 0 to 1.4V, R_L = 150Ω		0.025			*		%
Differential Phase Error at 3.58MHz	G = +2V/V, V_O = 0 to 1.4V, R_L = 150Ω		0.08			*		degrees
Gain Flatness to 0.1dB			100			*		MHz
OUTPUT								
Voltage Output	No Load							
Over Specified Temperature		±2.5	±2.75		*	*		V
HSQ Grade Over Temperature					±2.3	±2.5		V
Voltage Output	R_L = 250Ω							V
Over Specified Temperature		±2.5	±2.7		*	*		V
HSQ Grade Over Temperature					±2.0	±2.5		V
Voltage Output	R_L = 100Ω							
Over Specified Temperature		±2.0	±2.5		*	*		V
HSQ Grade Over Temperature					±2.0	±2.3		V
Current Output, +25°C to max Temp		±40	±52		*	*		mA
Over Specified Temperature		±30	±48		*	*		mA
HSQ Grade Over Temperature					±25	±35		mA
Short Circuit Current			60			*		mA
Output Resistance	1MHz, G = +1V/V		0.2			*		Ω

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

PARAMETER	CONDITIONS	OPA646H, P, U			OPA646HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	*		*	V
Quiescent Current			±5.25	±6.5		*	*	mA
Over Specified Temperature			±6.5	±7.5		*	*	mA
HSQ Grade Over Temperature						±7.5	±8.5	mA
TEMPERATURE RANGE								
Specification: H, P, PB, U, UB	Ambient	–40		+85	*		*	°C
HSQ	Ambient				–55		+125	°C
Thermal Resistance	θ_{JA}, Junction to Ambient							
P			120			*		°C/W
U			170			*		°C/W
H			120			*		°C/W

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step. (2) Recovery time to linear operation after a 50% overload recovery.

ORDERING INFORMATION

OPA646 ( ) ( )

Basic Model Number

Package Code
- H = 8-pin Sidebraze DIP
- P = 8-pin Plastic DIP
- U = 8-pin Plastic SOIC

Performance Grade Code
- SQ = –55°C to +125°C, Reliability Screened
- B(1) or No Letter = –40°C to +85°C

NOTE: (1) The "B" grade of the SOIC package will be marked with a "B" by Pin 8. Refer to the mechanical section for the location.

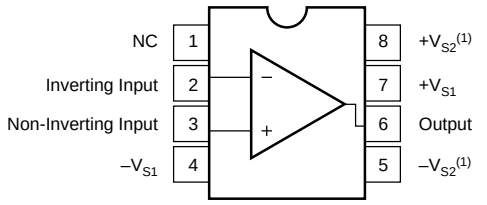
ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation(1)	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	–65°C to +150°C
P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PIN CONFIGURATION

Top View **DIP/SOIC**



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA646H, HSQ	8-Pin Cerdip	157
OPA646P, PB	8-Pin DIP	006
OPA646U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

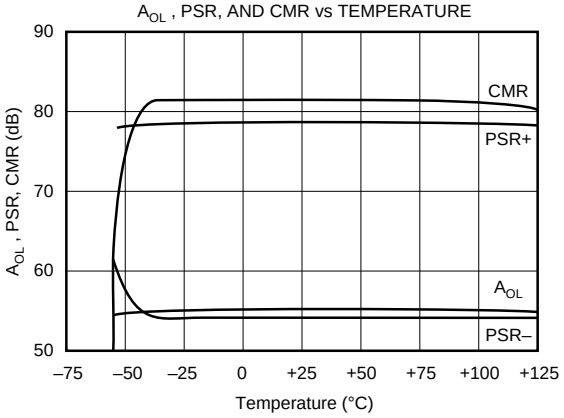
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

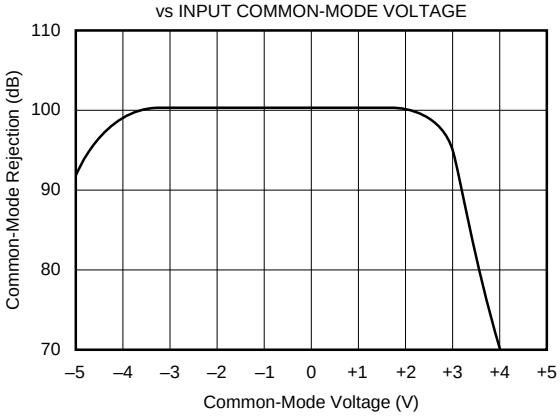
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

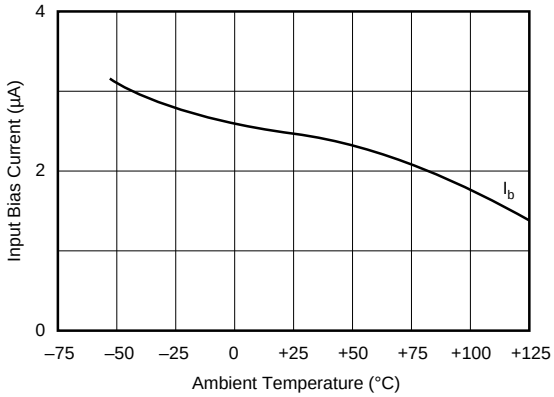
A_{OL} , PSR, AND CMR vs TEMPERATURE



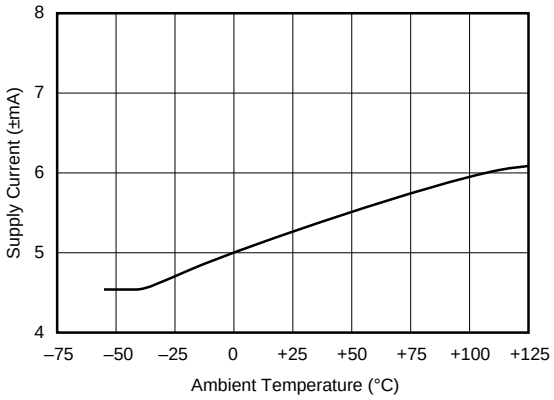
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



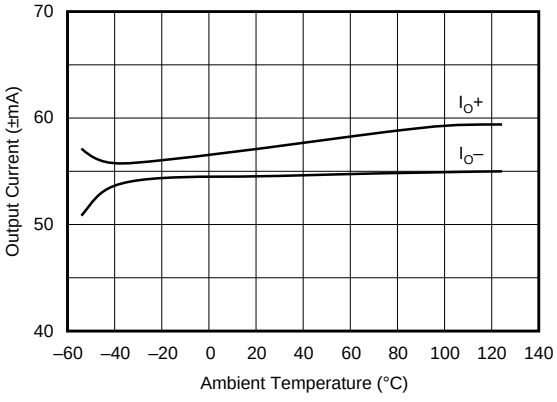
INPUT BIAS CURRENT vs TEMPERATURE



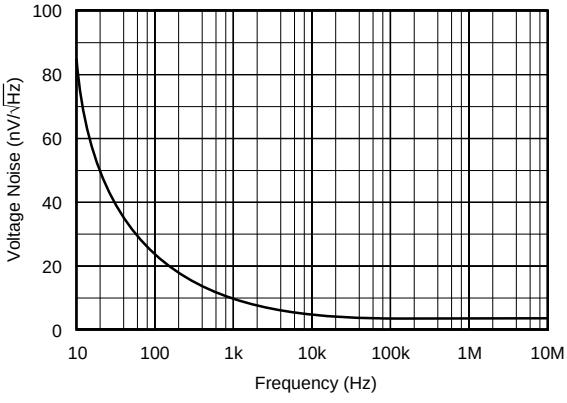
SUPPLY CURRENT vs TEMPERATURE



OUTPUT CURRENT vs TEMPERATURE



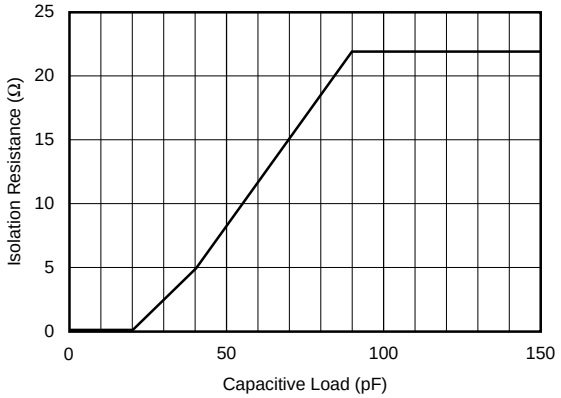
VOLTAGE NOISE vs FREQUENCY



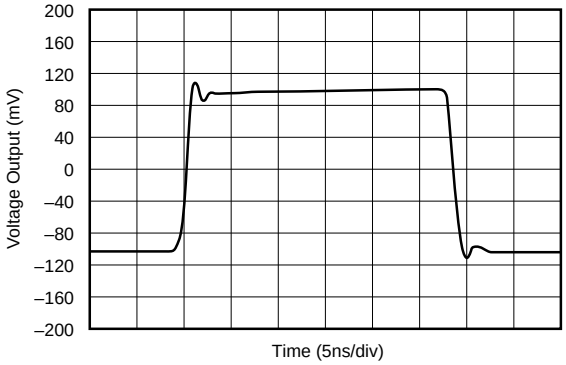
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

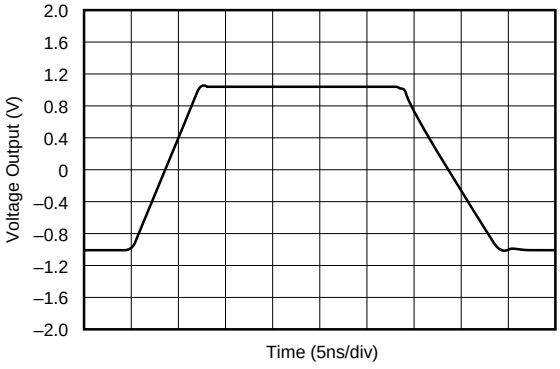
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



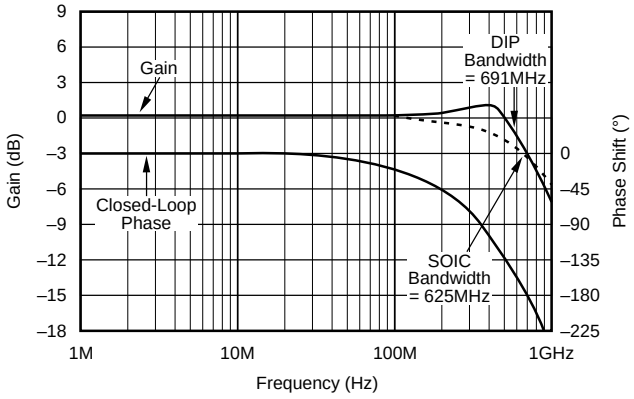
SMALL SIGNAL TRANSIENT RESPONSE (G = +1, R_L = 100Ω)



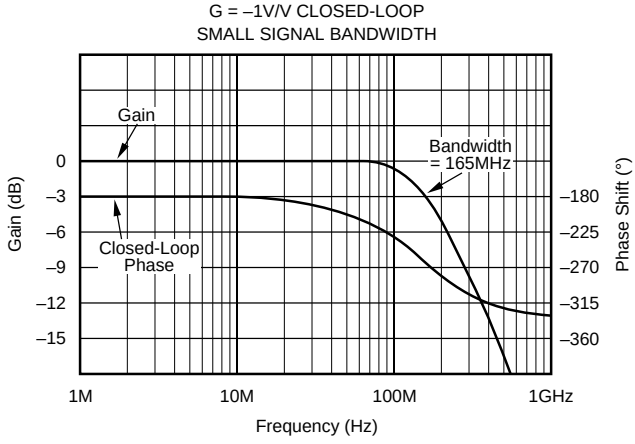
LARGE SIGNAL TRANSIENT RESPONSE (G = +1, R_L = 100Ω)



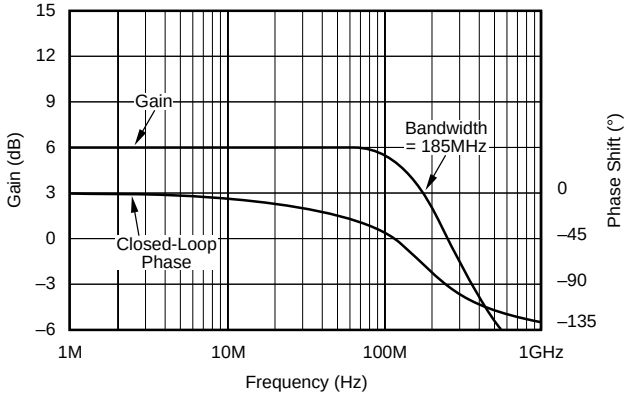
G = +1 CLOSED-LOOP SMALL SIGNAL BANDWIDTH



G = –1V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



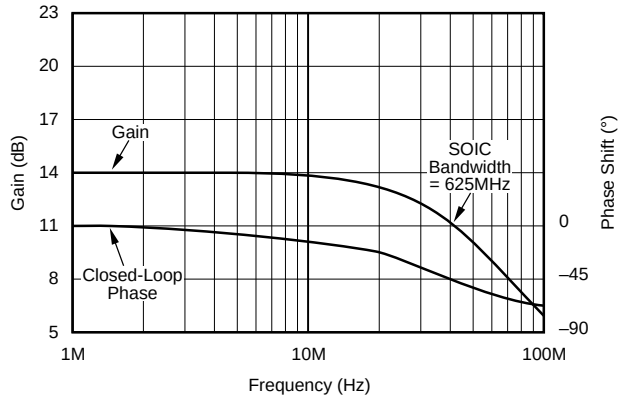
G = +2 CLOSED-LOOP SMALL SIGNAL BANDWIDTH



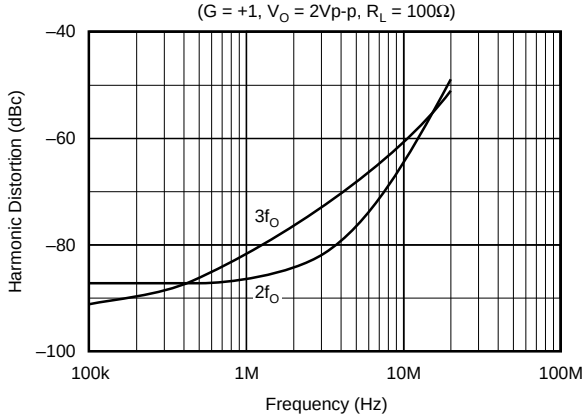
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

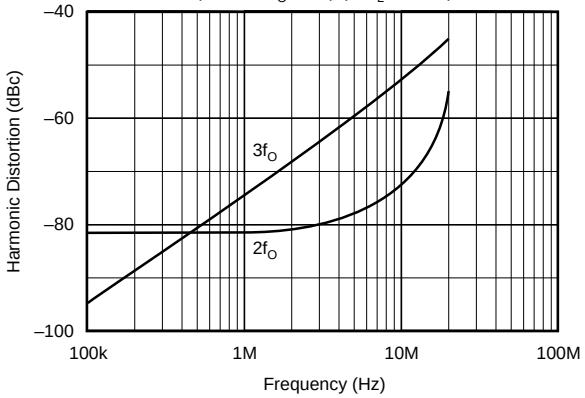
G = +5 CLOSED-LOOP
SMALL SIGNAL BANDWIDTH



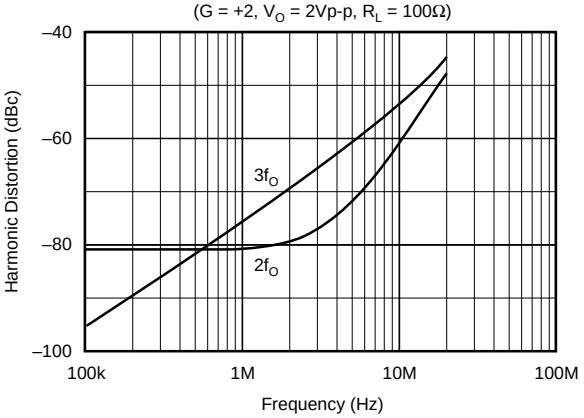
HARMONIC DISTORTION vs FREQUENCY
(G = +1, V_O = 2Vp-p, R_L = 100Ω)



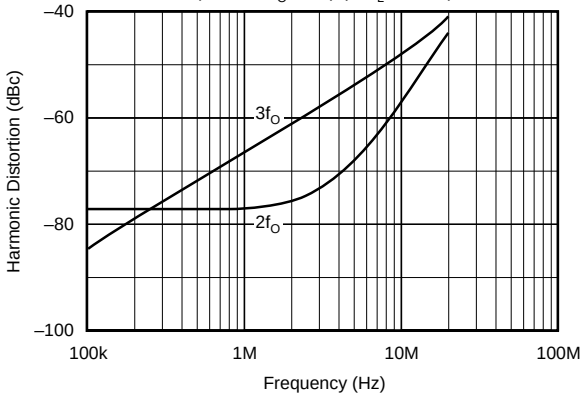
HARMONIC DISTORTION vs FREQUENCY
(G = –1, V_O = 2Vp-p, R_L = 100Ω)



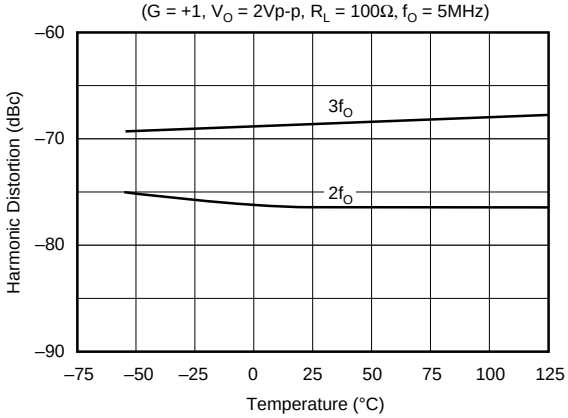
HARMONIC DISTORTION vs FREQUENCY
(G = +2, V_O = 2Vp-p, R_L = 100Ω)



HARMONIC DISTORTION vs FREQUENCY
(G = +5, V_O = 2Vp-p, R_L = 100Ω)



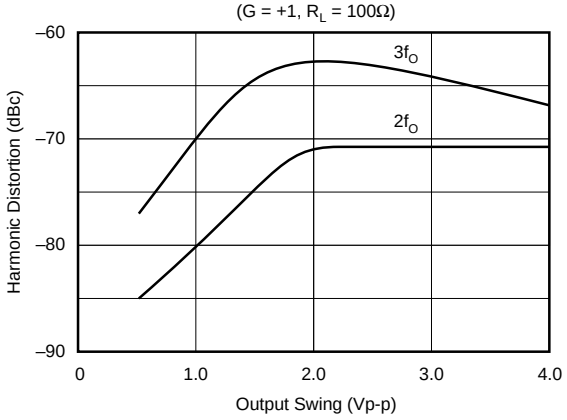
HARMONIC DISTORTION vs TEMPERATURE
(G = +1, V_O = 2Vp-p, R_L = 100Ω, f_O = 5MHz)



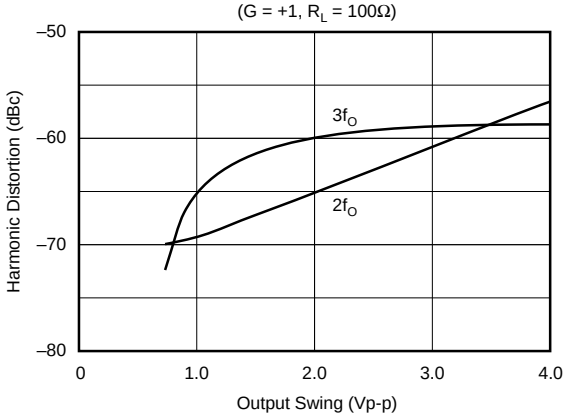
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω and all four power supply pins are used unless otherwise noted. R_{FB} = 25Ω for a gain of +1.

5MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = +1, R_L = 100Ω)



10MHz HARMONIC DISTORTION vs OUTPUT SWING
(G = +1, R_L = 100Ω)



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA646 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA646's design uses a "classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e., one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Cancelling offset errors (due to input bias currents) through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA646's "classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA646.

WIRING PRECAUTIONS

Maximizing the OPA646's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA646, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.01µF ceramic must also be added. Surface-mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to

isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance **including lower distortion.** The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface-mount capacitors on the topside of the PC Board is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the DEM-OPA64X Data Sheet for the recommended layout and component placements.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on backside of PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA646 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. Refer to the demonstration board layout at the end of the datasheet. **A longer feedback path than this will decrease the realized bandwidth substantially**.

6) Surface-mount components (chip resistors, capacitors, etc.) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA646U (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

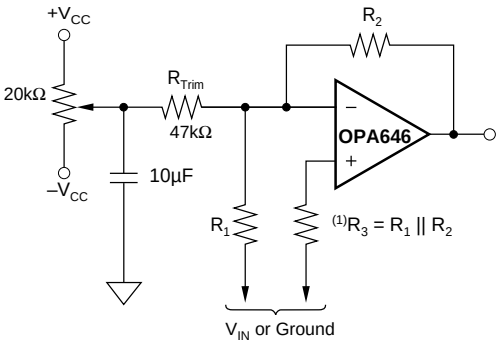
9) Standard commercial test equipment has not been designed to test devices in the OPA646's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.



NOTE: (1) R_3 is optional and can be used to cancel offset errors due to input bias currents.

FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection

from this potentially damaging source. The OPA646 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA646 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

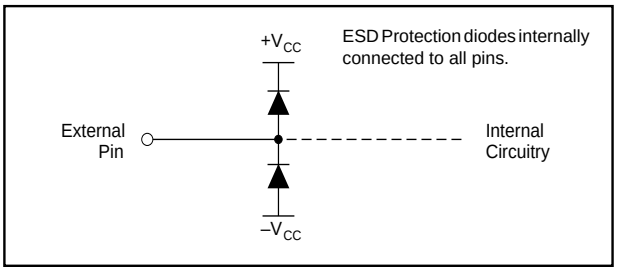


FIGURE 2. Internal ESD Protection.

The OPA646 utilizes a fine geometry high speed process that withstands 500V using the Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA646.

OUTPUT DRIVE CAPABILITY

The OPA646 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA646 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA646 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

THERMAL CONSIDERATIONS

The OPA646 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 7.5mA = 75mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max = $(\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

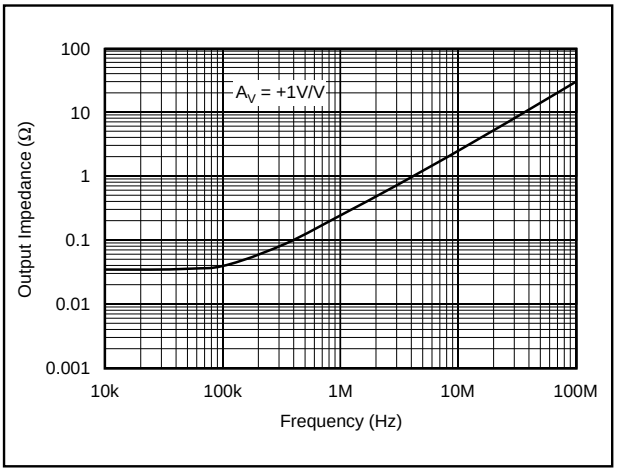


FIGURE 3. Small-Signal Output Impedance vs Frequency.

A short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in Figure 4.

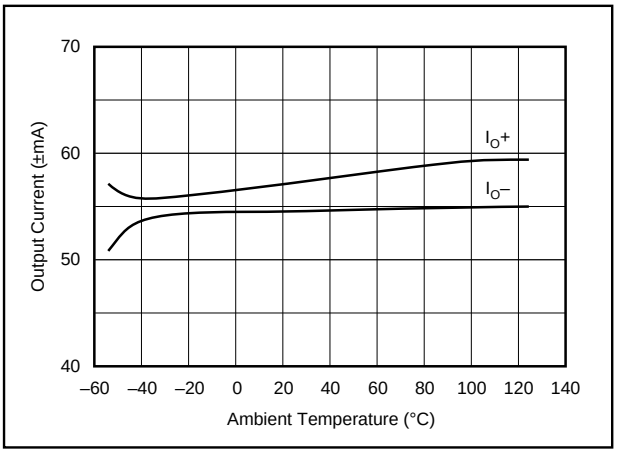


FIGURE 4. Output Current vs Temperature.

CAPACITIVE LOADS

The OPA646's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 10pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 5. This is particularly important when driving high capacitance loads such as flash A/D converters. Increasing the gain from +1 will improve the capacitive load drive due to increased phase margin.

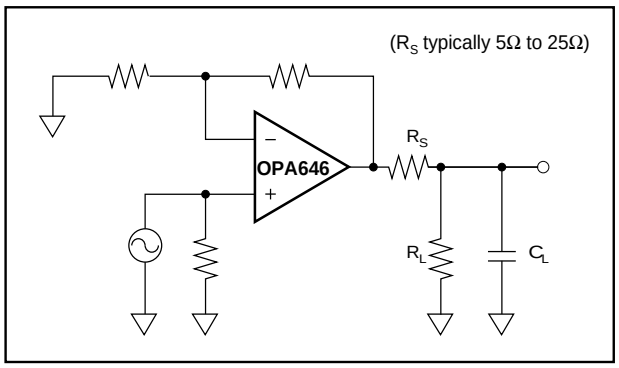


FIGURE 5. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA646 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA646 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 15ns to 0.01% for a 2V step, making the OPA646 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 65ns.

In practice, settling time measurements on the OPA646 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION

The OPA646's harmonic distortion characteristics into a 100Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be significantly improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

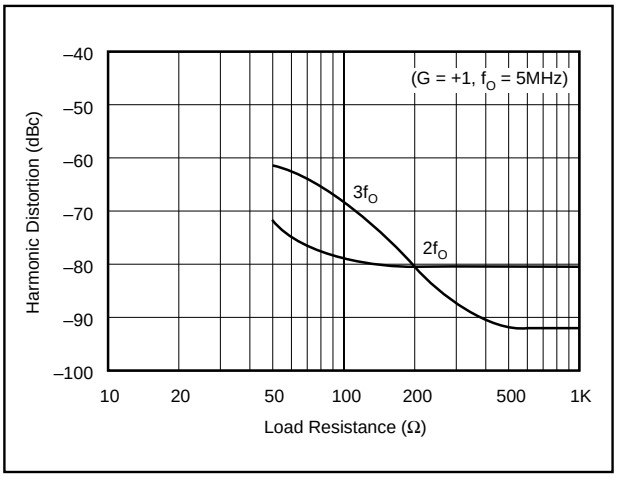


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance with R_F = 402Ω.

NOISE FIGURE

The OPA646 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA646's Noise Figure vs Source Resistance is shown in Figure 7.

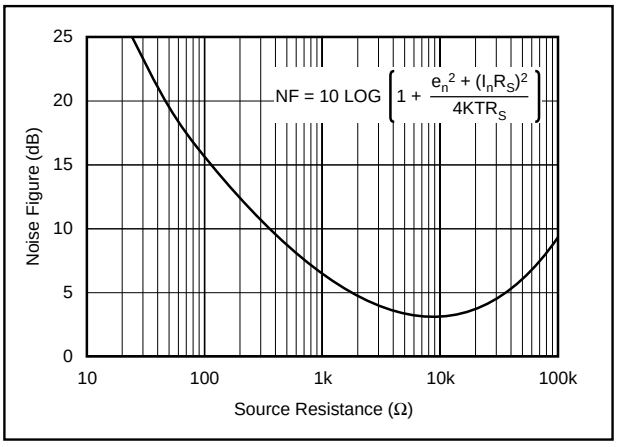


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA646. Contact Burr-Brown Applications Department to receive a spice diskette.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device —it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" on the HSQ grade provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = –65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20000G
Hermetic Seal	Fine: He leak rate < 5 x 10^{-8} atm cc/s, 30PSiG Gross: per Fluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on the HS package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X Data Sheet for details.

APPLICATIONS

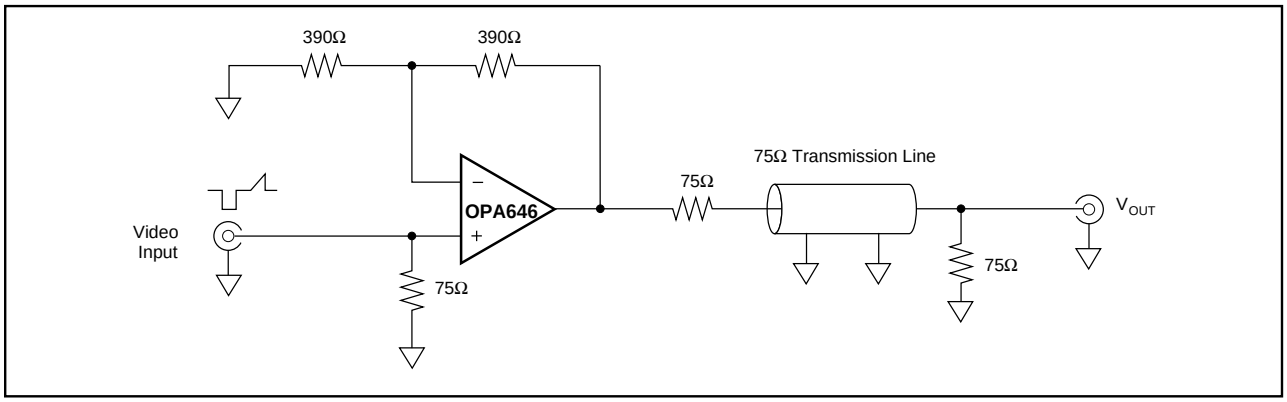


FIGURE 8. Low Power Video Amplifier.

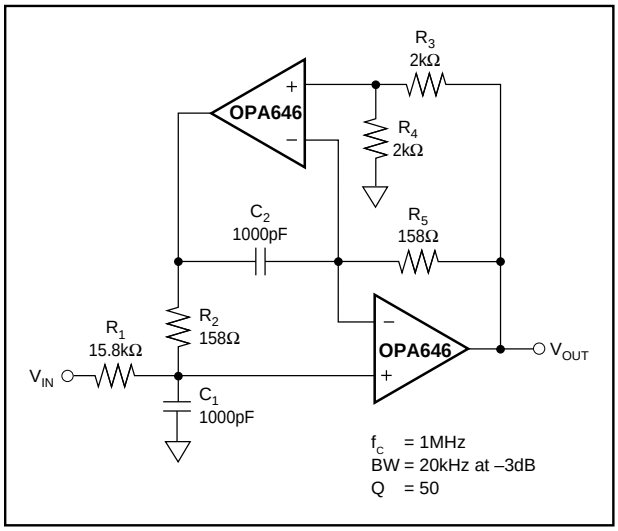


FIGURE 9. High-Q 1MHz Bandpass Filter.

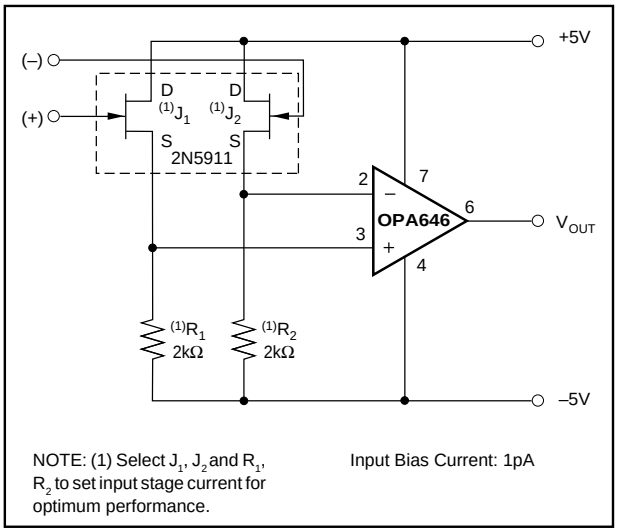


FIGURE 10. Low Power, Wideband FET Input Op Amp.

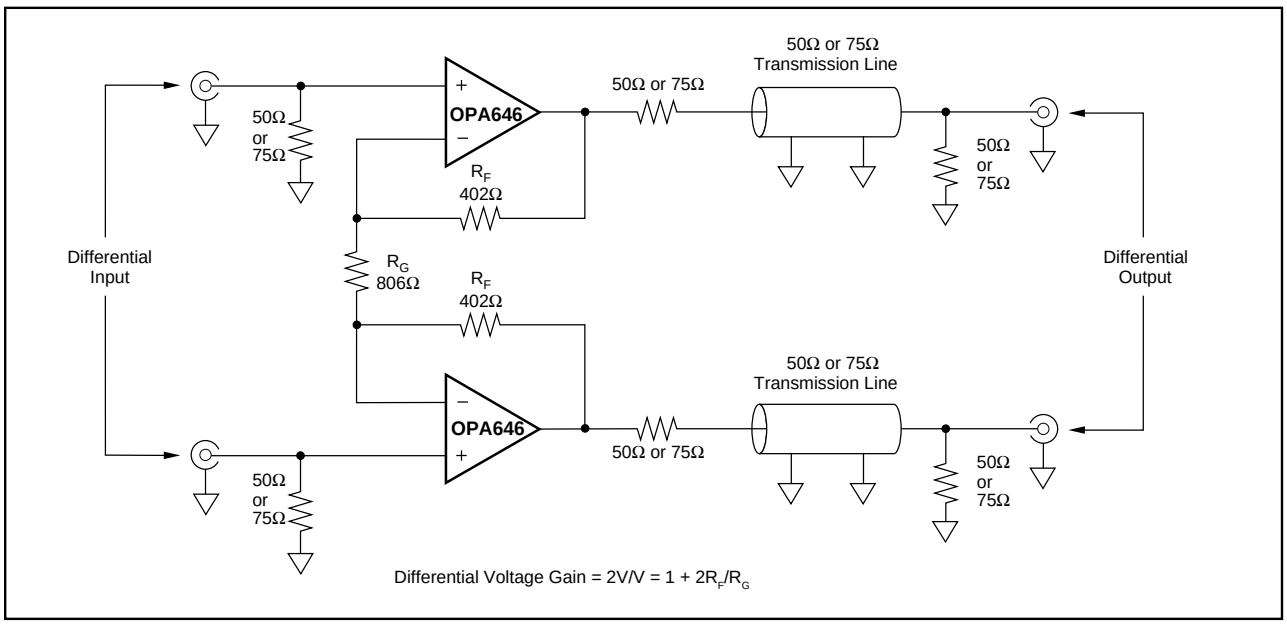


FIGURE 11. Differential Line Driver for 50Ω or 75Ω Systems.

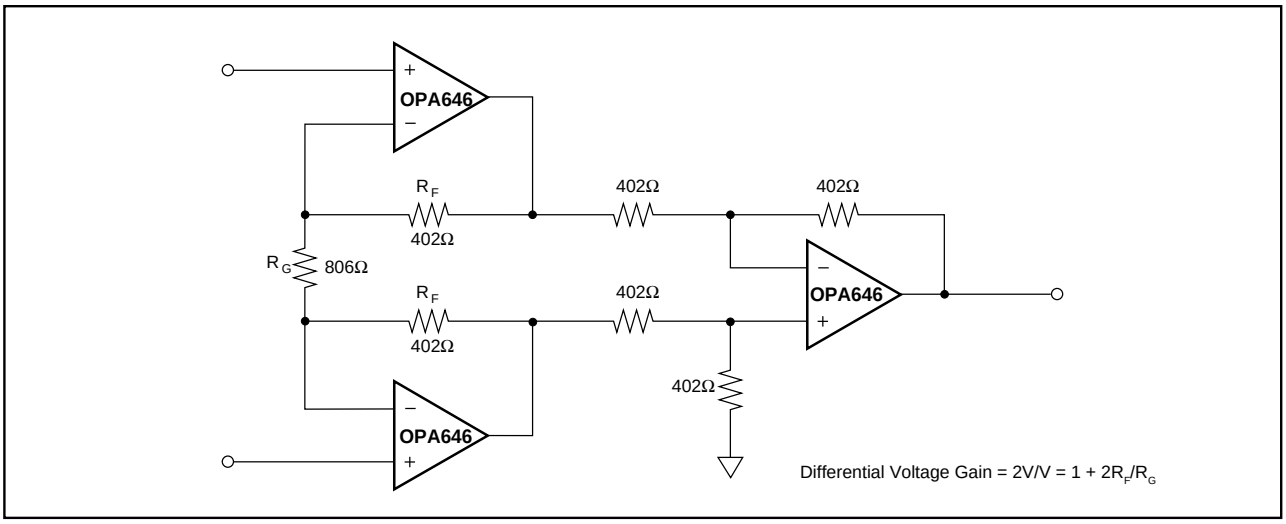


FIGURE 12. Wideband, Fast-Settling Instrumentation Amplifier.

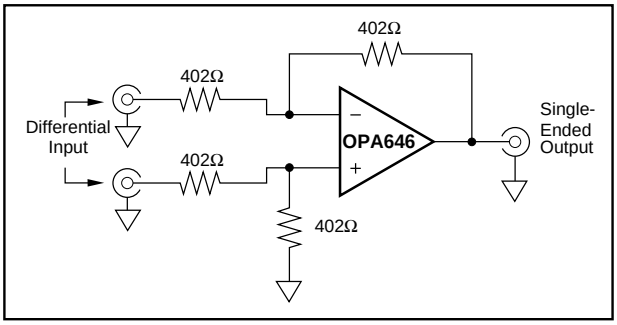


FIGURE 13. Unity Gain Difference Amplifier.

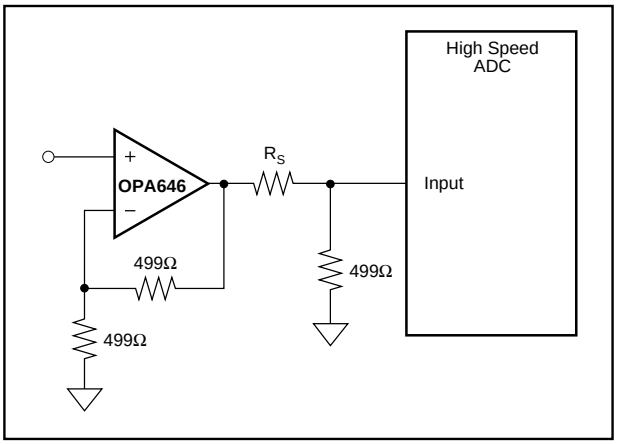


FIGURE 14. Differential Input Buffer Amplifier (G = +2V/V).

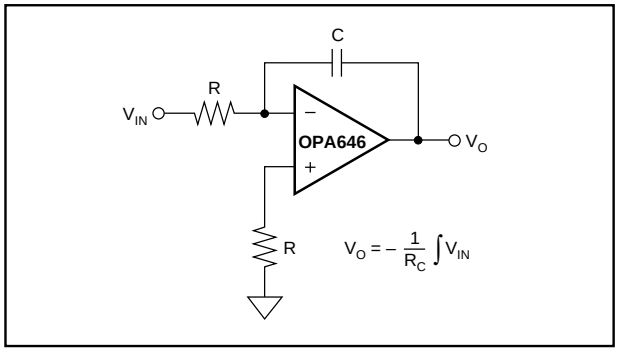


FIGURE 15. A High Speed Integrator.

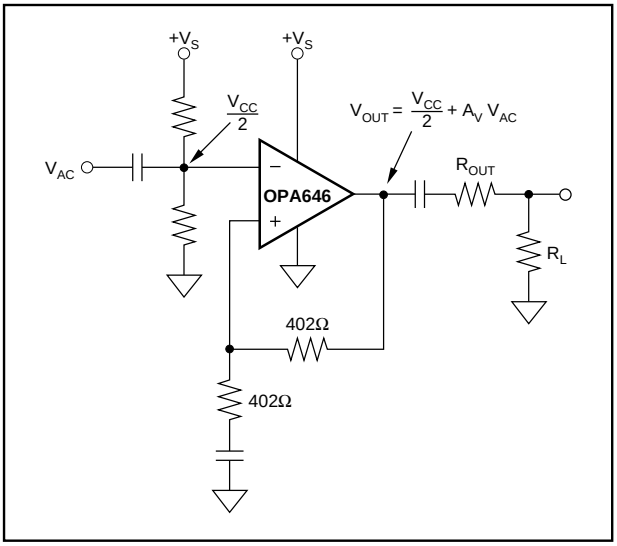
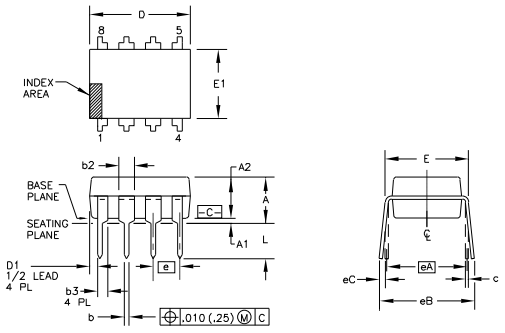


FIGURE 16. Single Supply Operation.

PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



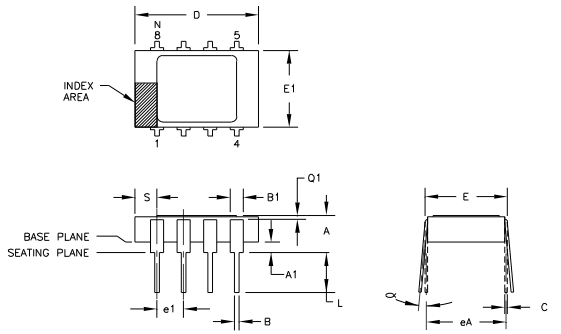
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.63	BASIC	5
eB	--	.430	--	10.92	6

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006	REV.: E
JEDEC NUMBER: MS-001-BA	

Package Number 157 - 8-Lead, Ceramic Side Braze DIP, .300 Wide



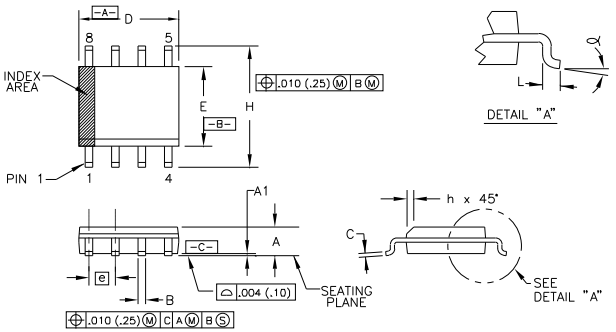
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45	
A1	.025	.055	0.64	1.40	
B	.015	.021	0.38	0.53	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	
D	.380	.550	9.65	13.97	
E	.290	.325	7.37	8.26	
E1	.280	.310	7.11	7.87	6
e1	.100	TYP.	2.54	TYP.	2
eA	.300	TYP.	7.62	TYP.	2
L	.125	.175	3.18	4.45	
N	8		8		4
Q1	.010	--	2.54	--	
S	.030	.120	0.76	3.05	

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
∝	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .005 IN. (0.13mm) RADIUS OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.
7. CONTROLLING DIMENSION: INCH.
8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: ZZ157	REV.: C
JEDEC NUMBER: MO-36-AA	

Package Number 182 - 8-Lead SOIC



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050	BASIC	1.27	BASIC	
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	
L	.016	.050	0.41	1.27	5
N	8		8		6
∝	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182	REV.: G
JEDEC NUMBER: MS-012-AA	