BURR - BROWN®

OPA641

Wideband Voltage Feedback OPERATIONAL AMPLIFIER

FEATURES

- GAIN-BANDWIDTH: 1.6GHz
- STABLE IN GAINS ≥ 2
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.015%/0.006°
- HIGH SLEW RATE: 650V/μs
- FAST 12-BIT SETTLING: 18ns (0.01%)
- HIGH COMMON-MODE REJECTION: 80dB
- LOW HARMONICS: –72dBc at 10MHz

APPLICATIONS

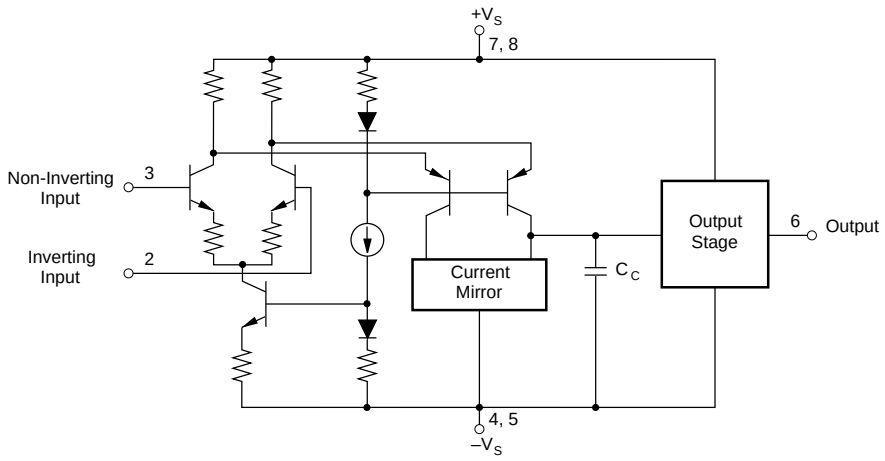
- COMMUNICATIONS
- MEDICAL IMAGING
- TEST EQUIPMENT
- CCD IMAGING
- ADC/DAC GAIN AMPLIFIER
- HIGH-RESOLUTION VIDEO
- LOW NOISE PREAMPLIFIER
- ACTIVE FILTERS

DESCRIPTION

The OPA641 is an extremely wideband operational amplifier featuring low noise, high slew rate and high spurious free dynamic range.

The OPA641 is conservatively compensated for stability in gains of 2 or greater. This amplifier has a fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. This allows the OPA641 to be used in all op amp applications requiring high speed and precision.

Low noise, wide bandwidth, and high linearity make this amplifier suitable for a variety of RF, video, and imaging applications.



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Printed in U.S.A. July, 1994

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, and all four power supply pins are used unless otherwise noted.

PARAMETER	CONDITIONS	OPA641H, P, U			OPA641HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE								
Input Offset Voltage			±2	±6		±1	±2	mV
Average Drift			±10			±6		µV/°C
HSQ Grade Over Temperature						±3	±6	mV
Power Supply Rejection (+V_S)	V_S = ±4.5 to ±5.5V	56	79		61	82		dB
(–V_S)		51	58		54	60		dB
INPUT BIAS CURRENT								
Input Bias Current	V_{CM} = 0V		13	30		*	*	µA
Over Specified Temperature			20	90		*	*	µA
HSQ Grade Over Temperature						30	75	µA
Input Offset Current	V_{CM} = 0V		0.2	2		*	1.0	µA
Over Specified Temperature			0.5	2.5		*	2.0	µA
HSQ Grade Over Temperature						1.2	4.0	µA
NOISE								
Input Voltage Noise								
Noise Density, f = 100Hz			8.0			*		nV/√Hz
f = 10kHz			2.9			*		nV/√Hz
f = 1MHz			2.8			*		nV/√Hz
f = 1MHz to 500MHz			2.8			*		nV/√Hz
Voltage Noise, BW = 100Hz to 500MHz			63			*		µVrms
Input Bias Current Noise Density								
f = 0.1Hz to 20kHz			2.0			*		pA/√Hz
Noise Figure (NF)								
R_S = 1kΩ			4			*		dB
R_S = 50Ω			13			*		dB
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±2.5	±2.85		*	*		V
Over Specified Temperature		±2.5	±2.75		*	*		V
Common-Mode Rejection	V_{CM} = ±0.5V	56	78		65	80		dB
INPUT IMPEDANCE								
Differential			15 || 1			*		kΩ || pF
Common-Mode			2 || 1			*		MΩ || pF
OPEN-LOOP GAIN, DC								
Open-Loop Voltage Gain	V_O = ±2V, R_L = 100Ω	50	58		53	61		dB
Over Specified Temperature	V_O = ±2V, R_L = 100Ω	45	56		48	*		dB
FREQUENCY RESPONSE, R_{FB} = 402Ω	All Four Power Pins Used							
Closed-Loop Bandwidth								
	Gain = +2V/V		800			*		MHz
	Gain = +5V/V		78			*		MHz
	Gain = +10V/V		39			*		MHz
Slew Rate[1]	G = +2, 2V Step		650			*		V/µs
At Minimum Specified Temperature	G = +2, 2V Step		550			*		V/µs
Settling Time: 0.01%	G = +2, 2V Step		18			*		ns
0.1%	G = +2, 2V Step		13			*		ns
1%	G = +2, 2V Step		5			*		ns
Differential Gain at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.015			*		%
Differential Phase at 3.58MHz, G = +2V/V	V_O = 0V to 1.4V, R_L = 150Ω		0.006			*		degrees
Gain Flatness	G = +2		0.1			*		MHz
Spurious Free Dynamic Range	G = +2, f = 5MHz, V_O = 2Vp-p		78			*		dBc
	G = +2, f = 10MHz, V_O = 2Vp-p		72			*		dBc
OUTPUT								
Voltage Output	No Load							
Over Specified Temperature		±2.6	±3.0		*	*		V
HSQ Grade Over Temperature					±2.5	±2.8		V
Voltage Output	R_L = 100Ω							
Over Specified Temperature		±2.25	±2.5		*	*		V
HSQ Grade Over Temperature		±2.0	±2.3					
Current Output		±40	±55		*	*		mA
Over Specified Temperature		±25	±50		*	*		mA
HSQ Grade Over Temperature					±25	±50		mA
Short Circuit Current			75					mA
Output Resistance	1MHz, G = +2V/V		0.04			*		Ω

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, and all four power supply pins are used unless otherwise noted.

PARAMETER	CONDITIONS	OPA641H, P, U			OPA641HSQ, PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
Specified Operating Voltage	T_{MIN} to T_{MAX}		±5			*		V
Operating Voltage Range	T_{MIN} to T_{MAX}	±4.5		±5.5	*		*	V
Quiescent Current			±15	±22		*	*	mA
Over Specified Temperature			±19	±24		*	*	mA
TEMPERATURE RANGE								
Specification: H, P, PB, U, UB	Ambient	–40		+85	*		*	°C
HSQ	Ambient				–55		+125	°C
Thermal Resistance	θ_{JA}, Junction to Ambient							
P			120			*		°C/W
U			170			*		°C/W
H			120			*		°C/W

NOTE: (1) Slew rate is rate of change from 10% to 90% of output voltage step.

ORDERING INFORMATION

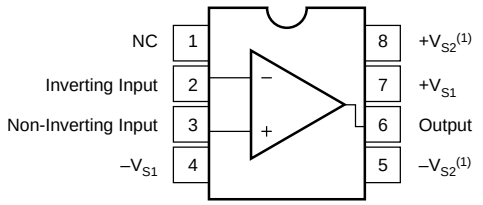
OPA641 ( ) ( ) (Q)

- Basic Model Number
- Package Code
  - H = 8-pin Sidebraze DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC
- Performance Grade Code
  - S = –55°C to +125°C
  - B[1] or No Letter = –40°C to +85°C
- Reliability Screening
  - Q = Q-Screened (HSQ Model Only)

NOTE: (1) The "B" grade of the SOIC package will be designated with a "B". Refer to the mechanical section for the location.

PIN CONFIGURATION

Top View **DIP/SOIC**



NOTE: (1) Making use of all four power supply pins is highly recommended, although not required. Using these four pins, instead of just pins 4 and 7, will lower the effective pin impedance and substantially lower distortion.

ABSOLUTE MAXIMUM RATINGS

Supply	±5.5VDC
Internal Power Dissipation[1]	See Applications Information
Differential Input Voltage	Total V_{CC}
Input Voltage Range	See Applications Information
Storage Temperature Range: H, HSQ	–65°C to +150°C
P, PB, U, UB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA641H, HSQ	8-Pin Cerdip	157
OPA641P, PB	8-Pin DIP	006
OPA641U, UB	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

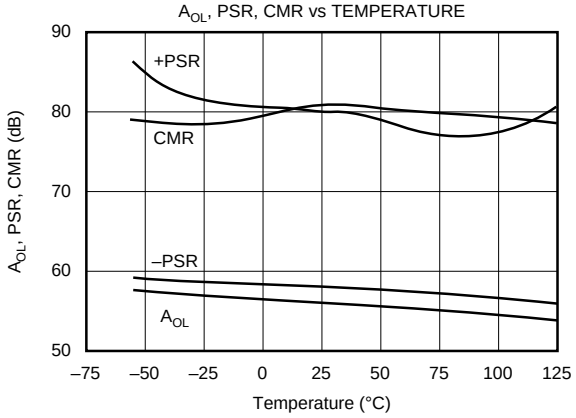
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

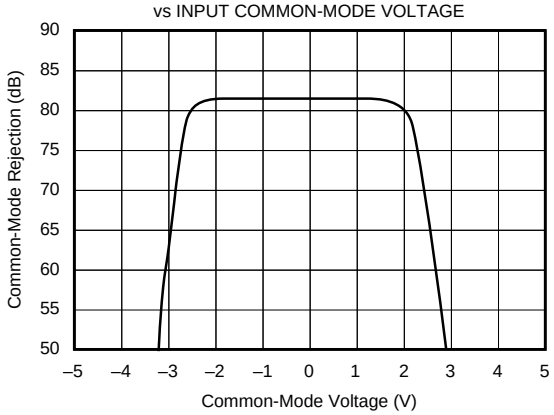
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, and all four power supply pins are used unless otherwise noted.

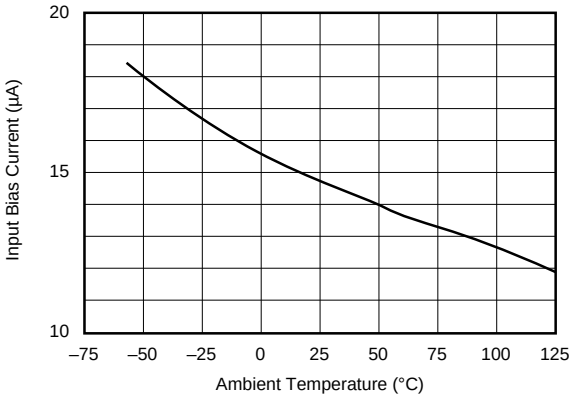
A_{OL}, PSR, CMR vs TEMPERATURE



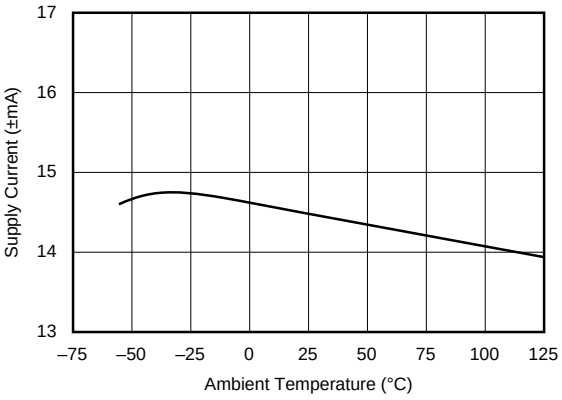
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



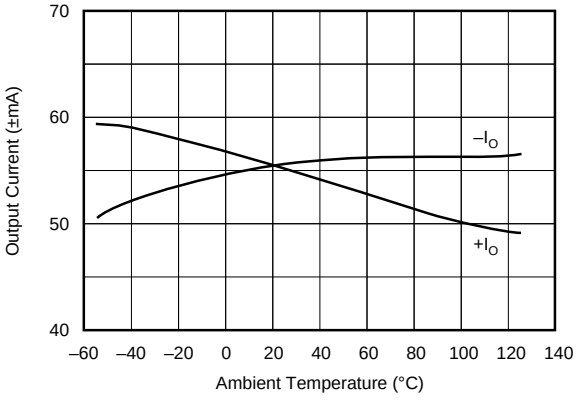
INPUT BIAS CURRENT vs TEMPERATURE



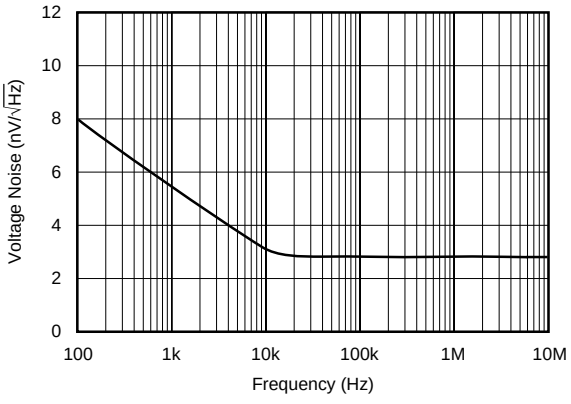
SUPPLY CURRENT vs TEMPERATURE



OUTPUT CURRENT vs TEMPERATURE



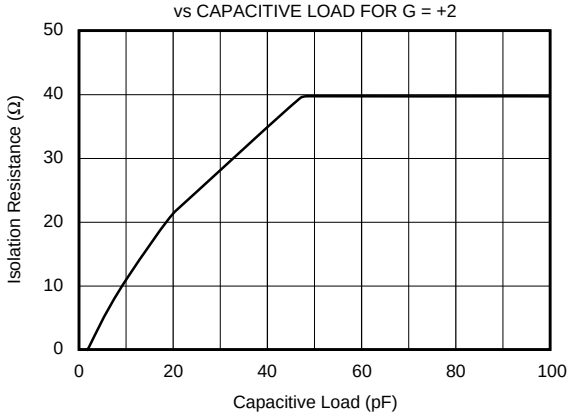
VOLTAGE NOISE vs FREQUENCY



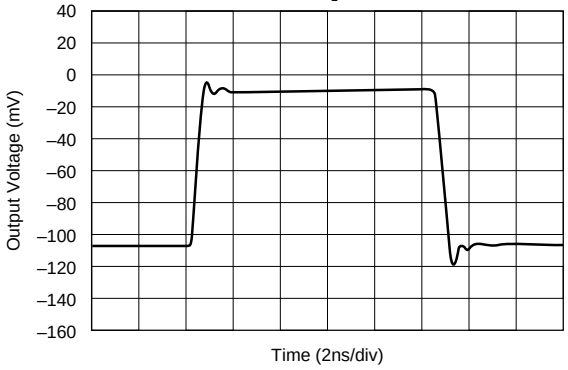
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, and all four power supply pins are used unless otherwise noted.

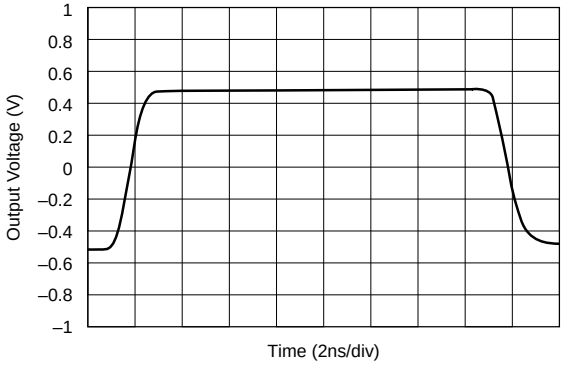
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD FOR G = +2



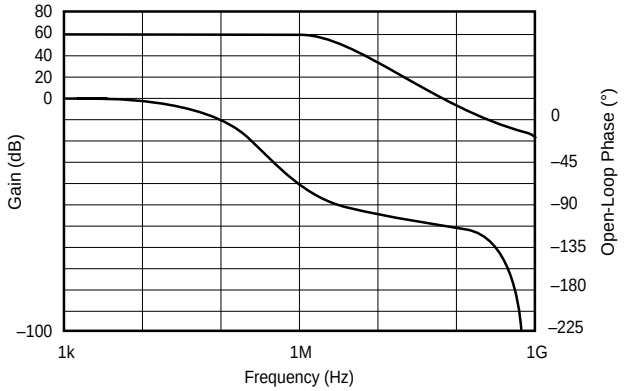
SMALL SIGNAL TRANSIENT RESPONSE (G = +2, R_L = 100Ω)



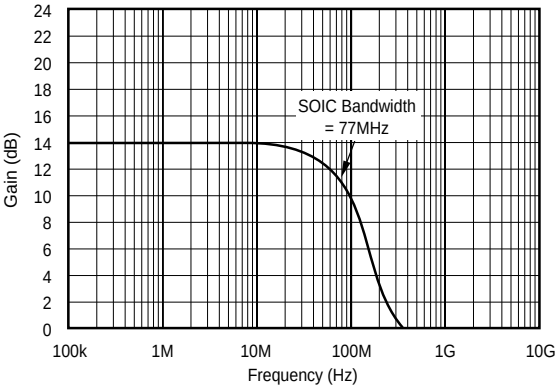
LARGE SIGNAL TRANSIENT RESPONSE (G = +2, R_L = 100Ω)



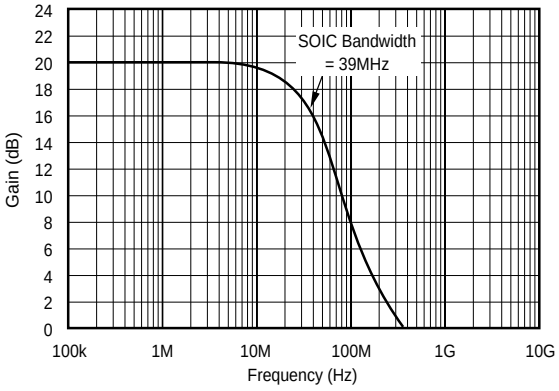
A_V = +2 OPEN-LOOP SMALL SIGNAL BANDWIDTH



G = +5 CLOSED-LOOP BANDWIDTH



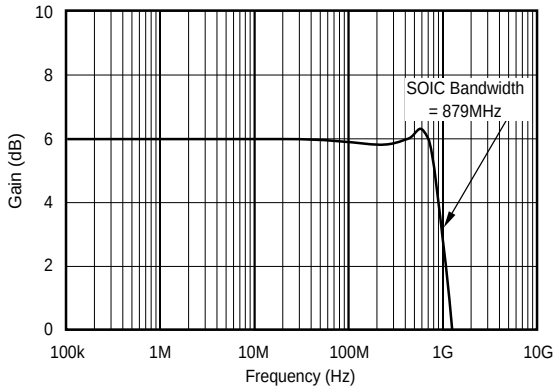
G = +10 CLOSED-LOOP BANDWIDTH



TYPICAL PERFORMANCE CURVES (CONT)

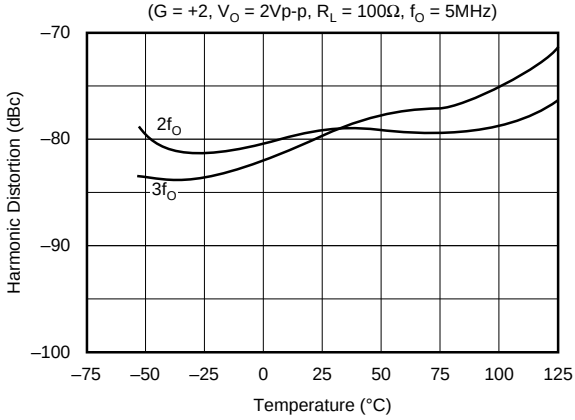
T_A = +25°C, V_S = ±5V, R_L = 100Ω, C_L = 2pF, R_{FB} = 402Ω, and all four power supply pins are used unless otherwise noted.

G = +2 CLOSED-LOOP BANDWIDTH

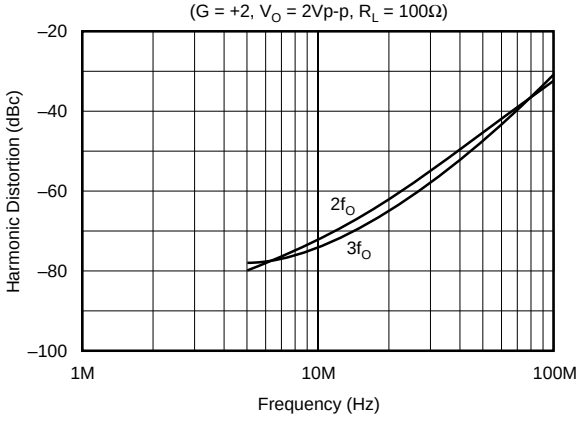


NOTE: Dip Bandwidth = 785MHz

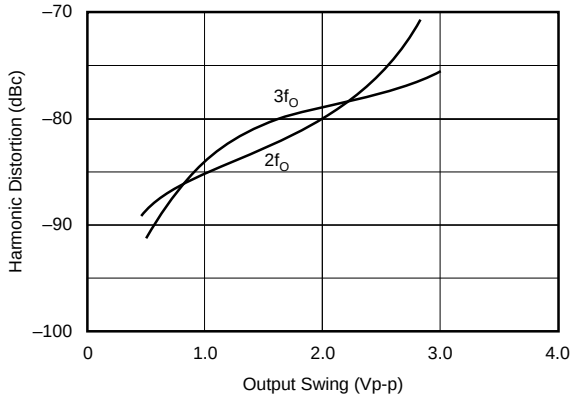
HARMONIC DISTORTION vs TEMPERATURE
(G = +2, V_O = 2Vp-p, R_L = 100Ω, f_O = 5MHz)



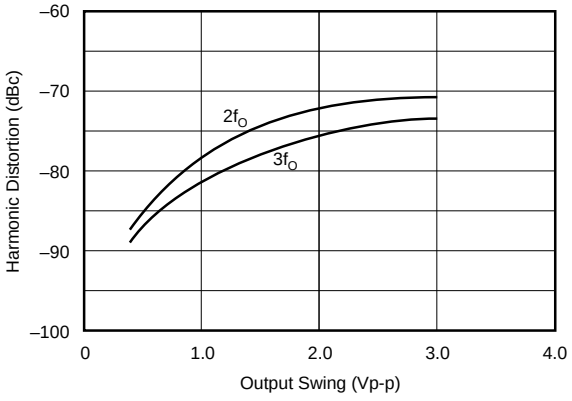
HARMONIC DISTORTION vs FREQUENCY
(G = +2, V_O = 2Vp-p, R_L = 100Ω)



5MHz HARMONIC DISTORTION vs OUTPUT SWING



10MHz HARMONIC DISTORTION vs OUTPUT SWING



APPLICATIONS INFORMATION

DISCUSSION OF PERFORMANCE

The OPA641 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA641's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer some disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e., one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA641's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA641.

WIRING PRECAUTIONS

Maximizing the OPA641's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA641, as it is with all high-frequency circuits. Oscillations at high frequencies can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (2.2µF) with very short leads are recommended. A parallel 0.01µF ceramic must also be added. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

Points to Remember

1) Making use of all four power supply pins will lower the effective power supply impedance seen by the input and output stages. This will improve the AC performance **including lower distortion**. The lowest distortion is achieved when running separated traces to V_{S1} and V_{S2}. Power supply bypassing with 0.01µF and 2.2µF surface mount capacitors on the topside of the PC board is recommended. It is essential to keep the 0.01µF capacitor very close to the power supply pins. Refer to the DEM-OPA64x Datasheet for the recommended layout and component placement.

2) Whenever possible, use surface mount. Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

3) Surface mount on the PC Board. Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

4) Whenever possible, solder the OPA641 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations.

5) Use a small feedback resistor (usually 25Ω) in unity-gain voltage follower applications for the best performance. For gain configurations, resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits. Feedback resistors should be placed directly between the output and the inverting input on the backside of the PC board. This placement allows for the shortest feedback path and the highest bandwidth. See the demonstration board layout at

the end of the datasheet. **A longer feedback path than this will decrease the realized bandwidth substantially.**

6) Due to the extremely high bandwidth of the OPA641, the SOIC package is strongly recommended due its low parasitic impedance. The parasitic impedance in the PDIP and CERDIP packages causes the OPA641 to experience about 5dB of gain peaking in unity-gain configurations. This is compared with virtually no gain peaking in the SOIC package in unity-gain. The gain peaking in the PDIP and CERDIP packages is minimized in gains of 4 or greater, however. Surface mount components (chip resistors, capacitors, etc.) also have low lead inductance and are therefore strongly recommended.

7) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

8) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

9) Standard commercial test equipment has not been designed to test devices in the OPA641's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

10) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

11) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

OFFSET VOLTAGE ADJUSTMENT

If additional offset adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce input bias current errors to the amplifier's offset current.

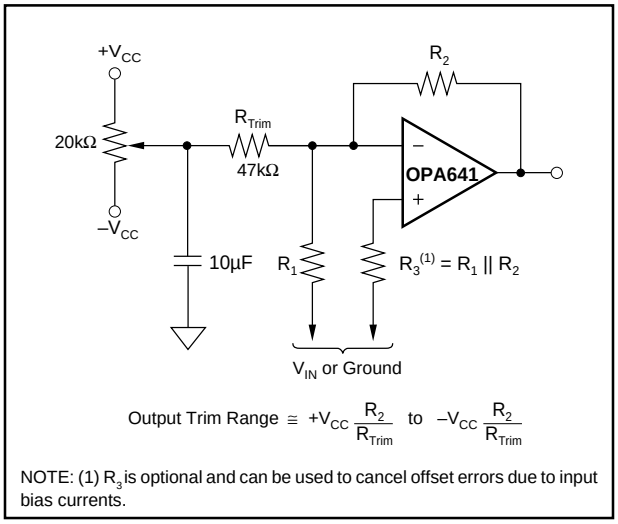


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA641 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA641 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

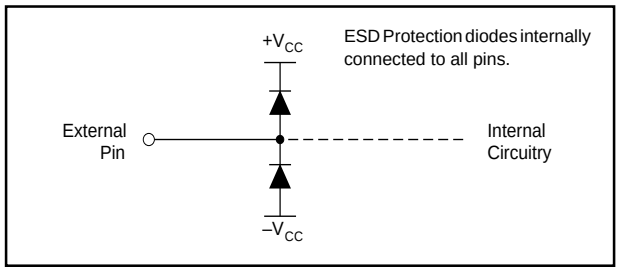


FIGURE 2. Internal ESD Protection.

The OPA641 utilizes a fine geometry high speed process that withstands 500V using Human Body Model and 100V using the Machine Model. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA641.

OUTPUT DRIVE CAPABILITY

The OPA641 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive 2Vp-p into a 75Ω load. This high-output drive capability makes the OPA641 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA641 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

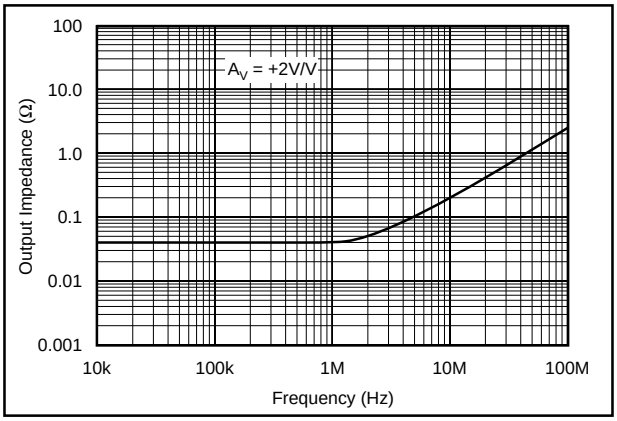


FIGURE 3. Small-Signal Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA641 does not require a heat sink for operation in most environments. At extreme temperatures and under full load conditions a heat sink may be necessary.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 24mA = 240mW$, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage ($\pm V_{OUT}$) the maximum value of P_{DL} occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to P_{DL}, max = $(\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

The short-circuit condition represents the maximum amount of internal power dissipation that can be generated. The variation of output current with temperature is shown in the Typical Performance Curves.

CAPACITIVE LOADS

The OPA641's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

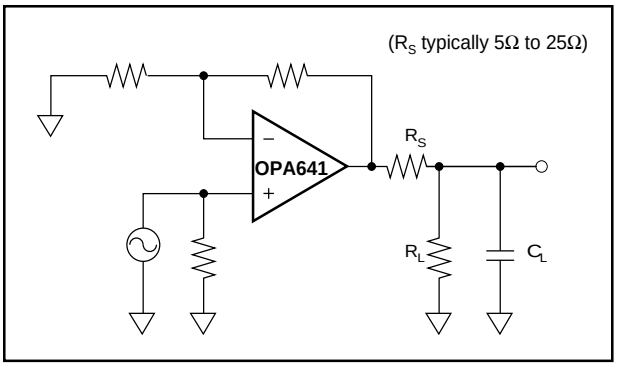


FIGURE 4. Driving Capacitive Loads.

COMPENSATION

The OPA641 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA641 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200μV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 18ns to 0.01% for a 2V step, making the OPA641 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA641 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results, a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 6 shows the test circuit used to measure settling time for the OPA641. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

DISTORTION AND NOISE

The OPA641's harmonic distortion characteristics vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance (refer to Figure 5). Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Although harmonic distortion may decrease with higher load resistances (i.e., higher feedback resistors), the effective output noise will increase due to the higher resistance. Therefore, noise or harmonic distortion may be optimized by picking the appropriate feedback resistor.

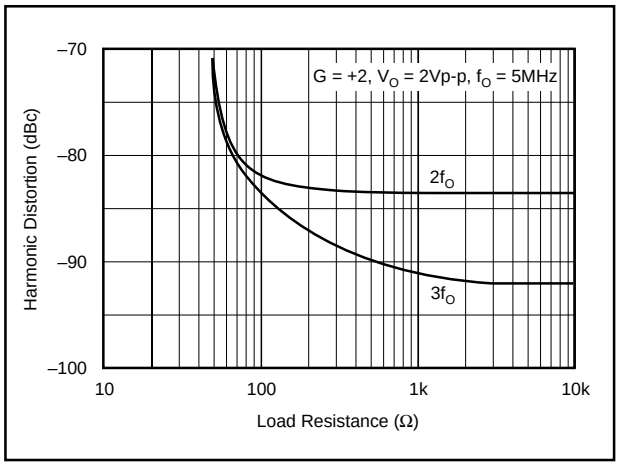


FIGURE 5. 5MHz Harmonic Distortion vs Load Resistance.

The third-order intercept point is an important parameter for many RF amplifier applications. Figure 6 shows the OPA641's single-tone third-order intercept versus frequency. This curve is particularly useful for determining the magnitude of the third harmonic as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA641 to operate in a gain of +2V/V and drive 2Vp-p into 100Ω at a frequency of 5MHz. Referring to Figure 6 we find that the intercept point is +38dBm. The magnitude of the third harmonic can now be easily calculated from the expression:

$$\text{Third Harmonic (dBc)} = 2(OPI^3P - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone

For this case OPI^3P = 38dBm, P_O = 7dBm, and the third harmonic = 2(38 – 7) = 62dB below the fundamental tone. The OPA641's low IMD makes the device an excellent choice for a variety of RF signal processing applications. The value for the two-tone third-order intercept is typically 6dB lower than the single-tone value.

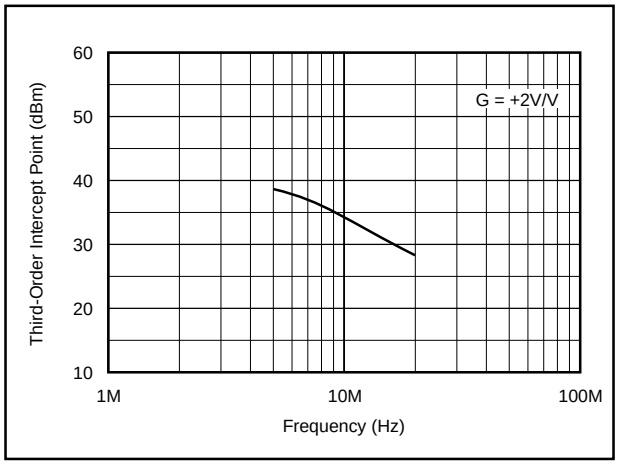


FIGURE 6. Single-Tone Third-Order Intercept Point vs Frequency.

NOISE FIGURE

The OPA641 voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA641's Noise Figure vs Source Resistance is shown in Figure 7.

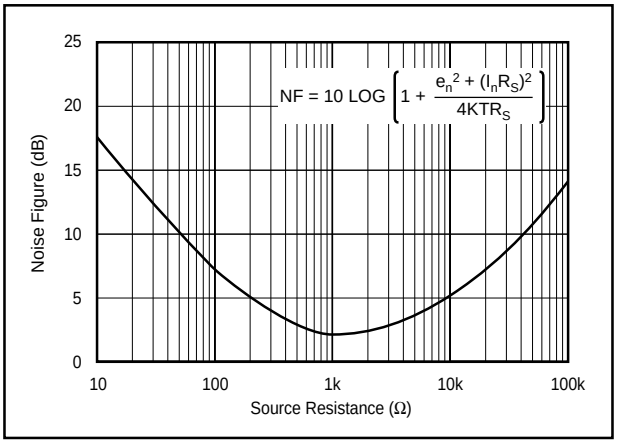


FIGURE 7. Noise Figure vs Source Resistance.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA641. Contact Burr-Brown Applications Department to receive a spice diskette.

ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device —it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected stress levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 150°C, 24 hrs
Temperature Cycling	Temperature = –65°C to 150°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Centrifuge	20,000G
Hermetic Seal	Fine: He leak rate < 5 x $1x0^{-8}$ atm cc/s, 30PSiG Gross: per Fluorocarbon bubble test, 60PSiG
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on the HSQ package only.

DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Refer to the DEM-OPA64X Datasheet for details.

APPLICATIONS

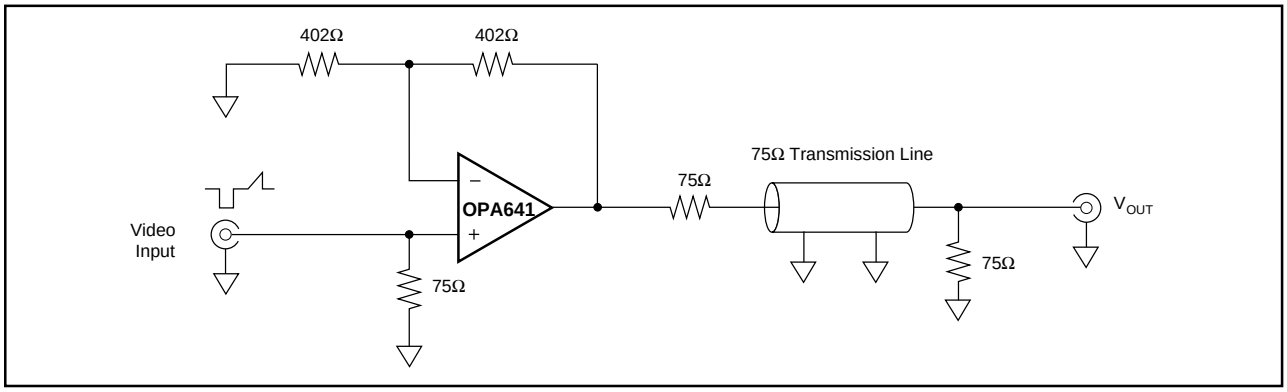


FIGURE 8. Video Gain Amplifier.

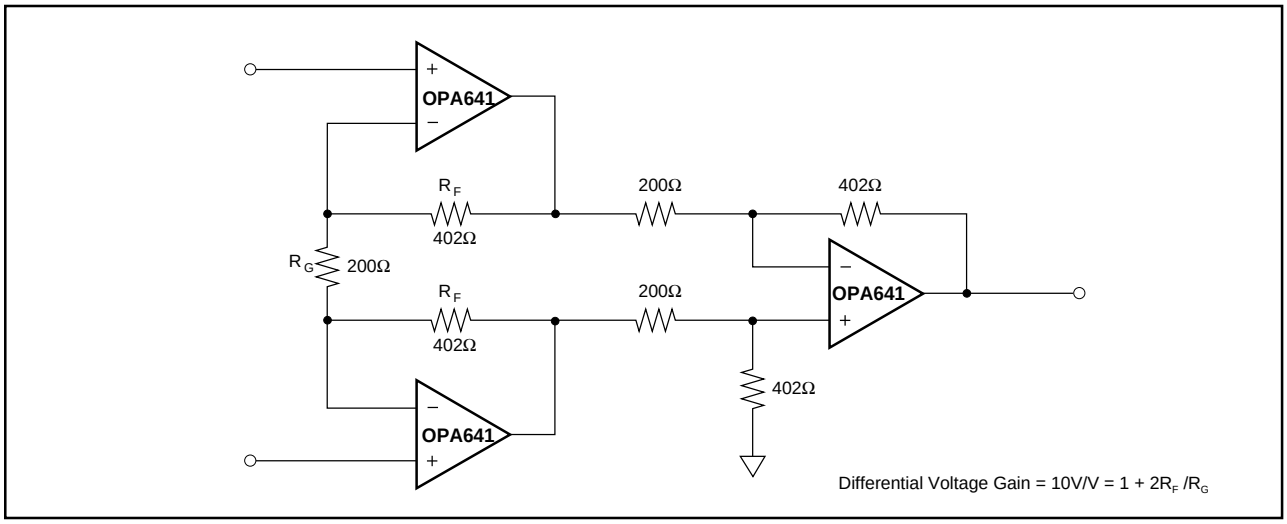


FIGURE 9. Wideband, Fast-Settling Instrumentation Amplifier.

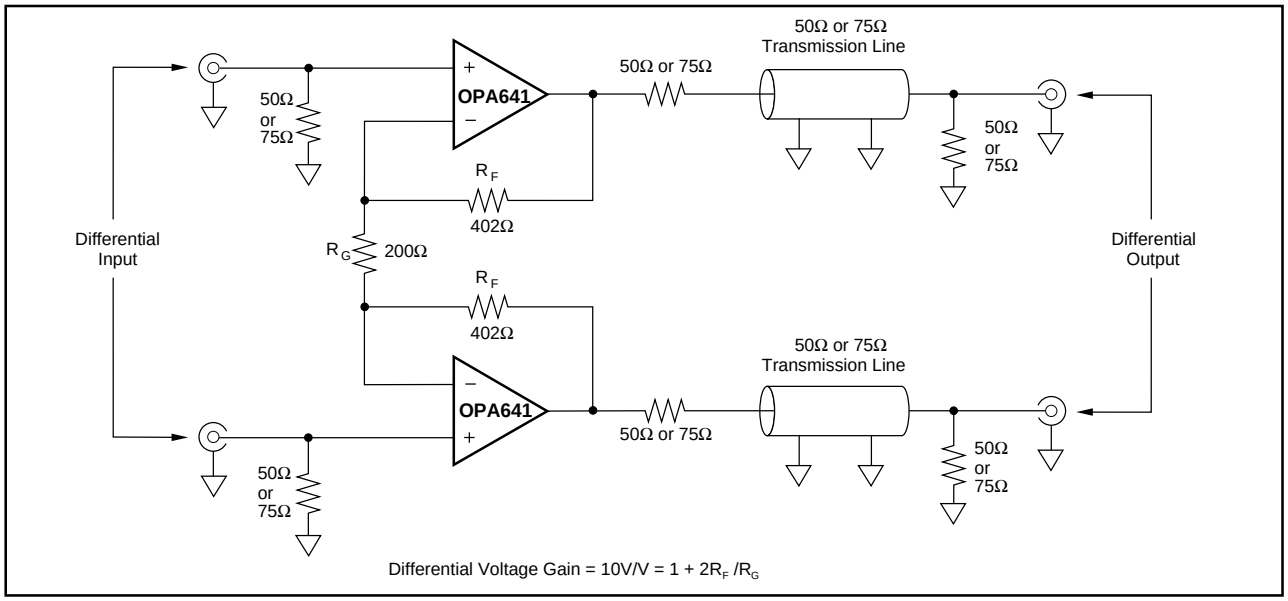


FIGURE 10. Differential Gain Amplifier and Driver for 50Ω or 75Ω Systems.

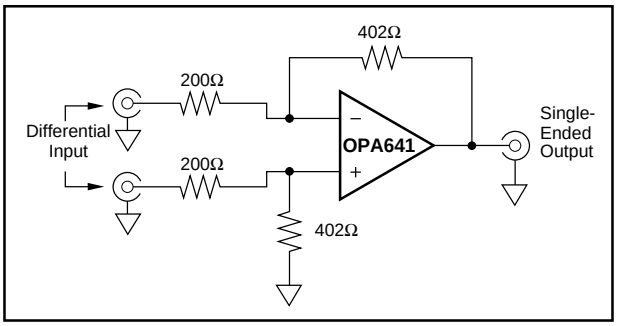


FIGURE 11. Difference Amplifier with Gain.

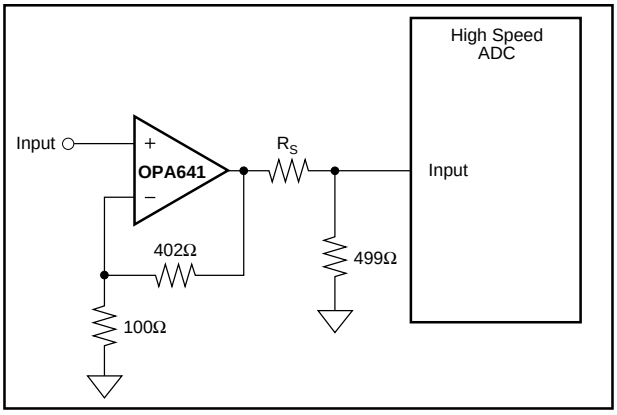


FIGURE 12. Gain Amplifier for ADCs (G = +5V/V).

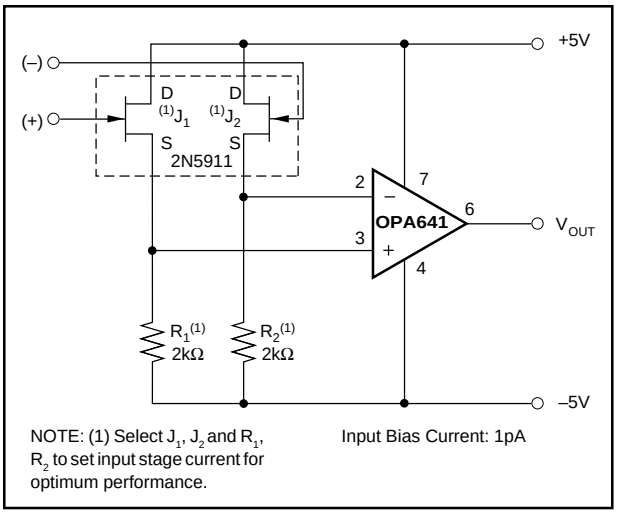
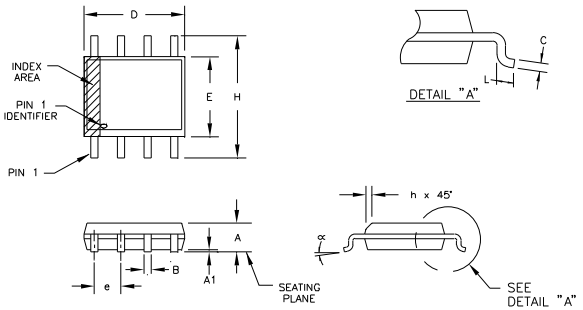


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

PACKAGE DRAWINGS

Package Number 182 - 8-Lead SO-8 Surface Mount

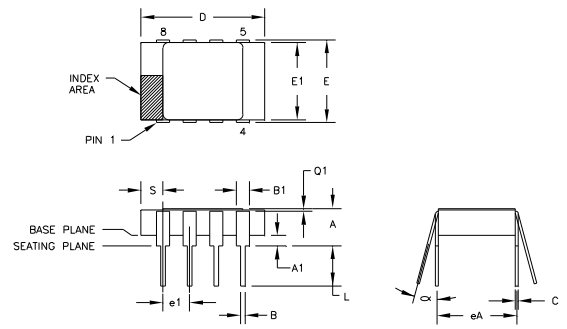


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.054	.068	1.37	1.73	
A1	.004	.009	0.10	0.23	
B	.014	.019	0.36	0.48	
C	.008	.0098	0.20	0.25	
D	.189	.196	4.80	4.98	
E	.150	.157	3.81	3.99	
e	.050 BASIC		1.27 BASIC		
H	.229	.244	5.82	6.20	
h	.010	.019	0.25	0.48	
L	.016	.050	0.41	1.27	
N	8		8		
∝	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.086 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 | REV.: F
JEDEC NUMBER: MS-012

Package Number 157 - 8-Pin Ceramic, Side-Braze DIP

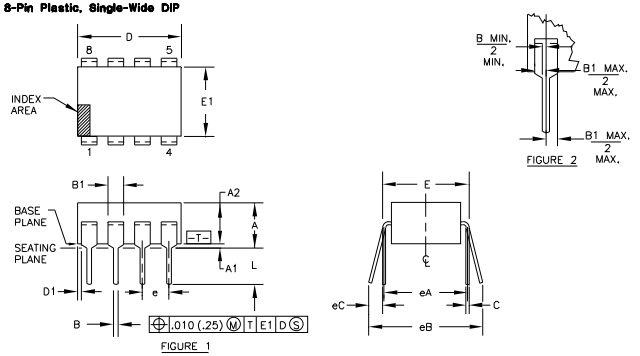


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.105	.175	2.67	4.45	
A1	.025	.055	0.64	1.40	
B	.015	.021	0.38	0.53	
B1	.038	.060	0.97	1.52	
C	.008	.012	0.20	0.30	
D	.380	.550	9.65	13.97	
E	.290	.325	7.37	8.26	
E1	.280	.310	7.11	7.87	6
e1	.100 TYP.		2.54 TYP.		2
eA	.300 TYP.		7.62 TYP.		2
L	.125	.175	3.18	4.45	
N	8		8		4
Q1	.010	--	2.54	--	
S	.030	.120	0.76	3.05	
∝	0°	15°	0°	15°	3

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .13mm (.005) RADIUS OF TRUE POSITION (TP) WITH MAXIMUM MATERIAL CONDITION.
3. ∝ APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE BASE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKAGE MATERIALS.
7. CONTROLLING DIMENSION: INCH.

PACKAGE NUMBER: ZZ157 | REV.: B
JEDEC NUMBER: MO-036

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
B	.014	.022	0.36	0.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	0.20	0.38	
D	.348	.430	8.84	10.92	4
D1	.005	--	0.13	--	
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
L	.115	.160	2.92	4.06	3
N	8		8		7

NOTES:
1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 4, 5, AND 8) MAY BE CONFIGURED AS SHOWN IN FIGURE 2.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 | REV.: D
JEDEC NUMBER: MS-001