BURR - BROWN®

OPA628

Low Distortion Wideband OPERATIONAL AMPLIFIER

FEATURES

- EXCELLENT DIFFERENTIAL GAIN: 0.015%
- EXCELLENT DIFFERENTIAL PHASE: 0.015°
- LOW DISTORTION: 90dB SFDR
- TWO-TONE THIRD-ORDER INTERCEPT: 60dBm
- LOW NOISE: 2.5nV/$\sqrt{Hz}$
- LOW NOISE FIGURE: 9dB
- BANDWIDTH (Gain = +1): 160MHz
- 0.1dB GAIN FLATNESS: 30MHz
- LOW OFFSET VOLTAGE: 500µV

APPLICATIONS

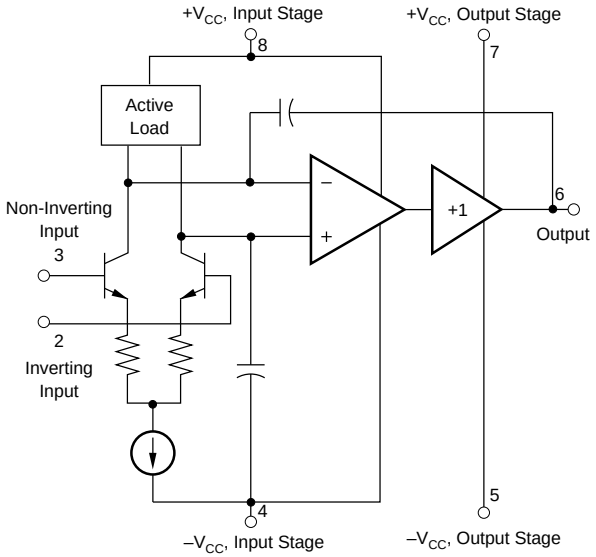
- BROADCAST QUALITY VIDEO
- MEDICAL IMAGING
- LOW NOISE PREAMPLIFIER
- PRECISION ADC/DAC BUFFER
- TELECOMMUNICATIONS
- ANALYTICAL INSTRUMENTS
- ACTIVE FILTERS
- DC RESTORATION CIRCUITS

DESCRIPTION

The OPA628 is a low distortion, wideband operational amplifier. It features low differential gain error of 0.015% and low differential phase error of 0.015° at NTSC and PAL frequencies with a 150Ω load (a back-terminated 75Ω cable). The 0.1dB gain flatness to 30MHz, and the excellent differential gain and phase make the OPA628 ideal for broadcast quality video applications. In addition, the spurious free dynamic range of 90dB makes the OPA628 an excellent choice to buffer the input of precision Analog-to-Digital converters. It can also be used to provide a buffer for the output of precision high speed Digital-to-Analog converters. The two-tone third-order intercept of the OPA628 is 60dBm.

The OPA628 is a unity gain stable, voltage feedback operational amplifier. It has all of the benefits associated with voltage feedback amplifiers including high input impedance, high common mode rejection, and symmetrical differential input flexibility. The unity gain bandwidth of the OPA628 is 160MHz. The low noise of 2.5nV/$\sqrt{Hz}$ and low noise figure of 9dB (R_S = 50Ω) make the OPA628 very useful in precision applications requiring wide dynamic range.

The superior distortion performance of the OPA628 is achieved by its multistage architecture which provides high open-loop gain. The distortion performance is additionally enhanced by separating the power supplies to the input and output stages requiring four power supply connections as shown in the block diagram below. This separation of supplies eliminates the effects of package and wire bond parasitic capacitance and inductance. The OPA628 is powered with ±5VDC supplies for low power dissipation. The OPA628 is available in 8-pin plastic DIP and SOIC packages. The temperature range is –40°C to +85°C.



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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5VDC, R_L=100Ω (including feedback impedance), and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA628AP, AU MIN	OPA628AP, AU TYP	OPA628AP, AU MAX	UNITS
INPUT NOISE					
Voltage: R_S = 0Ω	f_O = 100Hz		8.3		nV/√Hz
	f_O = 1kHz		3.5		nv/√Hz
	f_O = 10kHz		2.6		nV/√Hz
	f_O = 100kHz		2.5		nV/√Hz
	f_O = 1MHz to 100MHz		2.5		nV/√Hz
	f_B = 100Hz to 10MHz		8.1		µVrms
Current	f_O = 100kHz to 100MHz		2.2		pA/√Hz
Noise Figure	R_S = 50Ω, f_O = 1MHz to 100MHz		9.3		dB
OFFSET VOLTAGE					
Input Offset Voltage	V_{CM} = 0VDC		±0.5	±1	mV
Average Drift	T_A = T_{MIN} to T_{MAX}		±6		µV/°C
Supply Rejection (PSRR)	±V_{CC} = ±4.5V to ±5.5V	90	105		dB
Over Specification Temperature	±V_{CC} = ±4.5V to ±5.5V, T_A = T_{MIN} to T_{MAX}		100		dB
INPUT BIAS CURRENT					
Input Bias Current	V_{CM} = 0VDC		15	30	µA
Over Specification Temperature	V_{CM} = 0VDC, T_A = T_{MIN} to T_{MAX}		22		µA
Input Offset Current	V_{CM} = 0VDC		±0.3	±2	µA
Over Specification Temperature	T_A = T_{MIN} to T_{MAX}		±0.8		µA
INPUT IMPEDANCE					
Differential	Open–Loop		30 || 2		kΩ || pF
Common-Mode			10 || 6		MΩ || pF
INPUT VOLTAGE RANGE					
Common-Mode Input Range			±2.5		V
Common-Mode Rejection (CMRR)	V_{CM} = ±2.5V	90	110		dB
Over Specification Temperature	V_{CM} = ±2.5V, T_A = T_{MIN} to T_{MAX}		105		dB
OPEN-LOOP GAIN, DC					
Open-Loop Voltage Gain		90	100		dB
Over Specification Temperature	T_A = T_{MIN} to T_{MAX}		96		dB
FREQUENCY RESPONSE					
Closed-Loop Bandwidth	Gain = +1V/V		160		MHz
(–3dB)	Gain = +2V/V		77		MHz
	Gain = +5V/V		24		MHz
Bandwidth 0.1dB Flat	Gain = +2V/V		30		MHz
Differential Gain	3.58MHz, Gain = +2, V_O = 1.4V Ramp		0.015		%
Differential Phase	3.58MHz, Gain = +2, V_O = 1.4V Ramp		0.015		degrees
Harmonic Distortion	R_L = 100Ω, G = +1V/V, f = 5MHz, V_O = 2Vp-p				
	Second Harmonic		–91		dBc
	Third Harmonic		–98		dBc
	R_L = 500Ω, G = +2V/V, f = 5MHz, V_O = 2Vp-p				
	Second Harmonic		–90		dBc
	Third Harmonic		–97		dBc
	R_L = 500Ω, G = +2V/V, f = 10MHz, V_O = 2Vp-p				
	Second Harmonic		–83		dBc
	Third Harmonic		–87		dBc
3rd-Order Intercept	f_C = 5MHz, G = +2		70		dBm
3rd-Order Intercept	f_C = 10MHz, G = +2		60		dBm
Two-tone 3rd-Order Intercept	f_C = 5MHz, G = +2		60		dBm
Full Power Response[1]	V_O = 5Vp-p, Gain = +1V/V		20		MHz
	V_O = 2Vp-p, Gain = +1V/V		49		MHz
Slew Rate	2V Step, Gain = –1V/V		310		V/µs
Overshoot	2V Step, Gain = –1V/V		2		%
Settling Time: 0.10%	2V Step, Gain = –1V/V		20		ns
0.01%			64		ns
Overload Recovery Time[2]			60		ns
Phase Margin	Gain = +1V/V		60		degrees
Rise Time	Gain = +1V/V, 10% to 90%				
Small Signal	V_O = 100mVp-p		3		ns
Large Signal	V_O = 6Vp-p		15		ns
RATED OUTPUT					
Voltage Output	f_O = 1MHz, R_L = 100Ω	±3			V
Over Specification Temperature	f_O = 1MHz, R_L = 100Ω, T_A = T_{MIN} to T_{MAX}		±3		V
	f_O = 1MHz, R_L = 50Ω		±3		V
Output Resistance	1MHz, Gain = +1V/V		0.0005		Ω
Load Capacitance Stability	Gain = +1V/V, V_O = 2Vp-p		20		pF
Short Circuit Current	Continuous, Source		+180		mA
Short Circuit Current	Continuous, Sink		–130		mA

SPECIFICATIONS (CONT)

ELECTRICAL

At V_{CC} = ±5VDC, R_L=100Ω (including feedback impedance), and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	OPA628AP, AU MIN	OPA628AP, AU TYP	OPA628AP, AU MAX	UNITS
POWER SUPPLY					
Rated Voltage	$\pm V_{CC}$		±5		VDC
Derated Performance	$\pm V_{CC}$	±4.5		±6	VDC
Current, Quiescent	I_O = 0mADC		29	32	mA
Current, Quiescent	I_O = 0mADC, $T_A = T_{MIN}$ to T_{MAX}		31	35	mA
TEMPERATURE RANGE					
Specification: AP, AU	T_{MIN} and T_{MAX}	–40		+85	°C
Storage: AP, AU	Ambient Temperature	–55		+125	°C
θ_{JA} AP			90		°C/W
AU			100		°C/W

NOTES: (1) Full power response = slew rate/(2πVpeak). (2) Time for output to resume linear operation after saturation.

ORDERING INFORMATION

MODEL	PACKAGE
OPA628AP	8-Pin Plastic DIP
OPA628AU	8-Pin SOIC

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA628AP	8-Pin Plastic DIP	006
OPA628AU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

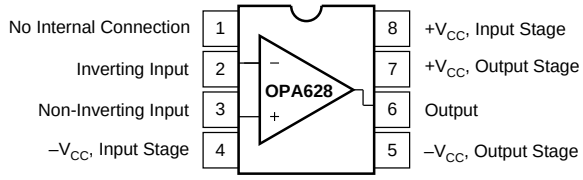
ABSOLUTE MAXIMUM RATINGS

Supply	±7VDC
Internal Power Dissipation[1]	See Applications Information
Differential Input Voltage	5V
Input Voltage Range	See Applications Information
Storage Temperature Range: AP, AU	–55°C to +125°C
Lead Temperature (soldering, DIP 10s)	+300°C
(soldering, SOIC 3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous to Ground
Junction Temperature (T_J)	+175°C

NOTE: (1) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

PIN CONFIGURATION

Top View — **8-Pin Plastic DIP, 8-Pin Plastic SOIC**



ELECTROSTATIC DISCHARGE SENSITIVITY

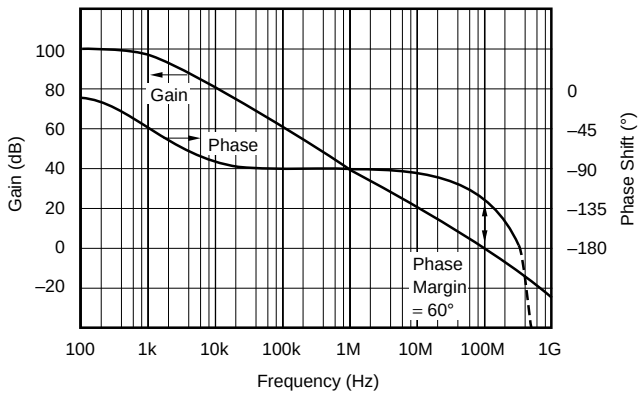
Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

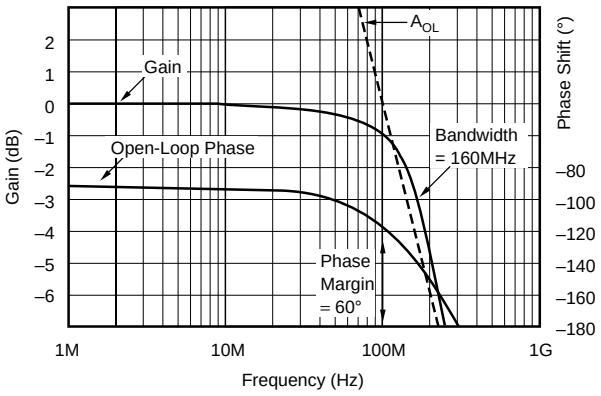
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5VDC, R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.

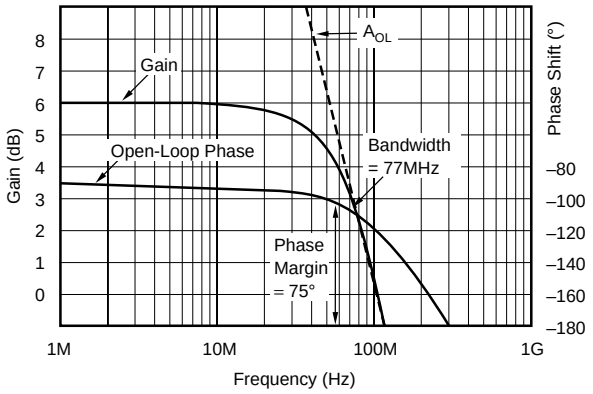
OPEN-LOOP FREQUENCY RESPONSE



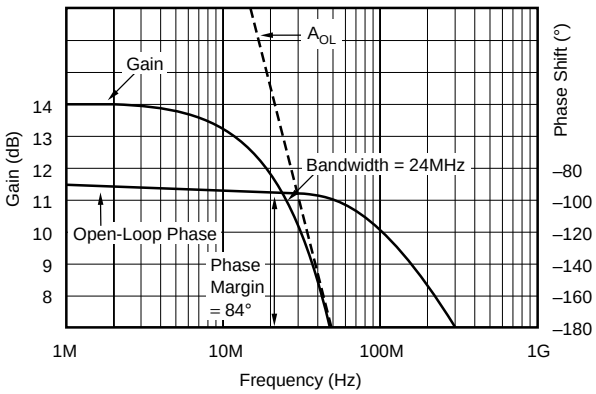
A_V = +1V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



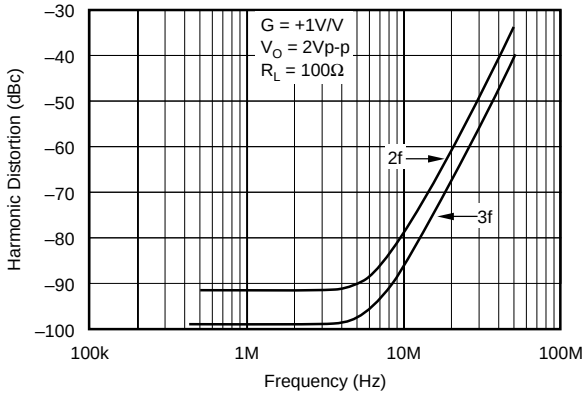
A_V = +2V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



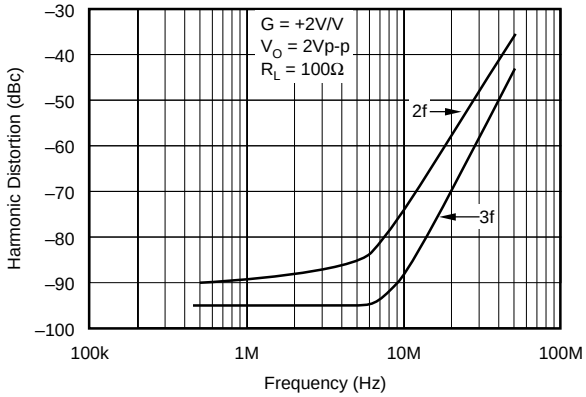
A_V = +5V/V CLOSED-LOOP SMALL SIGNAL BANDWIDTH



HARMONIC DISTORTION vs FREQUENCY



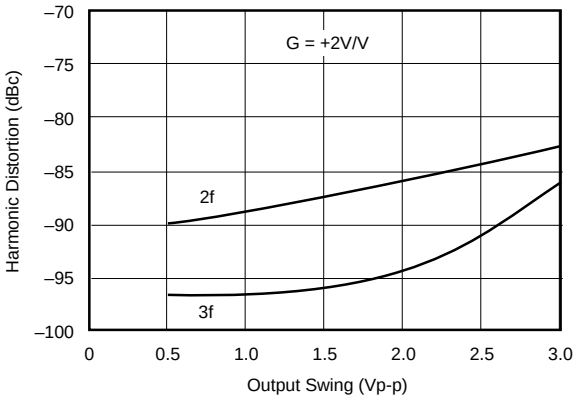
HARMONIC DISTORTION vs FREQUENCY



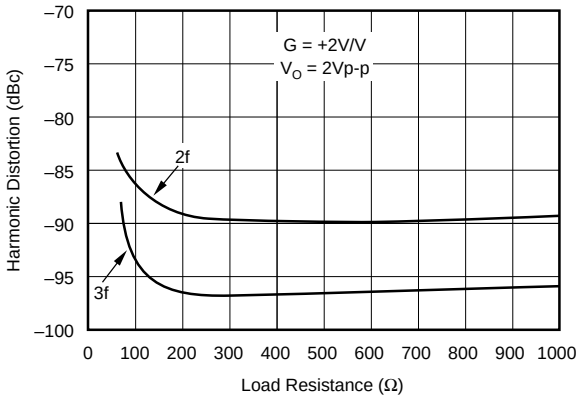
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, and R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.

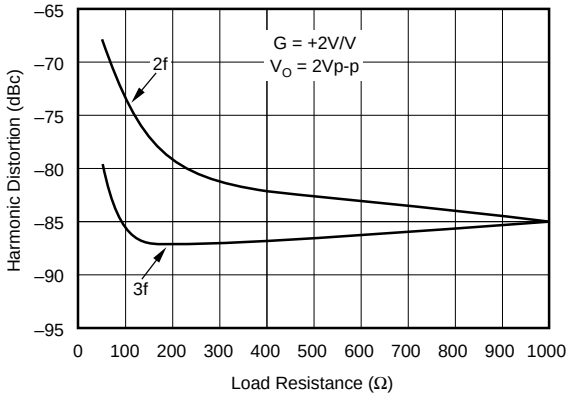
5MHz HARMONIC DISTORTION vs OUTPUT SWING



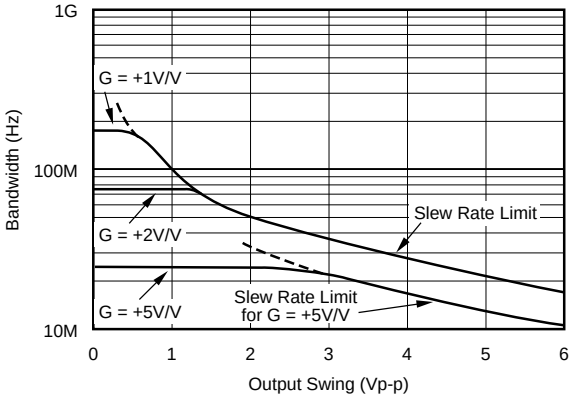
5MHz HARMONIC DISTORTION vs LOAD RESISTANCE



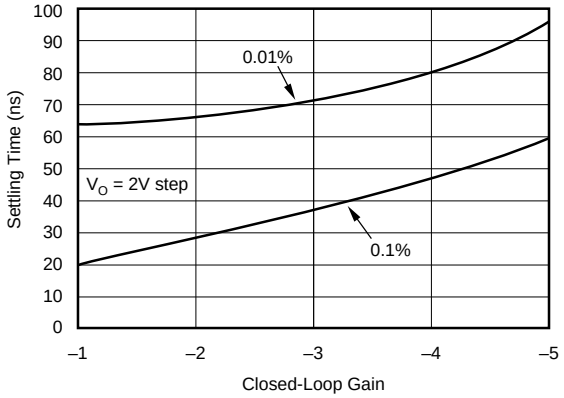
10MHz HARMONIC DISTORTION vs LOAD RESISTANCE



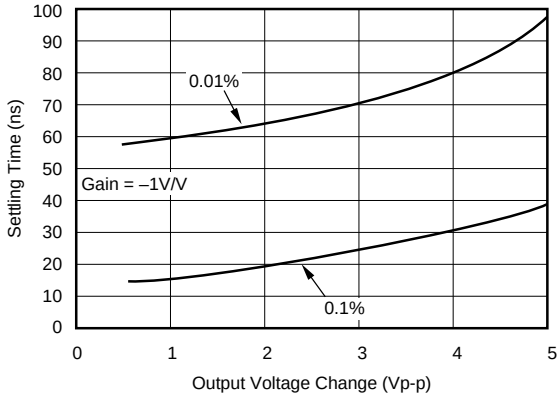
FULL-POWER BANDWIDTH vs OUTPUT SWING



SETTLING TIME vs CLOSED-LOOP GAIN



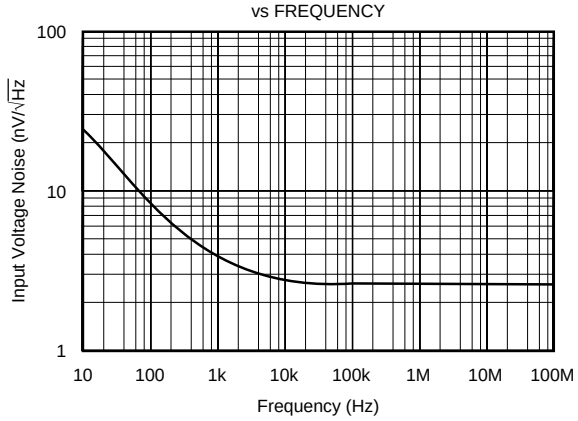
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



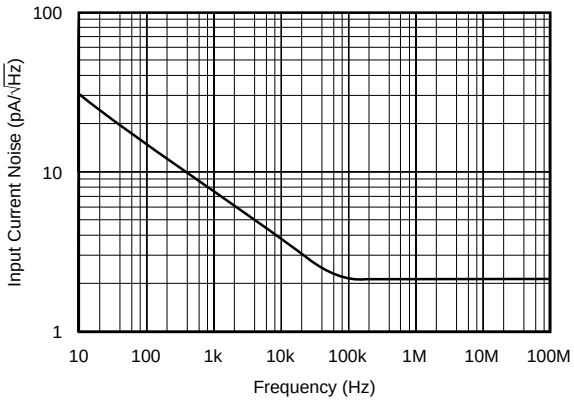
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.

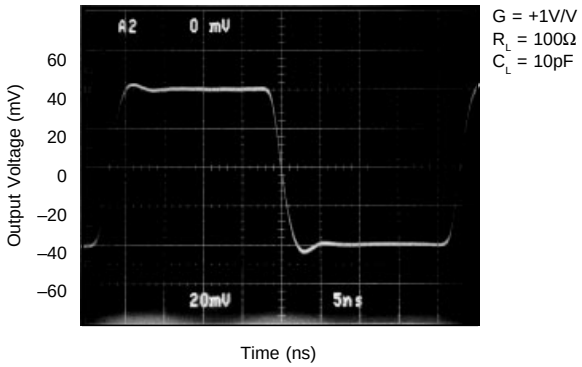
INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



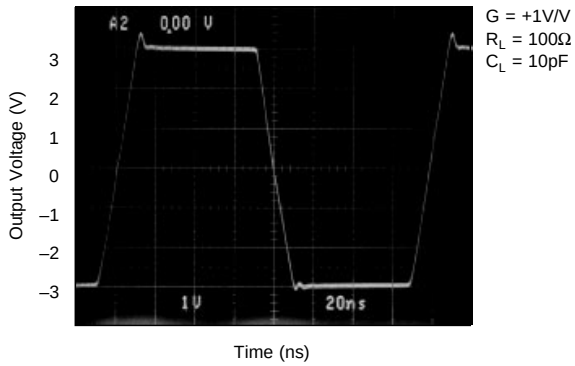
INPUT CURRENT NOISE SPECTRAL DENSITY



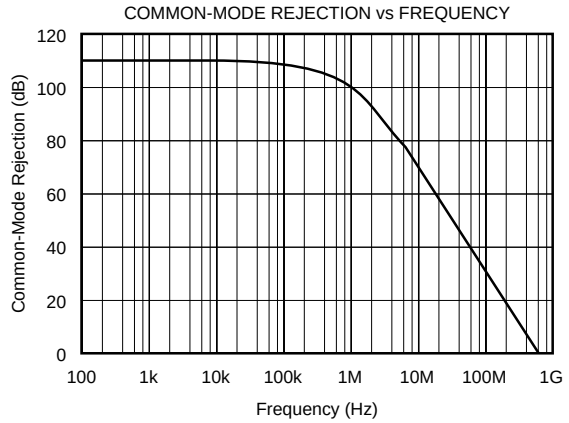
SMALL SIGNAL TRANSIENT RESPONSE



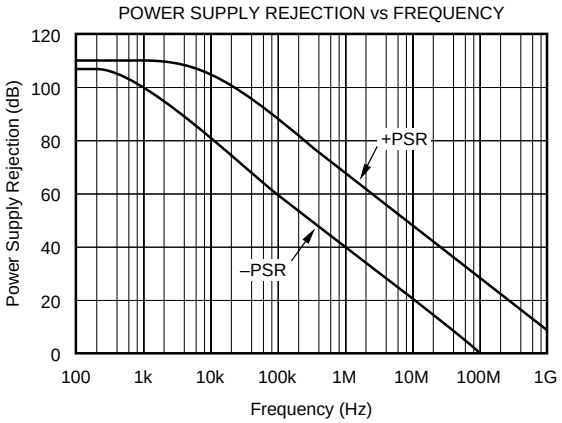
LARGE SIGNAL TRANSIENT RESPONSE



COMMON-MODE REJECTION vs FREQUENCY



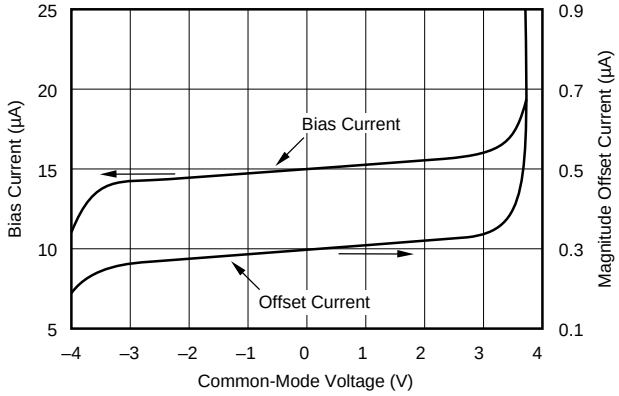
POWER SUPPLY REJECTION vs FREQUENCY



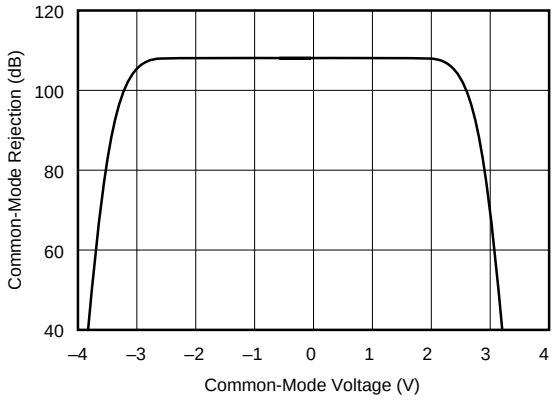
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.

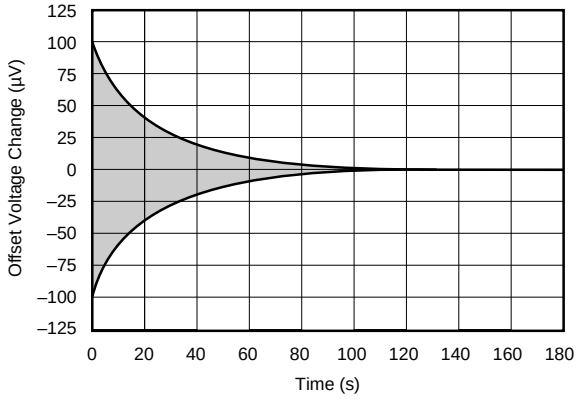
BIAS AND OFFSET CURRENT
vs INPUT COMMON-MODE VOLTAGE



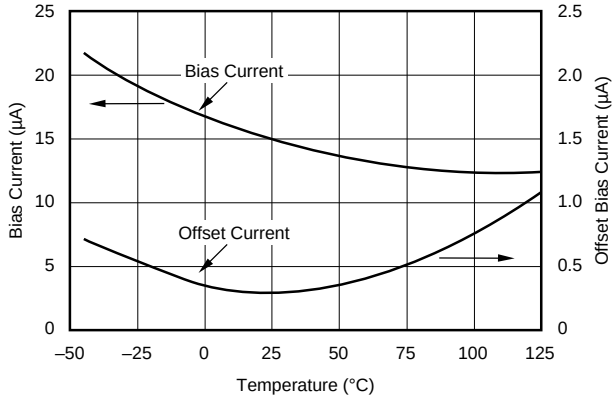
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



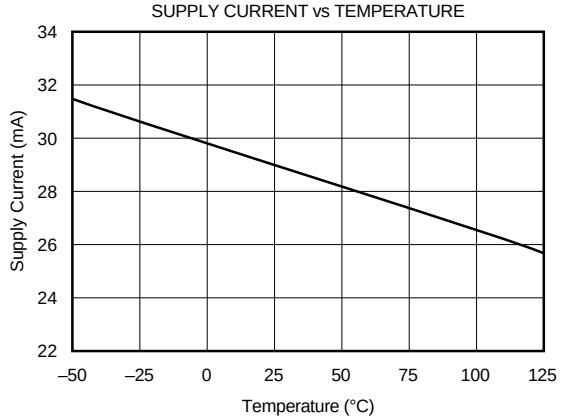
INPUT OFFSET VOLTAGE WARM-UP DRIFT



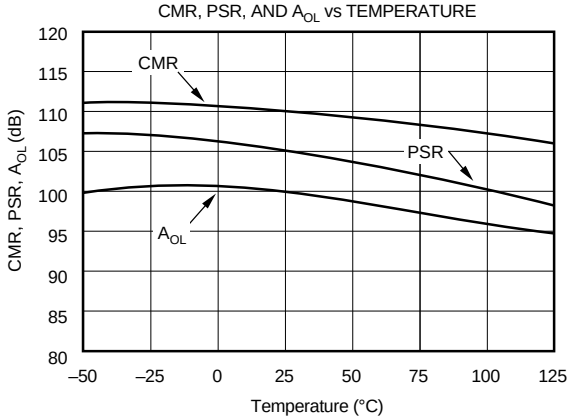
BIAS AND OFFSET CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE

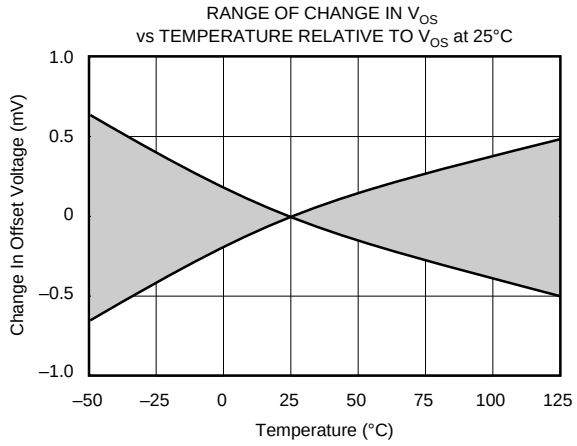


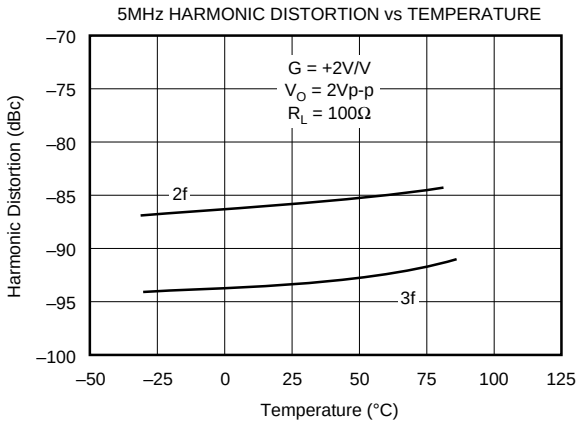
CMR, PSR, AND A_{OL} vs TEMPERATURE



TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_L = 100Ω (including feedback impedance), and T_A = +25°C unless otherwise noted.





DISCUSSION OF PERFORMANCE

The OPA628's classical operational amplifier architecture employs true differential and fully symmetrical inputs allowing optimal performance in either inverting or non-inverting circuit applications. All traditional circuit configurations and op amp theory apply to the OPA628. The use of low drift thin film resistors allows internal operating currents to be laser trimmed at wafer level to optimize AC performance such as distortion, bandwidth and settling time, as well as DC parameters such as input offset voltage. The result is a wideband, high frequency monolithic operational amplifier with a gain-bandwidth product of 150MHz, a spurious free dynamic range (SFDR) of 90dB, and input offset voltage of 500µV.

The layout considerations described in the "Printed Circuit Board Guidelines" section must be followed to achieve the best possible performance of the OPA628.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL subcarrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set. All PAL measurements were performed using a Rohde & Schwarz Video Analyzer UAF.

DG and DP of the OPA628 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 1 delivered a 100IRE modulated ramp to the 75Ω input of the video analyzer. The signal averaging feature of the analyzer was used to establish a reference against which the performance of the amplifier was measured. Signal averaging was also used to measure the DG and DP of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA628 is 0.015% differential gain and 0.015° differential phase to both NTSC and PAL standards. Increasing the closed-loop gain degrades the DP and DG.

GAIN FLATNESS

Small signal ±0.1dB gain flatness can be achieved up to 30MHz in a non-inverting gain of +2V/V through careful layout of the printed circuit board and frequency shaping of the feedback network. Frequency shaping is achieved empirically by placing a small capacitor in parallel with either the feedback resistor or the input resistor of the OPA628 to compensate for printed circuit parasitic capacitance. A capacitor in the range of approximately 1pF to 20pF is suggested. Printed circuit board layout design will determine if the capacitor should be placed across the feedback resistor or the input resistor.

Small signal ±0.1dB gain flatness of greater than 30MHz can be achieved at a gain of +1V/V. To eliminate the effects of package lead inductance, a small value resistor should be included in the feedback path. Maximizing gain flatness for a particular layout requires optimization of the feedback resistor; an approximate value is 50Ω to 75Ω.

DISTORTION

The OPA628's Harmonic Distortion characteristics when driving a 100Ω load are shown vs frequency and vs voltage output in the Typical Performance Curves. Distortion can be further optimized by decreasing output loading as also

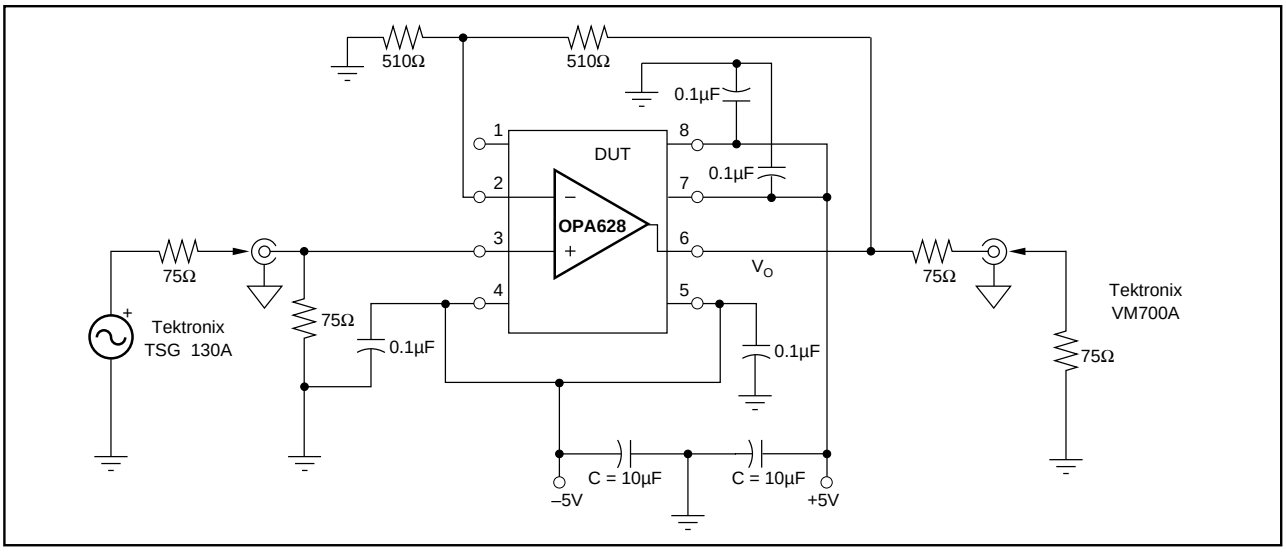


FIGURE 1. Configuration For Testing Differential Gain/Phase.

shown in Typical Performance Curves. Include the contribution of the feedback resistance when calculating the effective load resistance at the amplifier output. A high performance spectrum analyzer such as the HP3585B should be used to measure distortion.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. The specification table shows the OPA628's two-tone, third order IM intercept at 5MHz and 10MHz. For these measurements, tones were spaced 200kHz apart. This data is particularly useful for determining the magnitude of the third-order IM products. The magnitude of the third-order IM products can be easily calculated from the expression:

$$\text{Third IM} = 2(\text{OPI}^3\text{P} - P_O)$$

where OPI^3P = third-order output intercept, dBm
P_O = output level/tone, dBm/tone
Third IM = third-order intermodulation ratio below each output tone, dB

As an example, with OPI^3P = 60dBm, for P_O = 10dBm, the third order IM = 2(60 – 10) = 100dB below either 10dBm tone. The OPA628's low IM makes the device an excellent choice for a variety of RF signal processing applications. In order to obtain the full low distortion performance of the OPA628, it is imperative to follow the recommendations described in the "Printed Circuit Board Guidelines" section.

OUTPUT DRIVE CAPABILITY

The OPA628 has been optimized for low distortion performance with back terminated 50Ω and 75Ω loads (R_{LOAD} = 100Ω and 150Ω, respectively). However, it is capable of driving 6Vpp into a 50Ω load with a sacrifice in distortion. This high-output drive capability makes the OPA628 an ideal choice for a wide range of RF, IF, and video applications. All transmission lines should be terminated with the characteristic impedance of the transmission line.

Internal current-limiting circuitry limits output current to about 130mA at 25°C. This prevents damage from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 2, the OPA628 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

NOISE FIGURE

The OPA628's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA628's Noise Figure vs Source Resistance is shown in Figure 3 for frequencies above 1MHz.

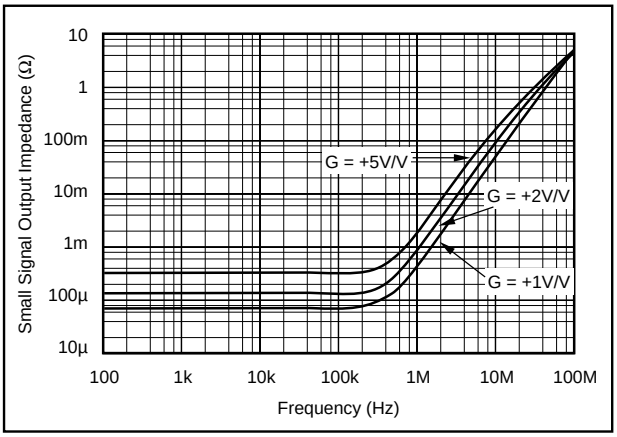


FIGURE 2. Small Signal Output Impedance vs Frequency.

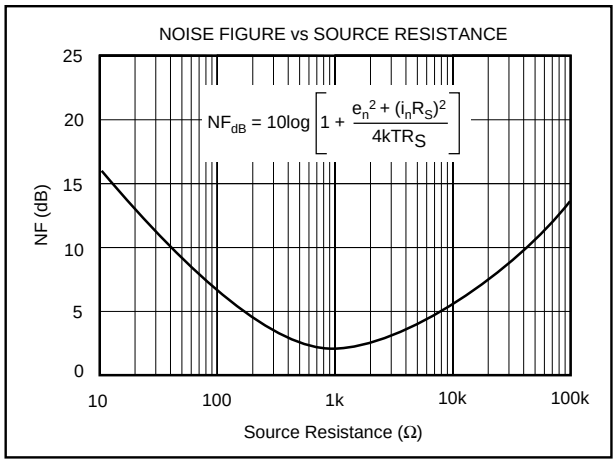


FIGURE 3. Noise Figure vs Source Resistance.

SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, is only 64ns to 0.01% for a 2V step. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Printed Circuit Board Guidelines." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 60ns. Settling time measurements for the OPA628 were performed in the circuit configuration of Figure 5. A sampling oscilloscope was used with signal averaging.

CAPACITIVE LOADS

Capacitive loads will decrease the OPA628's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 20pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 4. This is particularly important when driving high capacitance loads such as flash A/D converters.

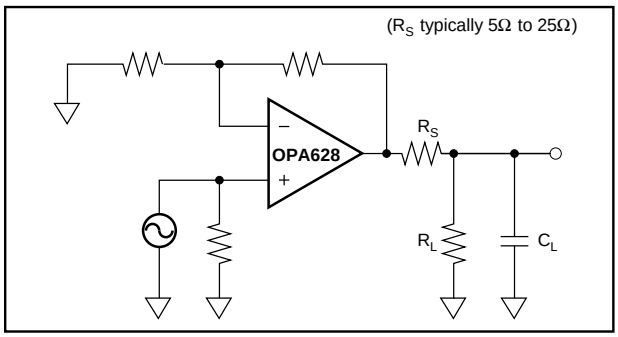


FIGURE 4. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/ft for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

COMPENSATION

The OPA628 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2V/V.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA628 in a good layout is very flat with frequency. However, some circuit configurations, such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

THERMAL CONSIDERATIONS

The OPA628 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 6.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where P_{DQ} is the quiescent power dissipation and P_{DL} is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, P_{DQ} = 10V X 32mA = 320mW, max). For the case where the amplifier is driving a grounded load (R_L) with a DC voltage (V_{OUT}) the maximum value of P_{DL} occurs at $V_{OUT} = V_{CC}/2$, and is equal to P_{DL}, max = $(V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common P_{DL} = 5V X 180mA = 900mW. Thus, P_D, max = 320mW + 900mW ≈ 1.2W.

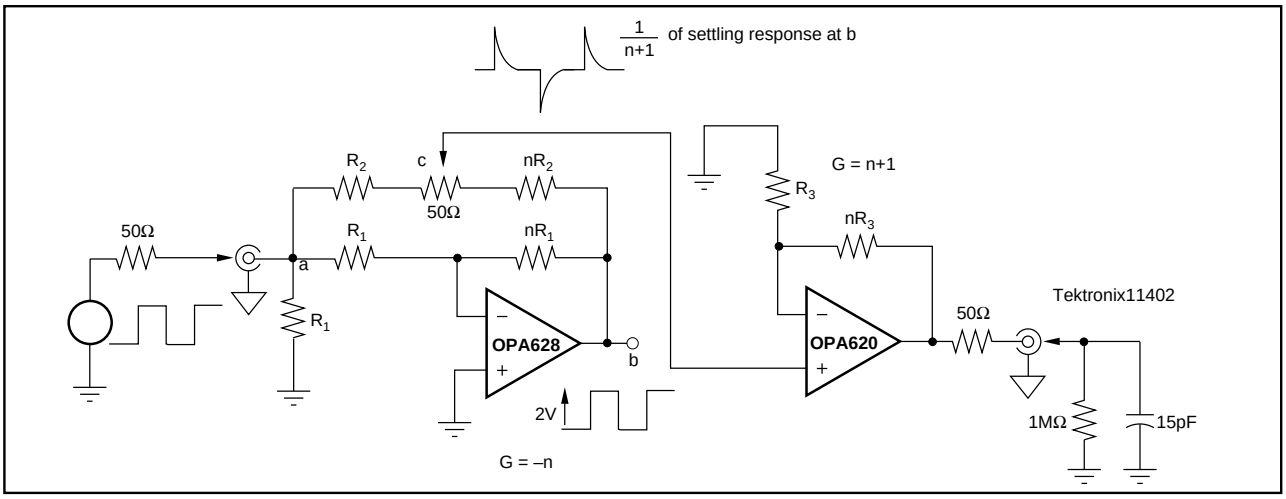


FIGURE 5. Settling Time Test Circuit.

Note that the short circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1.2W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, θ_{JA}, of each package. The variation of short circuit current with temperature is shown in Figure 7.

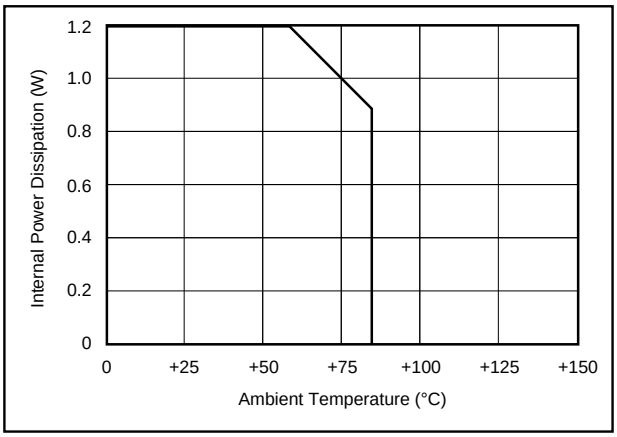


FIGURE 6. Maximum Power Dissipation.

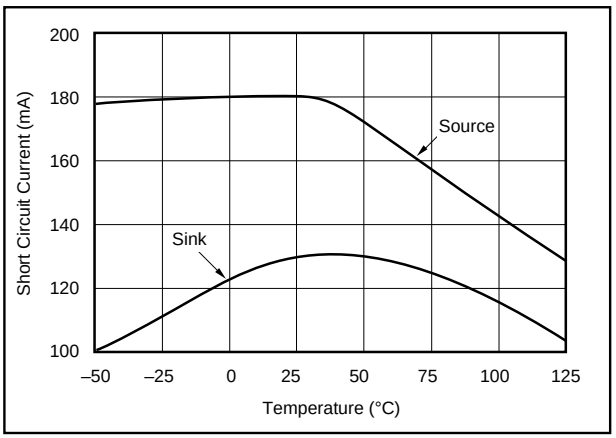


FIGURE 7. Short Circuit Current vs Temperature.

INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA628 incorporates on-chip ESD protection diodes as shown in Figure 8. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

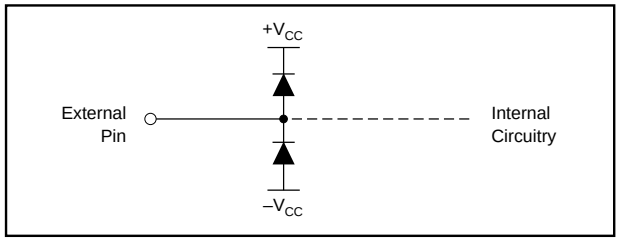


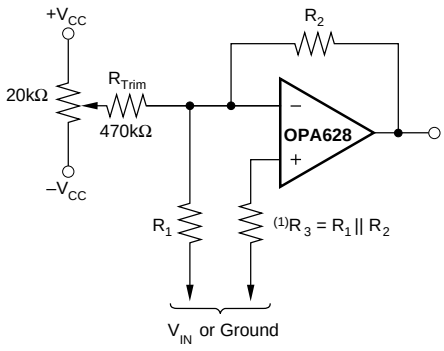
FIGURE 8. Internal ESD Protection.

All pins on the OPA628 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to approximately 10mA whenever possible.

OFFSET VOLTAGE ADJUSTMENT

The OPA628's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 9 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by

the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with R_3. This will reduce error due to the amplifier's input bias current.



NOTE: (1) R_3 is optional and can be used to reduce error due to input bias currents.

FIGURE 9. Offset Voltage Trim.

SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models are available for the OPA628. Contact Burr-Brown Applications Department to receive a SPICE diskette.

RELIABILITY DATA

Reliability reports are available upon request for each of the package options offered.

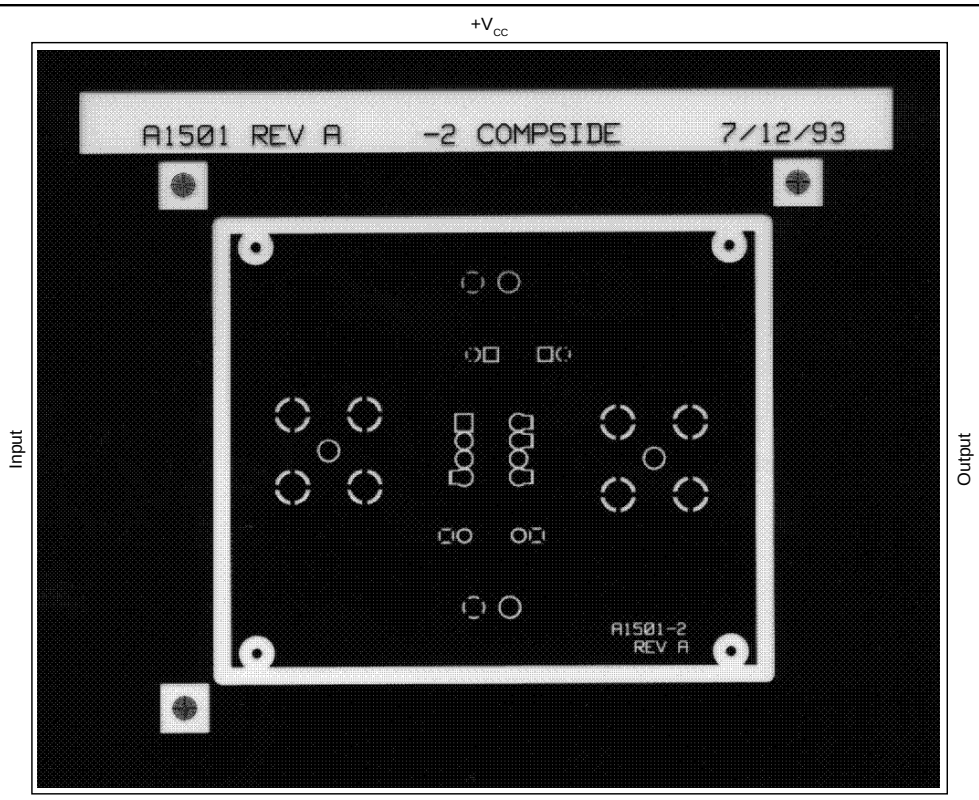
DEMONSTRATION BOARDS

Contact Burr-Brown Applications Department for availability of demonstration boards for the OPA628. There are separate demonstration boards for the DIP and SOIC packages. These demonstration boards use the PC board layouts shown in Figures 10a and 10b. They are carefully designed for optimum low distortion performance as described in the wiring precaution section.

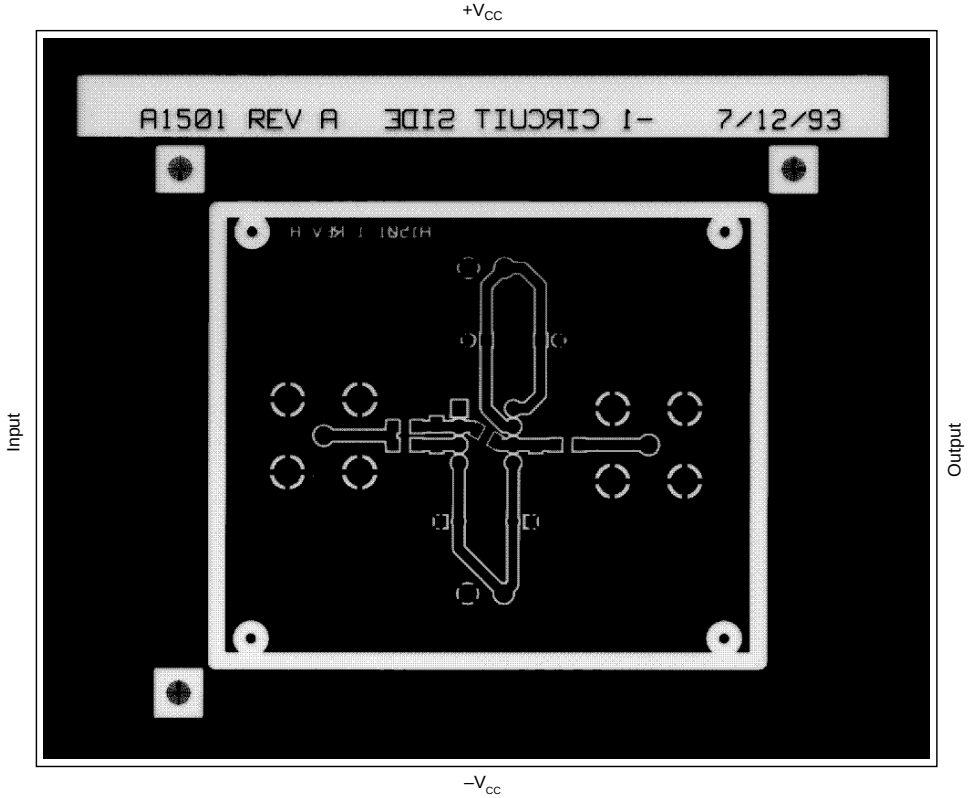
PRINTED CIRCUIT BOARD GUIDELINES

The printed circuit board layout is critical to obtaining the full performance of the OPA628, particularly optimum distortion and gain flatness. The guidelines below should be employed to design the OPA628 printed circuit board. Conceptual layouts illustrating these guidelines for the DIP and SOIC packages are shown in Figures 10a and 10b.

1. Establish the primary ground plane on the IC side of the PC board. The primary ground plane is the lowest impedance ground plane, it should be as wide as possible with minimal interruptions. Connect all unused space on both sides of the board to the ground plane. The ground plane should extend beneath the body of the IC on **both** sides of the board. A 2-ounce copper ground plane is recommended. The input signal ground return, the load return, and the power supply common should all be connected to the same physical point to avoid ground loops which can cause unwanted feedback.
2. The entire physical circuit should be as small as practical. All signal and power supply paths should be as short and direct as possible to minimize stray capacitance and inductance which are detrimental to high frequency performance. Minimize signal trace impedance by keeping traces as wide and short as possible. Stray capacitance should be minimized, especially at high impedance nodes such as the amplifier's input terminals. In addition, stray signal coupling from the output of the amplifier back to the input should be minimized.
3. In general, the use of surface mount components improves performance over through-hole components by minimizing parasitics. (However, it should be noted that use of the DIP version of the OPA628 will not compromise amplifier performance.) If circuit elements with leads are used, the leads should be kept as short as possible (6mm) to minimize lead inductance. Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1,000Ω on the high end and to a value that is within the amplifier's output drive limits on the low end. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load.
4. As with any low distortion, wide bandwidth amplifier, power supply bypassing is extremely critical and must always be used. The system power supplies should be well bypassed at the board level with a minimum of 2.2µF tantalum capacitors. In addition, all four power supply leads should be locally bypassed to ground as close as possible to the amplifier pins. Surface mount 0.1µF capacitors will provide the best performance for local bypassing. Johanson 0.1µF capacitors (part number 250R18B104ZP4W) are used on the OPA628 demonstration board. All power supply bypass capacitors should be low impedance designs and should be located on the primary ground plane side of the PC board for the lowest impedance connection to ground. Properly bypassed and modulation free power supply lines allow optimum amplifier performance.
5. The OPA628 should be soldered directly into the PC board for best performance.



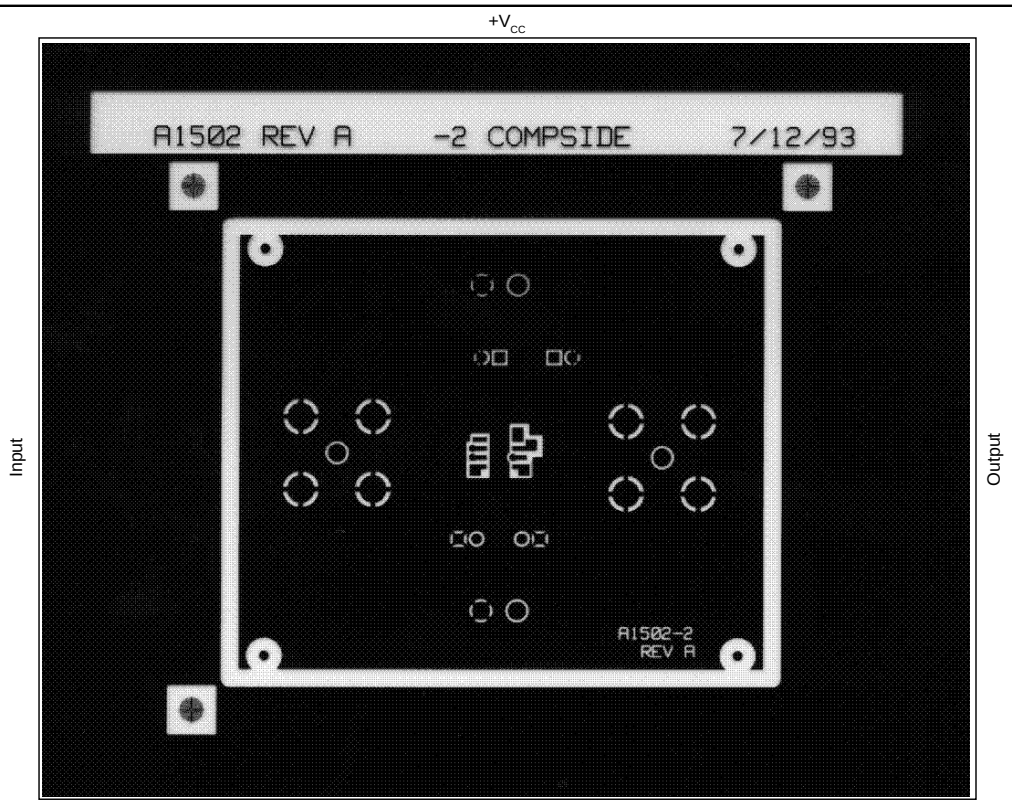
Top-side and Primary Ground-plane



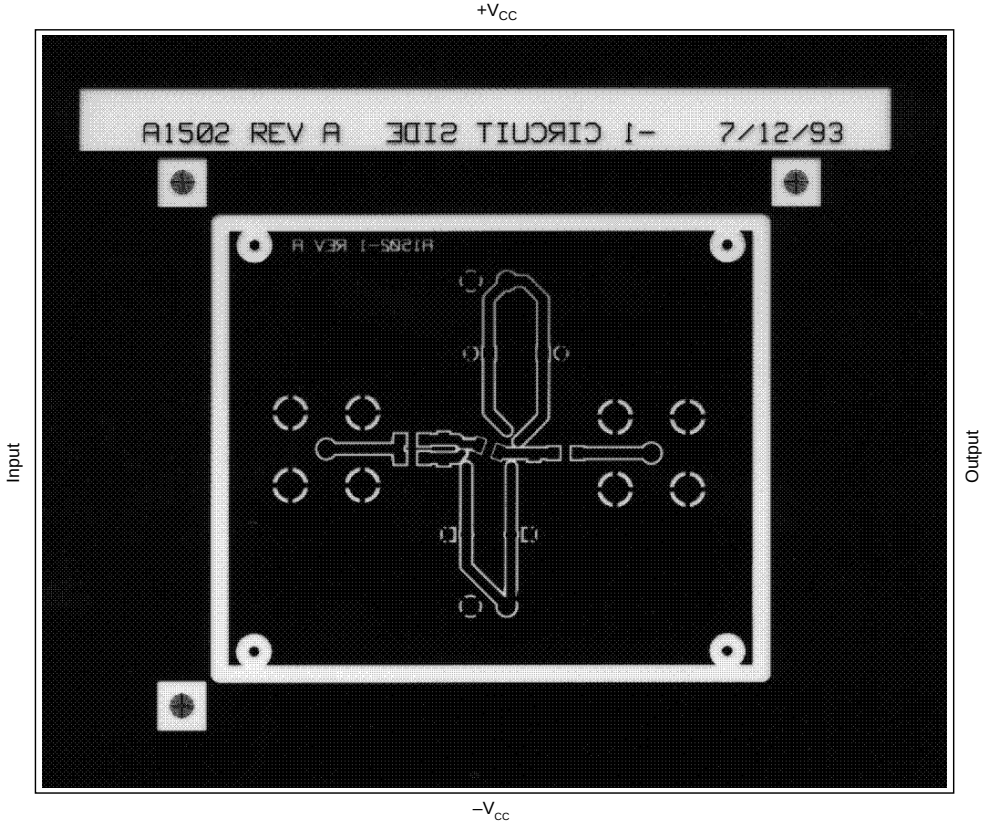
Bottom (as seen through board)

NOTES: (1) Pin 1 designated by rectangular pad. (2) DUT inserted Top-side. (3) Power supply by-pass caps installed at pin locations on Top-side. (4) All unused area on both sides connected to primary ground-plane. (5) Continue ground-plane under DUT both sides.

FIGURE 10a. Conceptual PCB Layout (8-pin DIP).



Top-side and Primary Ground-plane



Bottom (as seen through board)

NOTES: (1) Pad 1 designated by smallest rectangle. (2) DUT installed Top-side. (3) Power supply bypass caps installed at pad locations on Top-side. (4) All unused area on both sides connected to primary ground-plane. (5) Continue ground-plane under DUT both sides.

FIGURE 10b. Conceptual PCB Layout (8-pin SOIC).

APPLICATIONS

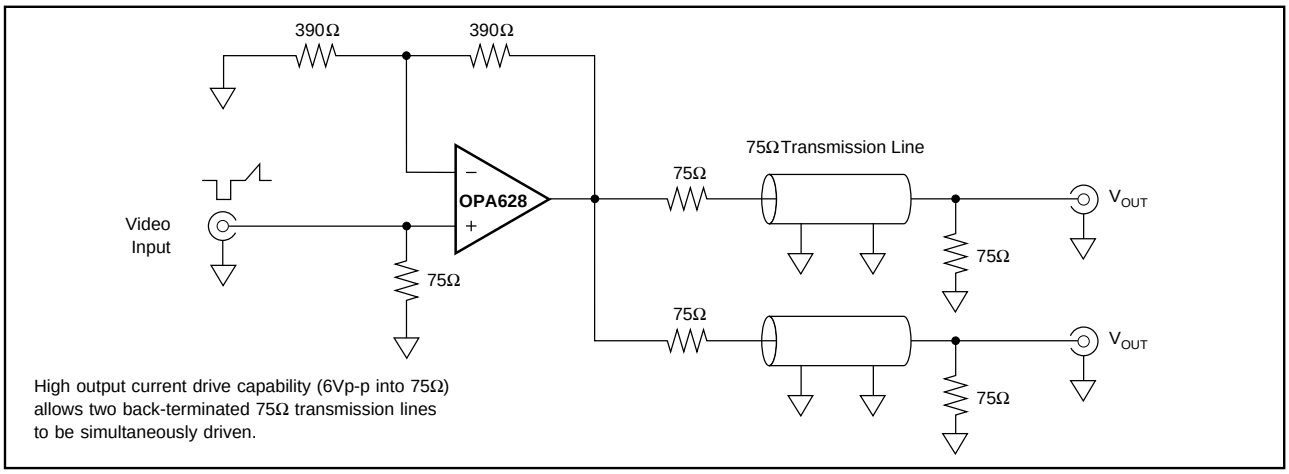
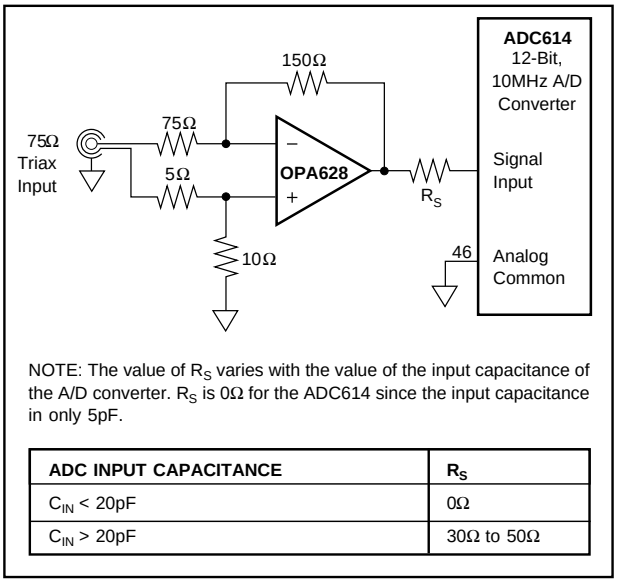


FIGURE 11. Video Distribution Amplifier.



NOTE: The value of R_S varies with the value of the input capacitance of the A/D converter. R_S is 0Ω for the ADC614 since the input capacitance in only 5pF.

ADC INPUT CAPACITANCE	R_S
C_{IN} < 20pF	0Ω
C_{IN} > 20pF	30Ω to 50Ω

FIGURE 12. Differential Input Buffer Amplifier (G = 2V/V).

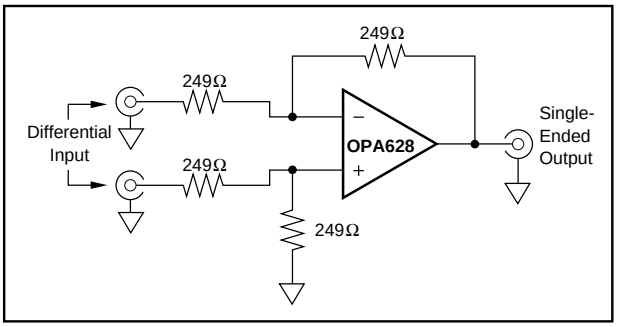
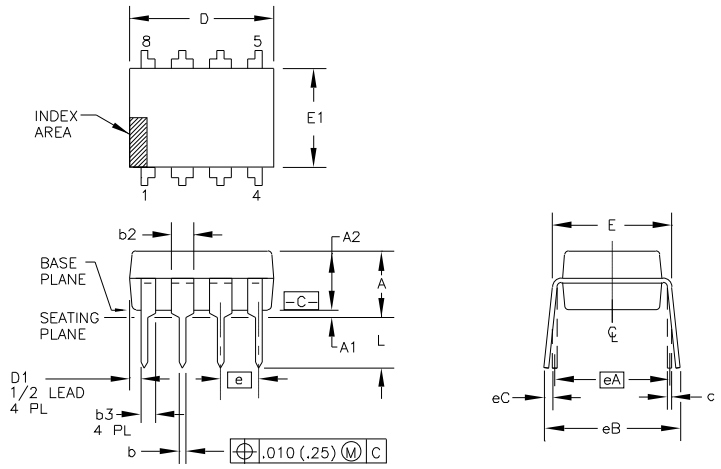


FIGURE 13. Low Distortion Unity Gain Difference Amplifier.

PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



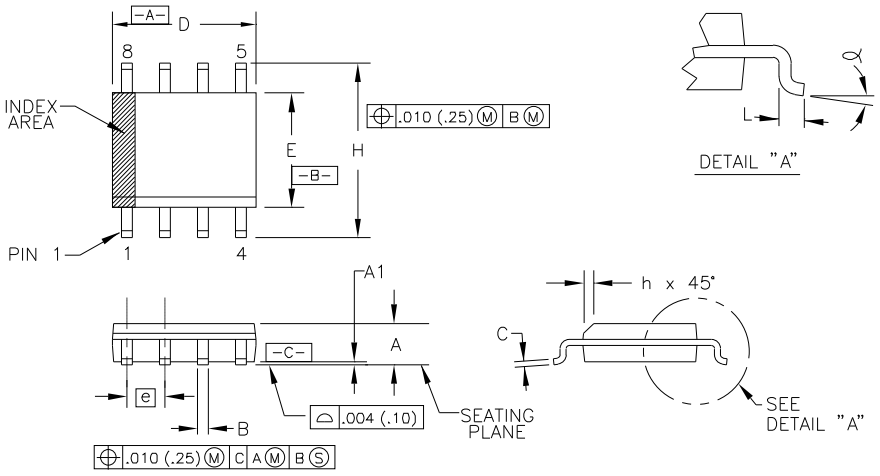
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C- .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006	REV.: E
JEDEC NUMBER: MS-001-BA	

Package Number 182 - 8-Lead SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050 BASIC		1.27 BASIC		
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	
L	.016	.050	0.41	1.27	5
N	8		8		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182	REV.: G
JEDEC NUMBER: MS-012-AA	