

**OPA627**  
**OPA637**

## Precision High-Speed *Difet*<sup>®</sup> OPERATIONAL AMPLIFIERS

### FEATURES

- VERY LOW NOISE:  $4.5\text{nV}/\sqrt{\text{Hz}}$  at 10kHz
- FAST SETTLING TIME:  
OPA627—550ns to 0.01%  
OPA637—450ns to 0.01%
- LOW  $V_{OS}$ : 100 $\mu\text{V}$  max
- LOW DRIFT: 0.8 $\mu\text{V}/^\circ\text{C}$  max
- LOW  $I_B$ : 5pA max
- OPA627: Unity-Gain Stable
- OPA637: Stable in Gain  $\geq 5$

### DESCRIPTION

The OPA627 and OPA637 *Difet* operational amplifiers provide a new level of performance in a precision FET op amp. When compared to the popular OPA111 op amp, the OPA627/637 has lower noise, lower offset voltage, and much higher speed. It is useful in a broad range of precision and high speed analog circuitry.

The OPA627/637 is fabricated on a high-speed, dielectrically-isolated complementary NPN/PNP process. It operates over a wide range of power supply voltage— $\pm 4.5\text{V}$  to  $\pm 18\text{V}$ . Laser-trimmed *Difet* input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

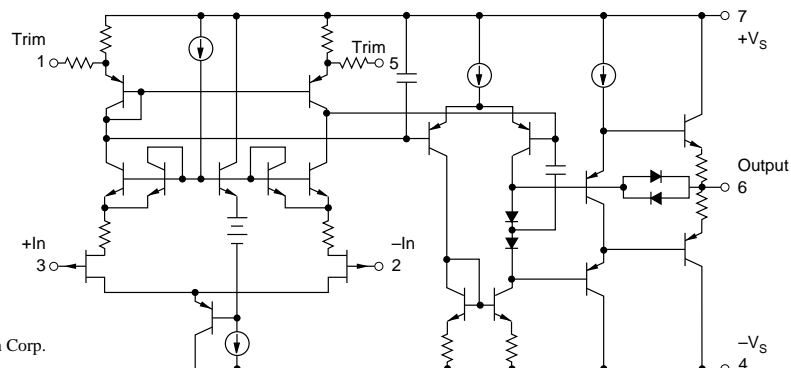
### APPLICATIONS

- PRECISION INSTRUMENTATION
- FAST DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- ACTIVE FILTERS

High frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than five.

*Difet* fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA627/637 is available in plastic DIP, SOIC and metal TO-99 packages. Industrial and military temperature range models are available.



*Difet*<sup>®</sup>, Burr-Brown Corp.

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# SPECIFICATIONS

## ELECTRICAL

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	OPA627BM, BP, SM OPA637BM, BP, SM			OPA627AM, AP, AU OPA637AM, AP, AU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> <sup>(1)</sup> Input Offset Voltage AP, BP, AU Grades Average Drift AP, BP, AU Grades Power Supply Rejection	$V_S = \pm 4.5$ to $\pm 18\text{V}$		40 100 0.4 0.8	100 250 0.8 2		130 280 1.2 2.5	250 500 2	$\mu\text{V}$ $\mu\text{V}$ $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$ dB
<b>INPUT BIAS CURRENT</b> <sup>(2)</sup> Input Bias Current Over Specified Temperature SM Grade Over Common-Mode Voltage Input Offset Current Over Specified Temperature SM Grade	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$ $V_{CM} = \pm 10\text{V}$ $V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		1 1 1 0.5	5 1 50 5 1 50		2 2 2 1	10 2	pA nA nA pA pA nA nA
<b>NOISE</b> Input Voltage Noise Noise Density: $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Voltage Noise, BW = 0.1Hz to 10Hz Input Bias Current Noise Noise Density, $f = 100\text{Hz}$ Current Noise, BW = 0.1Hz to 10Hz			15 8 5.2 4.5 0.6	40 20 8 6 1.6		20 10 5.6 4.8 0.8		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\mu\text{Vp-p}$ $\text{fA}/\sqrt{\text{Hz}}$ $\text{fA}/\text{p-p}$
<b>INPUT IMPEDANCE</b> Differential Common-Mode			$10^{13} \parallel 8$ $10^{13} \parallel 7$			*	*	$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Input Range Over Specified Temperature Common-Mode Rejection	$V_{CM} = \pm 10.5\text{V}$	$\pm 11$ $\pm 10.5$ 106	$\pm 11.5$ $\pm 11$ 116		*	*		V V dB
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain Over Specified Temperature SM Grade	$V_O = \pm 10\text{V}$ , $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$ , $R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$ , $R_L = 1\text{k}\Omega$	112 106 100	120 117 114		106 100	116 110		dB dB dB
<b>FREQUENCY RESPONSE</b> Slew Rate: OPA627 OPA637 Settling Time: OPA627 0.01% 0.1% OPA637 0.01% 0.1% Gain-Bandwidth Product: OPA627 OPA637 Total Harmonic Distortion + Noise	$G = -1$ , 10V Step $G = -4$ , 10V Step $G = -1$ , 10V Step $G = -1$ , 10V Step $G = -4$ , 10V Step $G = -4$ , 10V Step $G = 1$ $G = 10$ $G = +1$ , $f = 1\text{kHz}$	40 100	55 135 550 450 450 300 16 80 0.00003		*	*		V/ $\mu\text{s}$ V/ $\mu\text{s}$ ns ns ns ns MHz MHz %
<b>POWER SUPPLY</b> Specified Operating Voltage Operating Voltage Range Current		$\pm 4.5$	$\pm 15$ $\pm 7$	$\pm 18$ $\pm 7.5$	*	*	*	V V mA
<b>OUTPUT</b> Voltage Output Over Specified Temperature Current Output Short-Circuit Current Output Impedance, Open-Loop	$R_L = 1\text{k}\Omega$ $V_O = \pm 10\text{V}$ 1MHz	$\pm 11.5$ $\pm 11$ $\pm 35$	$\pm 12.3$ $\pm 11.5$ $\pm 45$ $+70/-55$ 55	$\pm 100$	*	*	*	V mA mA $\Omega$
<b>TEMPERATURE RANGE</b> Specification: AP, BP, AM, BM, AU SM Storage: AM, BM, SM AP, BP, AU $\theta_{JA}$ : AM, BM, SM AP, BP AU		-25 -55 -60 -40		+85 +125 +150 +125	*	*	*	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$

\* Specifications same as "B" grade.

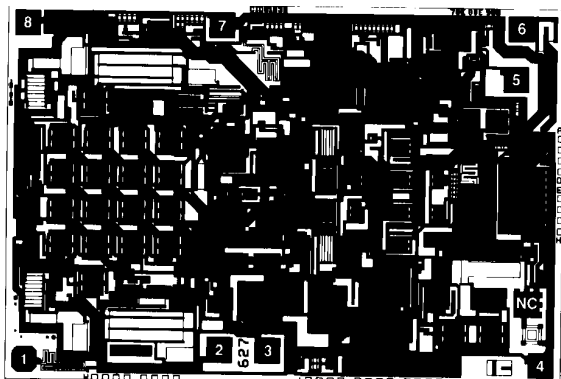
NOTES: (1) Offset voltage measured fully warmed-up. (2) High-speed test at  $T_J = +25^\circ\text{C}$ . See Typical Performance Curves for warmed-up performance.

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OPA627/637

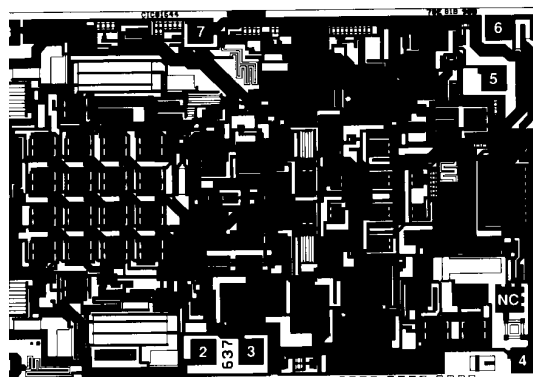
## DICE INFORMATION



OPA627 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Offset Trim	5	Offset Trim
2	-In	6	Output
3	+In	7	+V <sub>S</sub>
4	-V <sub>S</sub>	8	Substrate
		NC	No Connection

**Substrate Bias:** Dielectrically isolated. See data sheet for connection options.



OPA637 DIE TOPOGRAPHY

### MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	117 x 80 ±5	2.97 x 2.03 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count	46	
Backgating:	None	

## ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA627AP	Plastic DIP	-25°C to +85°C
OPA627BP	Plastic DIP	-25°C to +85°C
OPA627AU	SOIC	-25°C to +85°C
OPA627AM	TO-99 Metal	-25°C to +85°C
OPA627BM	TO-99 Metal	-25°C to +85°C
OPA627SM	TO-99 Metal	-55°C to +125°C
OPA637AP	Plastic DIP	-25°C to +85°C
OPA637BP	Plastic DIP	-25°C to +85°C
OPA637AU	SOIC	-25°C to +85°C
OPA637AM	TO-99 Metal	-25°C to +85°C
OPA637BM	TO-99 Metal	-25°C to +85°C
OPA637SM	TO-99 Metal	-55°C to +125°C

## ABSOLUTE MAXIMUM RATINGS

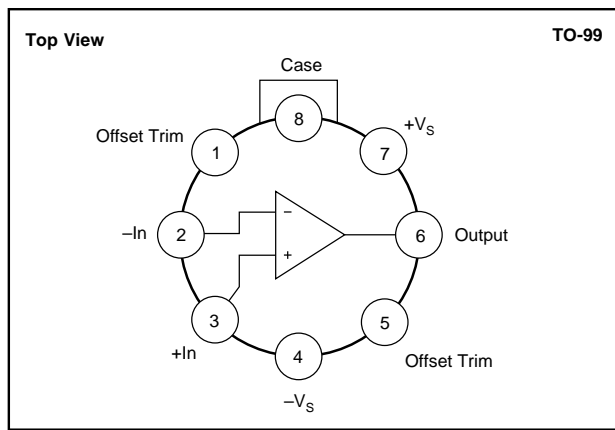
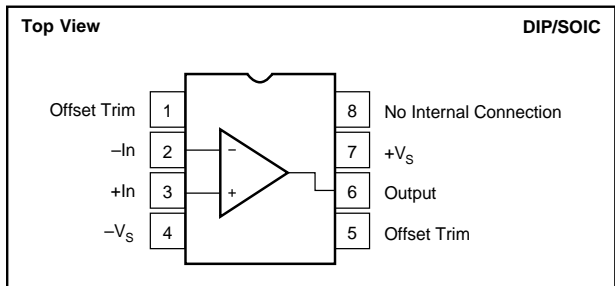
Supply Voltage .....	±18V
Input Voltage Range .....	+V <sub>S</sub> + 2V to -V <sub>S</sub> - 2V
Differential Input Range .....	Total V <sub>S</sub> + 4V
Power Dissipation .....	1000mW
Operating Temperature	
M Package .....	-55°C to +125°C
P, U Package .....	-40°C to +125°C
Storage Temperature	
M Package .....	-65°C to +150°C
P, U Package .....	-40°C to +125°C
Junction Temperature	
M Package .....	+175°C
P, U Package .....	+150°C
Lead Temperature (soldering, 10s) .....	+300°C
SOIC (soldering, 3s) .....	+260°C

## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
OPA627AP	Plastic DIP	006
OPA627BP	Plastic DIP	006
OPA627AU	SOIC	182
OPA627AM	TO-99 Metal	001
OPA627BM	TO-99 Metal	001
OPA627SM	TO-99 Metal	001
OPA637AP	Plastic DIP	006
OPA637BP	Plastic DIP	006
OPA637AU	SOIC	182
OPA637AM	TO-99 Metal	001
OPA637BM	TO-99 Metal	001
OPA637SM	TO-99 Metal	001

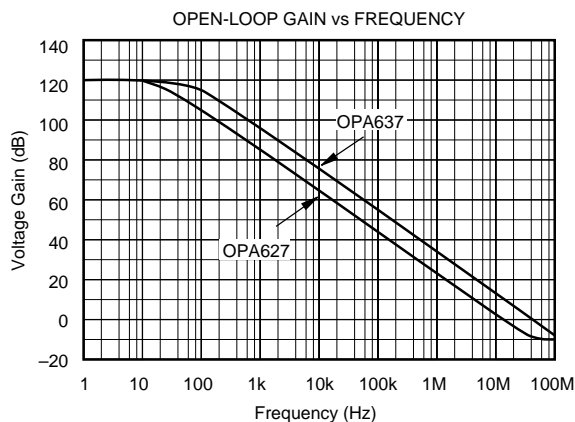
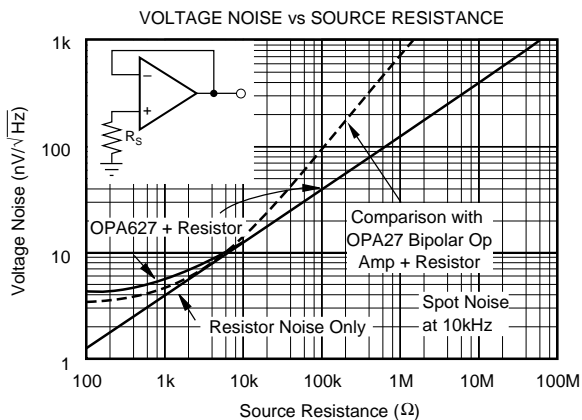
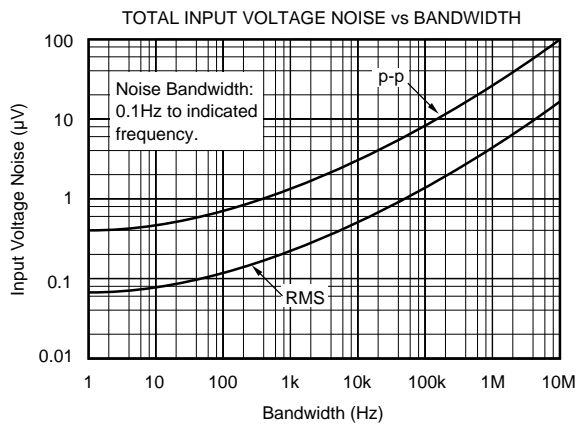
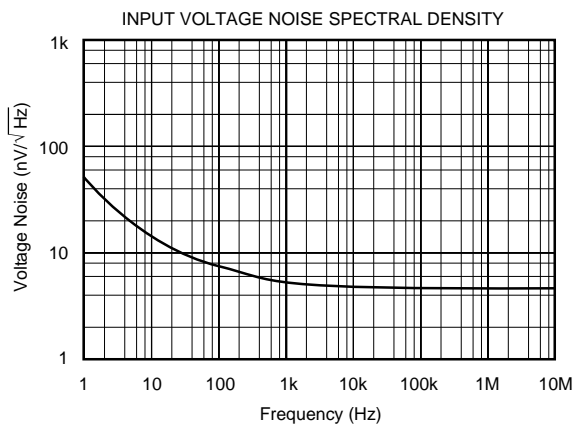
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## PIN CONFIGURATIONS



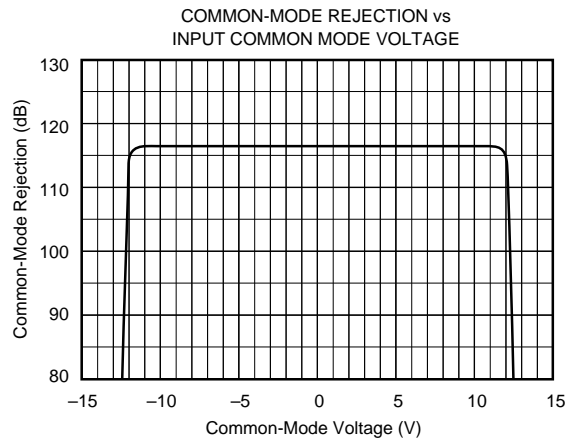
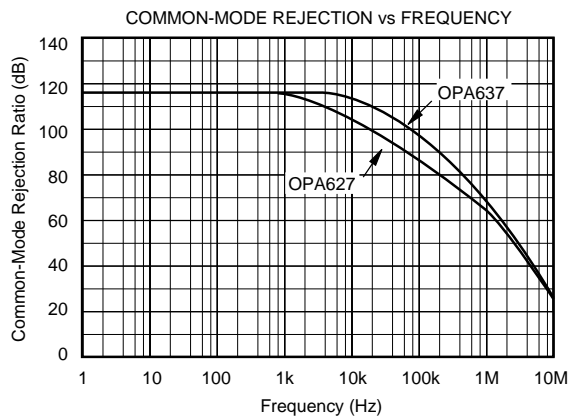
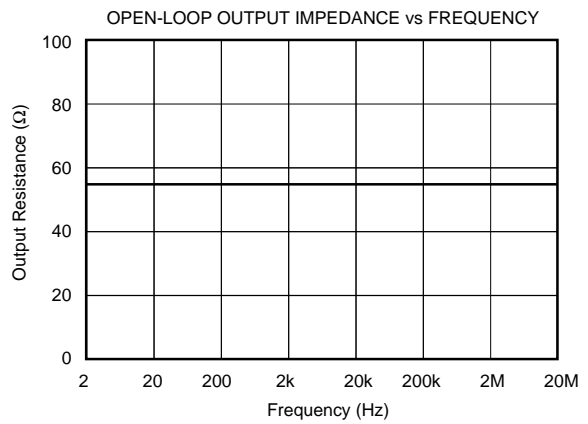
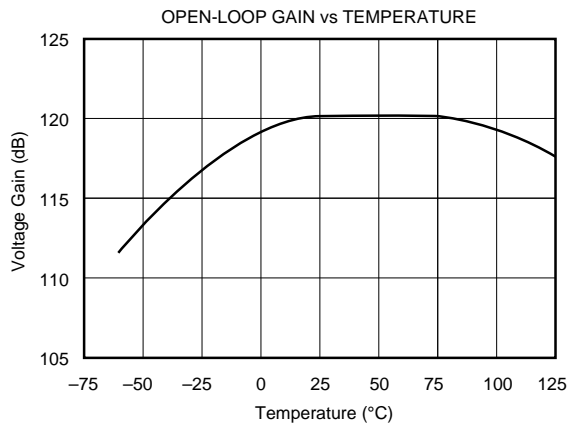
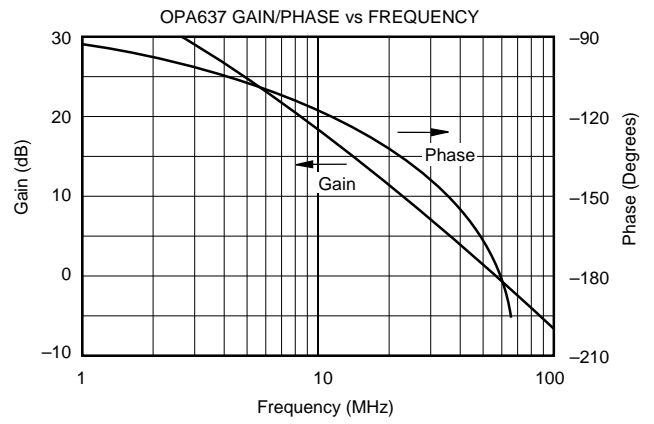
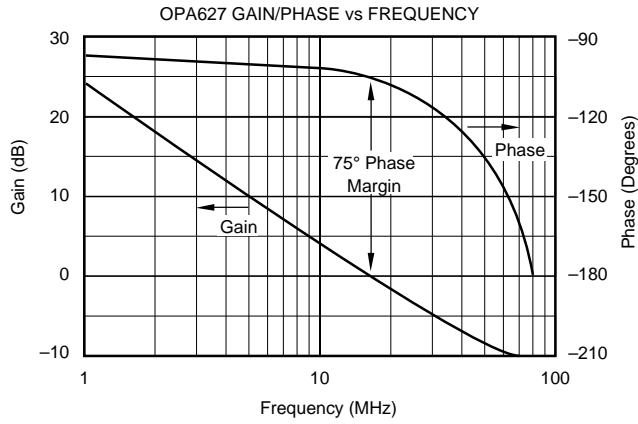
## TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



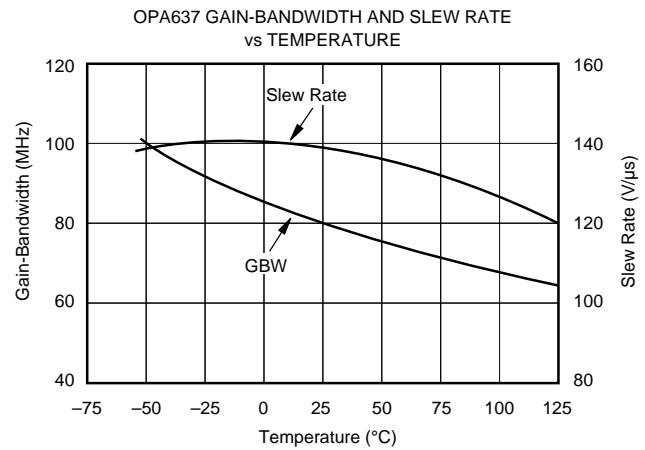
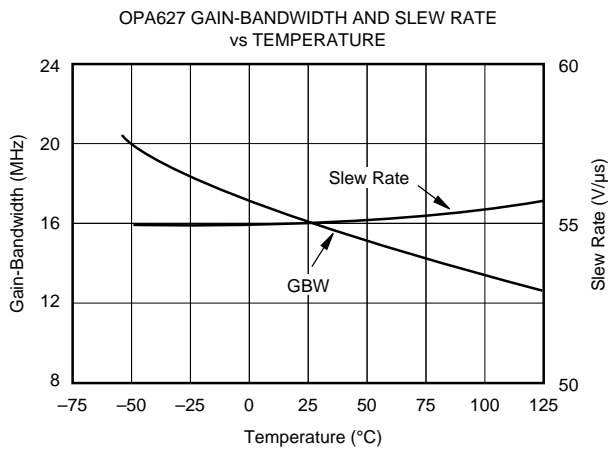
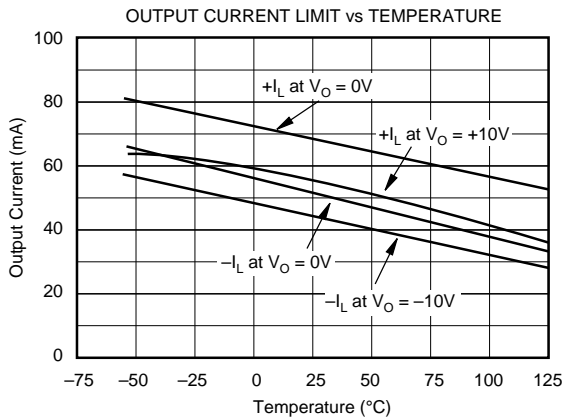
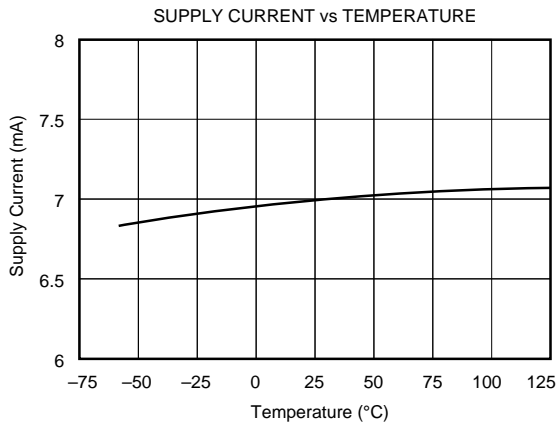
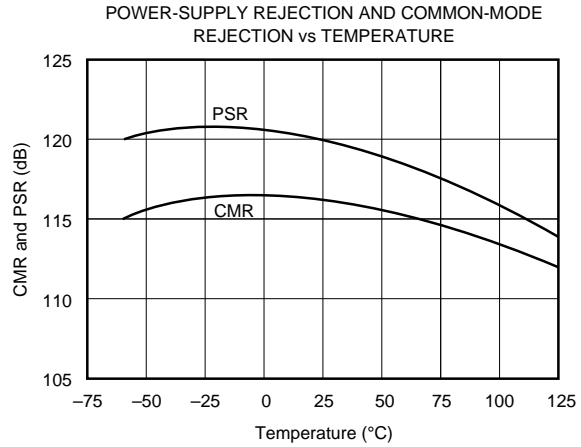
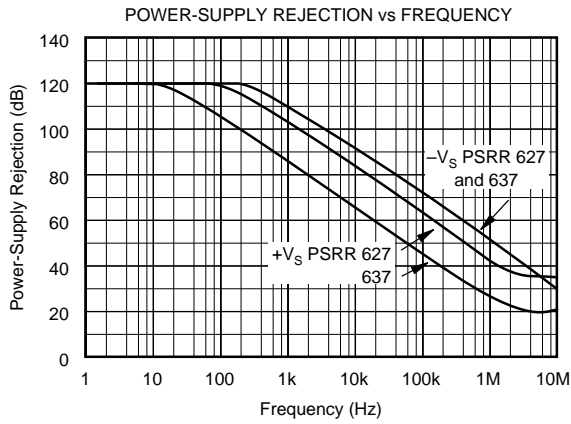
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



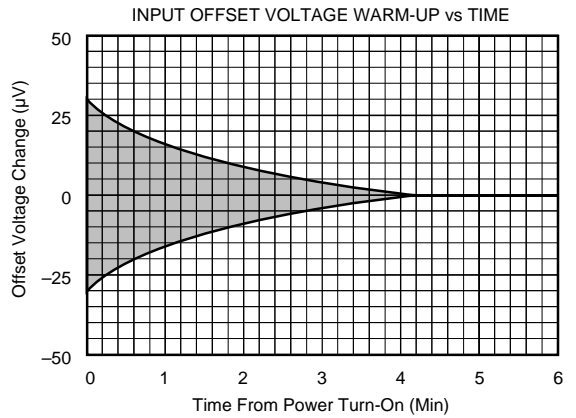
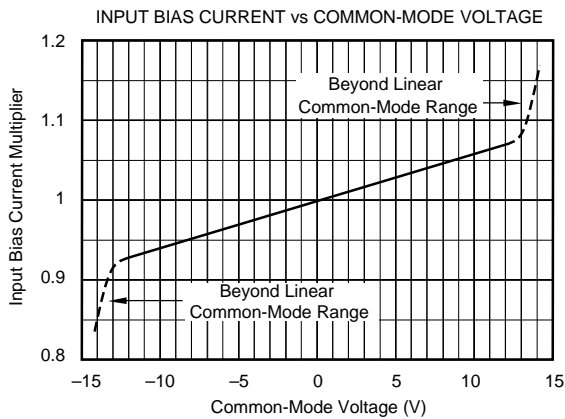
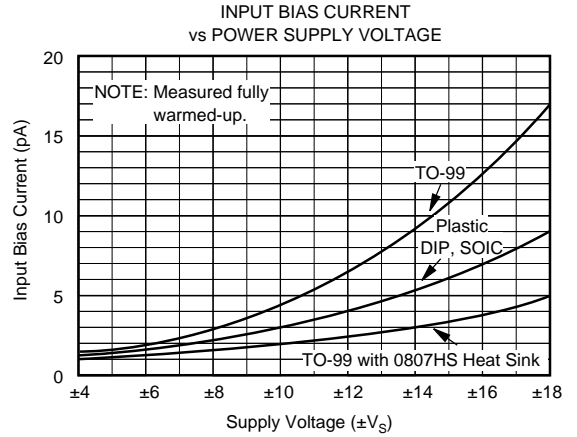
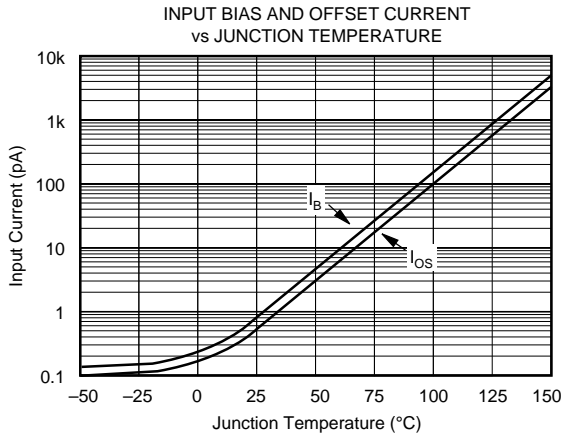
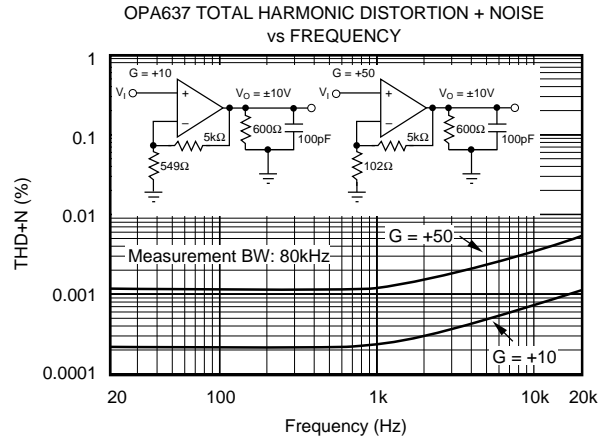
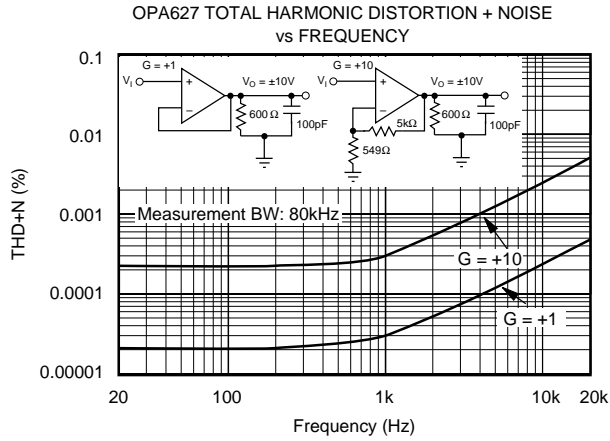
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



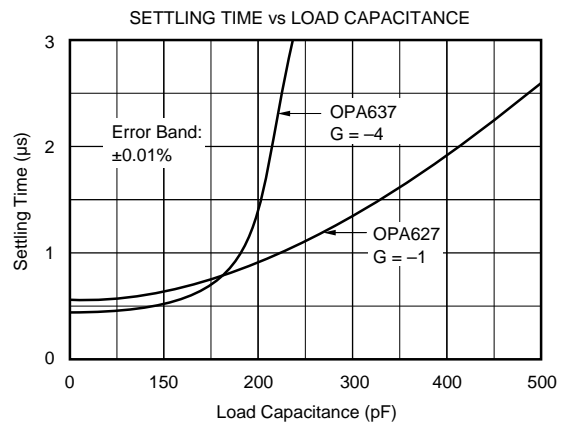
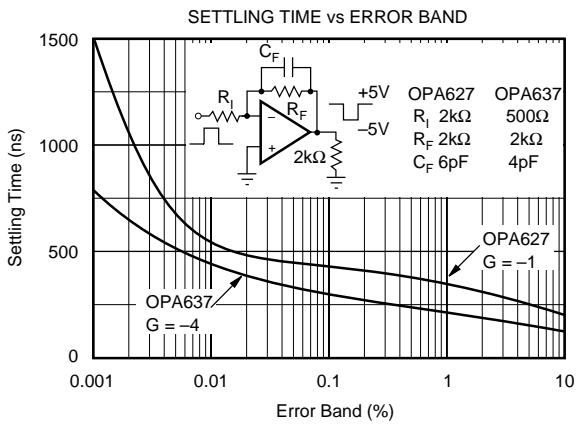
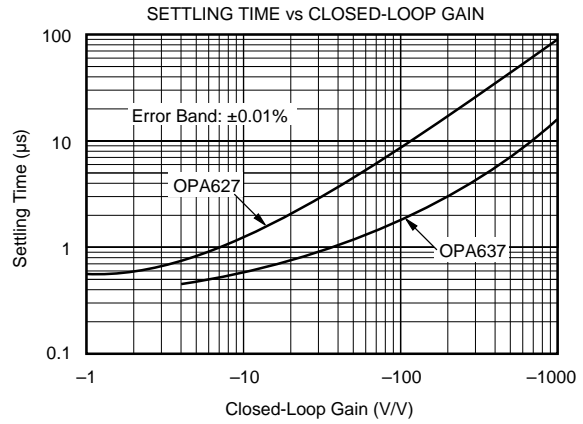
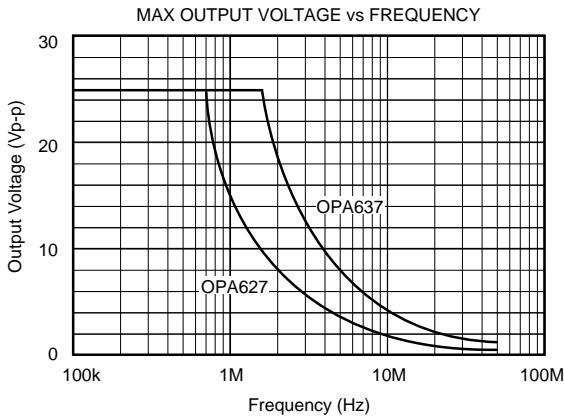
# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{V}$ , unless otherwise noted.



## APPLICATIONS INFORMATION

The OPA627 is unity-gain stable. The OPA637 may be used to achieve higher speed and bandwidth in circuits with noise gain greater than five. Noise gain refers to the closed-loop gain of a circuit as if the non-inverting op amp input were being driven. For example, the OPA637 may be used in a non-inverting amplifier with gain greater than five, or an inverting amplifier of gain greater than four.

When choosing between the OPA627 or OPA637, it is important to consider the high frequency noise gain of your circuit configuration. Circuits with a feedback capacitor (Figure 1) place the op amp in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 2, where a small feedback capacitance is used to compensate for the input capacitance at the op amp's inverting input. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to five or greater, the OPA637 may be used.

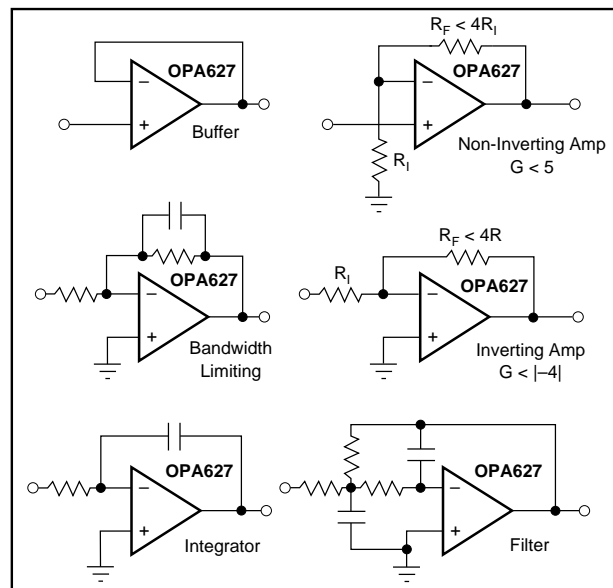


FIGURE 1. Circuits with Noise Gain Less than Five Require the OPA627 for Proper Stability.



## OFFSET VOLTAGE ADJUSTMENT

The OPA627/637 is laser-trimmed for low offset voltage and drift, so many circuits will not require external adjustment. Figure 3 shows the optional connection of an external potentiometer to adjust offset voltage. This adjustment should not be used to compensate for offsets created elsewhere in a system (such as in later amplification stages or in an A/D converter) because this could introduce excessive temperature drift. Generally, the offset drift will change by approximately  $4\mu\text{V}/^\circ\text{C}$  for 1mV of change in the offset voltage due to an offset adjustment (as shown on Figure 3).

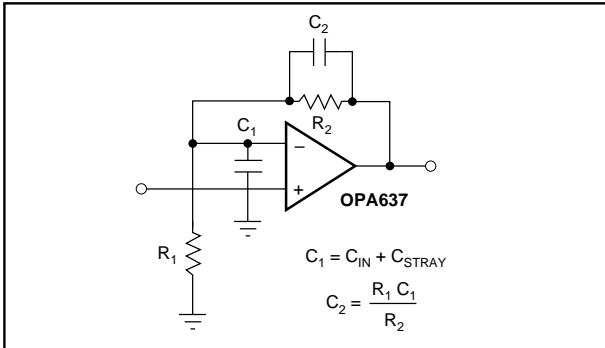


FIGURE 2. Circuits with Noise Gain Equal to or Greater than Five May Use the OPA637.

## NOISE PERFORMANCE

Some bipolar op amps may provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA627/637 is unique in providing very low voltage noise and very low current noise. This provides optimum noise performance over a wide range of sources, including reactive source impedances. This can be seen in the performance curve showing the noise of a source resistor combined with the

noise of an OPA627. Above a  $2\text{k}\Omega$  source resistance, the op amp contributes little additional noise. Below  $1\text{k}\Omega$ , op amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

## CIRCUIT LAYOUT

As with any high speed, wide bandwidth circuit, careful layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the input pins and feedback circuitry.

The case connection (pin 8 of TO-99 metal package only) should be connected to an AC ground for lowest possible pickup of external fields. While DC ground would be the most likely choice, pin 8 could also be connected to either power supply. (The case is not internally connected to the negative power supply as it is with most common op amps.) For lowest possible input bias current, the case may be driven as a guard—see Input Bias Current section. Pin 8 of the plastic DIP and SOIC versions has no internal connection.

Power supply connections should be bypassed with good high frequency capacitors positioned close to the op amp

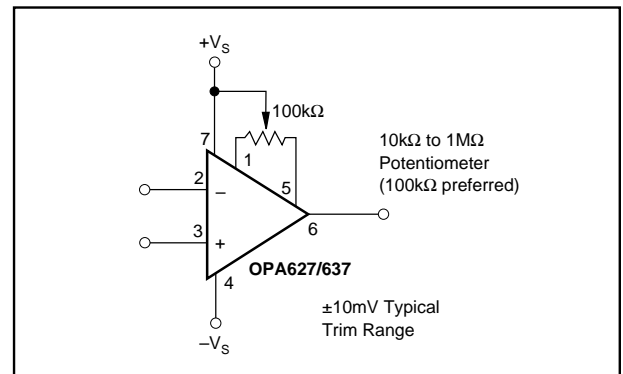


FIGURE 3. Optional Offset Voltage Trim Circuit.

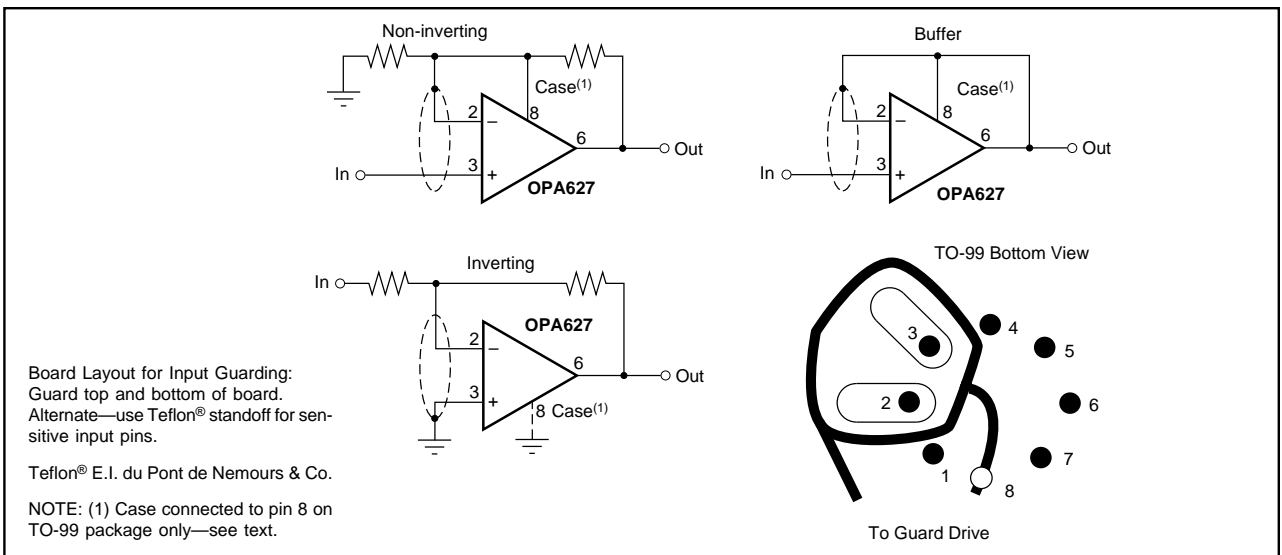


FIGURE 4. Connection of Input Guard for Lowest  $I_B$ .

pins. In most cases 0.1µF ceramic capacitors are adequate. The OPA627/637 is capable of high output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1µF solid tantalum capacitors may improve dynamic performance in these applications.

### INPUT BIAS CURRENT

**Difet** fabrication of the OPA627/637 provides very low input bias current. Since the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, the die temperature should be kept as low as possible. The high speed and therefore higher quiescent current of the OPA627/637 can lead to higher chip temperature. A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the  $I_B$  to one-third its warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects. See the data sheet on the 807HS for details.

Temperature rise in the plastic DIP and SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces will also help dissipate heat.

The OPA627/637 may also be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using ±5V power supplies reduces power dissipation to one-third of that at ±15V. This reduces the  $I_B$  of TO-99 metal package devices to approximately one-fourth the value at ±15V.

Leakage currents between printed circuit board traces can easily exceed the input bias current of the OPA627/637. A circuit board “guard” pattern (Figure 4) reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current will flow harmlessly to the low-impedance node. The case connection (TO-99 metal pack-

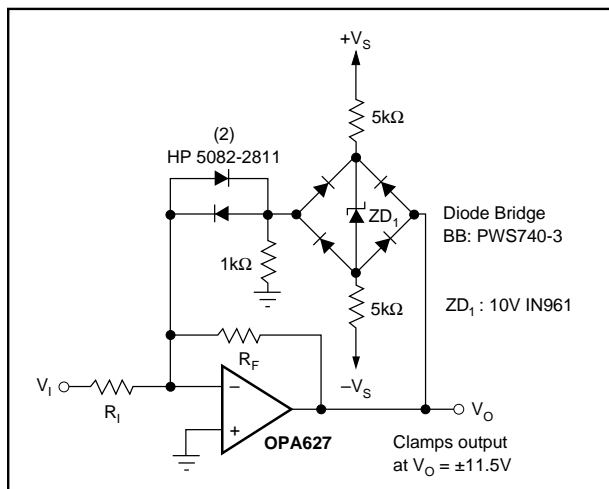


FIGURE 5. Clamp Circuit for Improved Overload Recovery.

age only) may also be driven at guard potential to minimize any leakage which might occur from the input pins to the case. The case is not internally connected to  $-V_S$ .

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be removed with cleaning solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at 85°C.

Many FET-input op amps exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA627/637 virtually constant with wide common-mode voltage changes. This is ideal for accurate high input-impedance buffer applications.

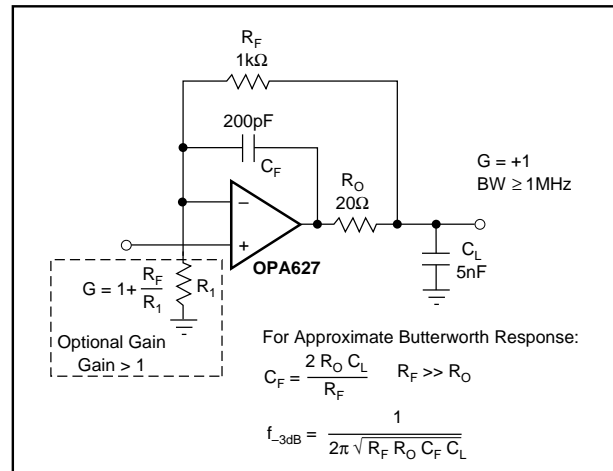


FIGURE 6. Driving Large Capacitive Loads.

### PHASE-REVERSAL PROTECTION

The OPA627/637 has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This is most often encountered in non-inverting circuits when the input is driven below  $-12V$ , causing the output to reverse into the positive rail. The input circuitry of the OPA627/637 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

### OUTPUT OVERLOAD

When the inputs to the OPA627/637 are overdriven, the output voltage of the OPA627/637 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6µs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 5. Diodes at the inverting input prevent degradation of input bias current.

## CAPACITIVE LOADS

As with any high-speed op amp, best dynamic performance can be achieved by minimizing the capacitive load. Since a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth of the OPA627 makes it the better choice for driving large capacitive loads. Figure 6 shows a circuit for driving very large load capacitance. This circuit's two-pole response can also be used to sharply limit system bandwidth. This is often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

## INPUT PROTECTION

The inputs of the OPA627/637 are protected for voltages between  $+V_s + 2V$  and  $-V_s - 2V$ . If the input voltage can exceed these limits, the amplifier should be protected. The diode clamps shown in Figure 7a will prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies—well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor,  $R_s$ , to limit the current. Be aware that adding resistance to the input will increase noise. The  $4nV/\sqrt{Hz}$  theoretical thermal noise of a  $1k\Omega$  resistor will add to the  $4.5nV/\sqrt{Hz}$  noise of the OPA627/637 (by the square-root of the sum of the squares), producing a total noise of  $6nV/\sqrt{Hz}$ . Resistors below  $100\Omega$  add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25nA—more than a thousand times larger than the input bias current of the OPA627/637. Leakage current of these diodes is typically much lower and may be adequate in many applications. Light falling on the

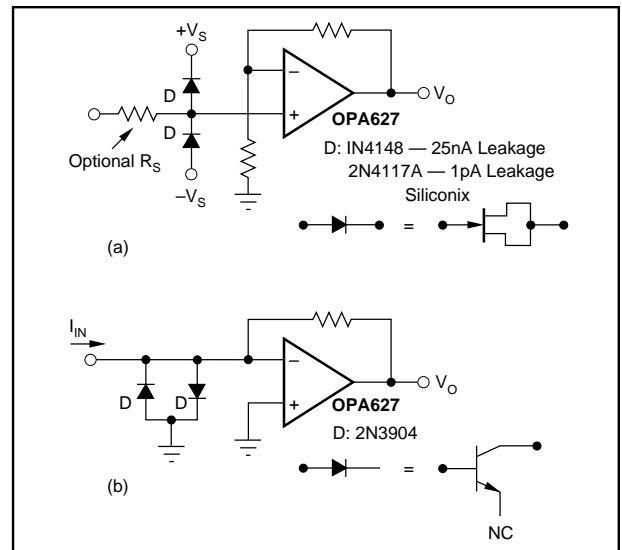


FIGURE 7. Input Protection Circuits.

junction of the protection diodes can dramatically increase leakage current, so common glass-packaged diodes should be shielded from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1pA and its metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers (Figure 7b). Although in normal operation, the voltage at the summing junction will be near zero (equal to the offset voltage of the amplifier), large input transients may cause this node to exceed 2V beyond the power supplies. In this case, the summing junction should be protected with diode clamps connected to ground. Even with the low voltage present at the summing junction, common signal diodes may have excessive leakage current. Since the reverse voltage on these diodes is clamped, a diode-connected signal transistor can be used as an inexpensive low leakage diode (Figure 7b).

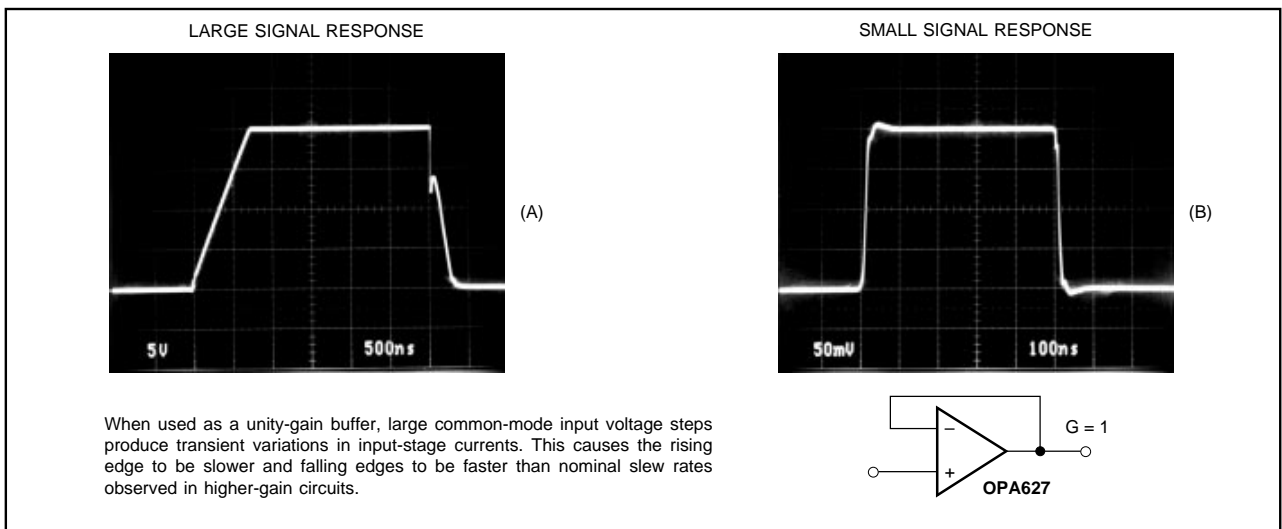


FIGURE 8. OPA627 Dynamic Performance,  $G = +1$ .

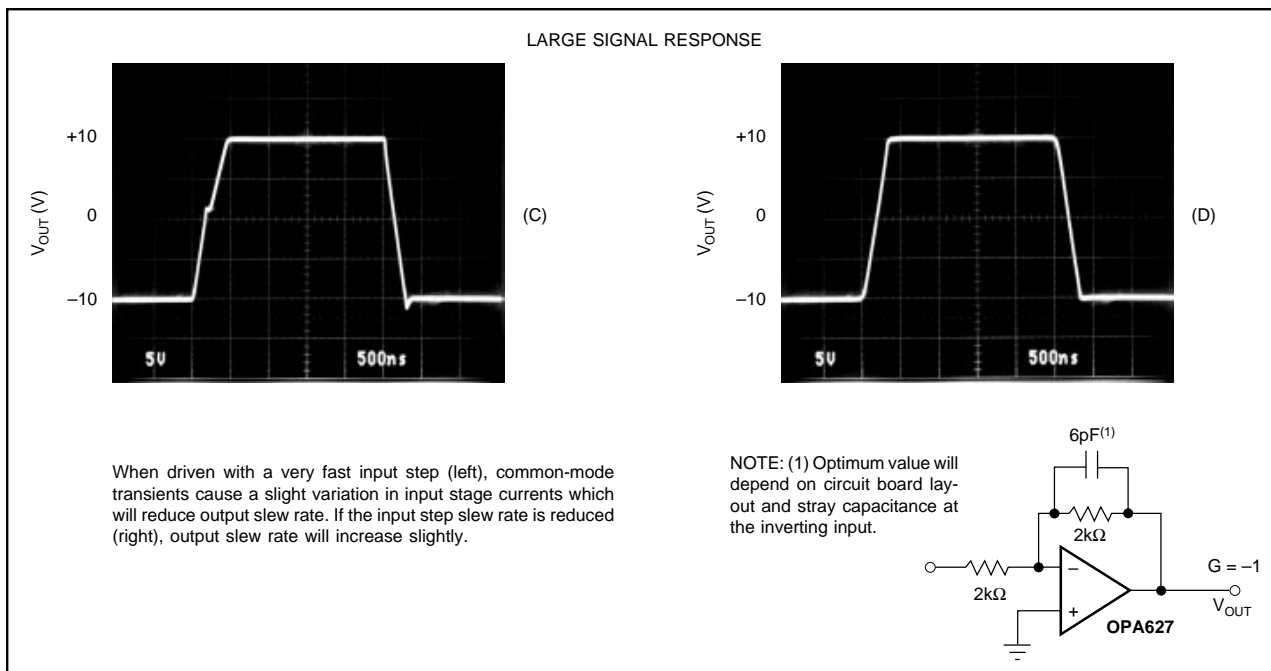


FIGURE 9. OPA627 Dynamic Performance,  $G = -1$ .

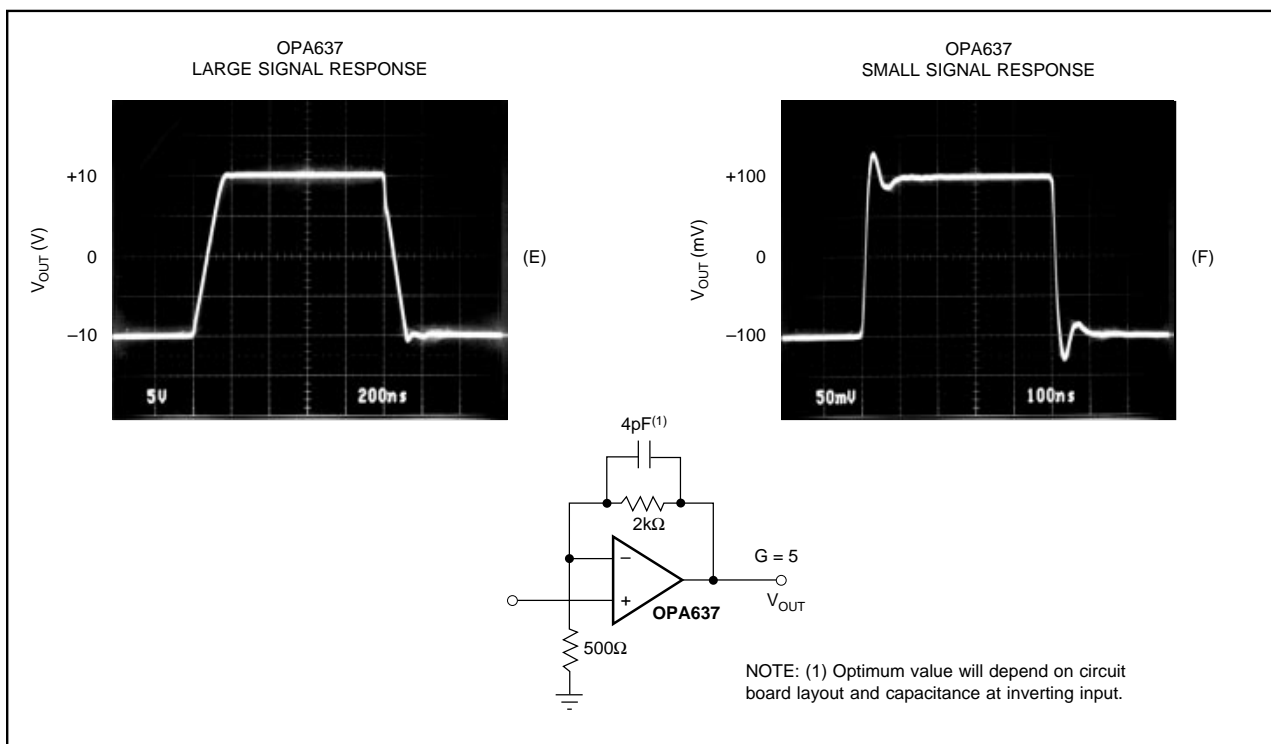


FIGURE 10. OPA637 Dynamic Response,  $G = 5$ .

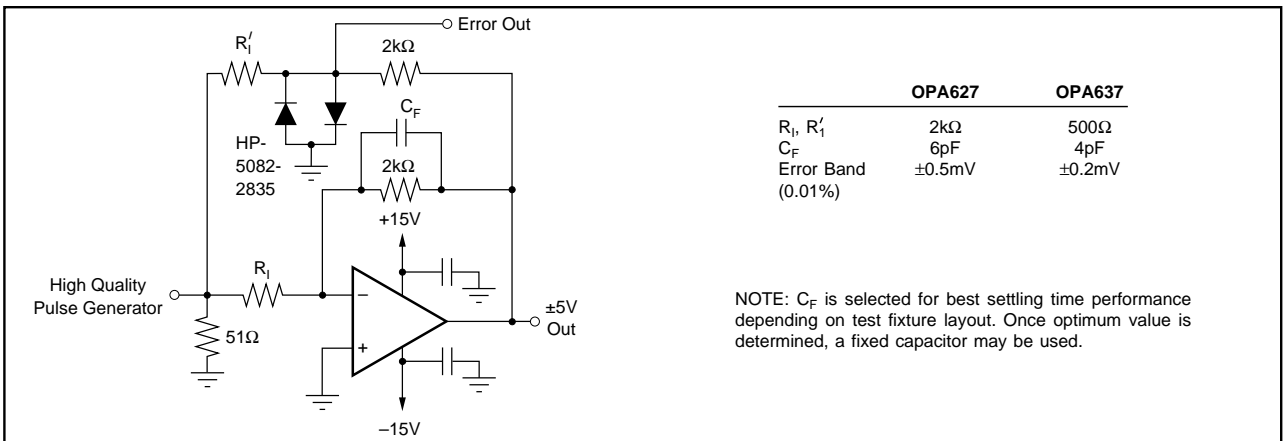


FIGURE 11. Settling Time and Slew Rate Test Circuit.

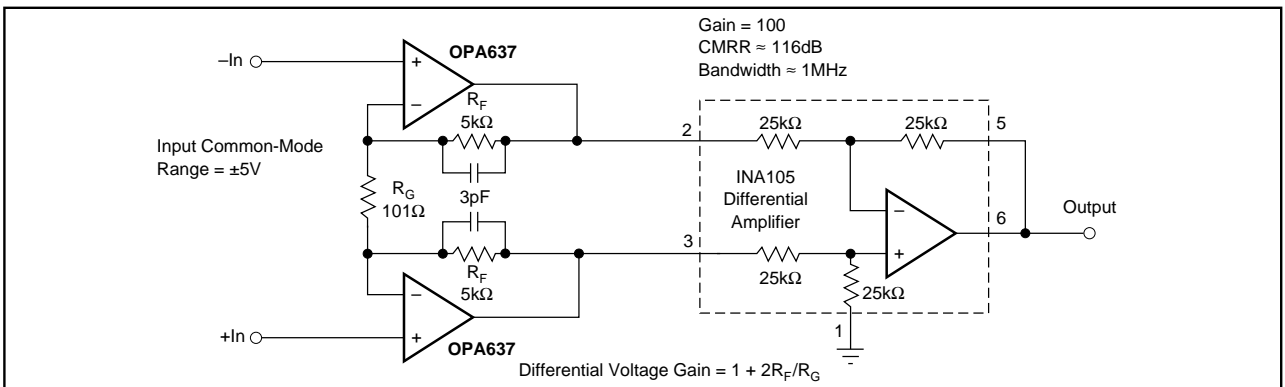


FIGURE 12. High Speed Instrumentation Amplifier, Gain = 100.

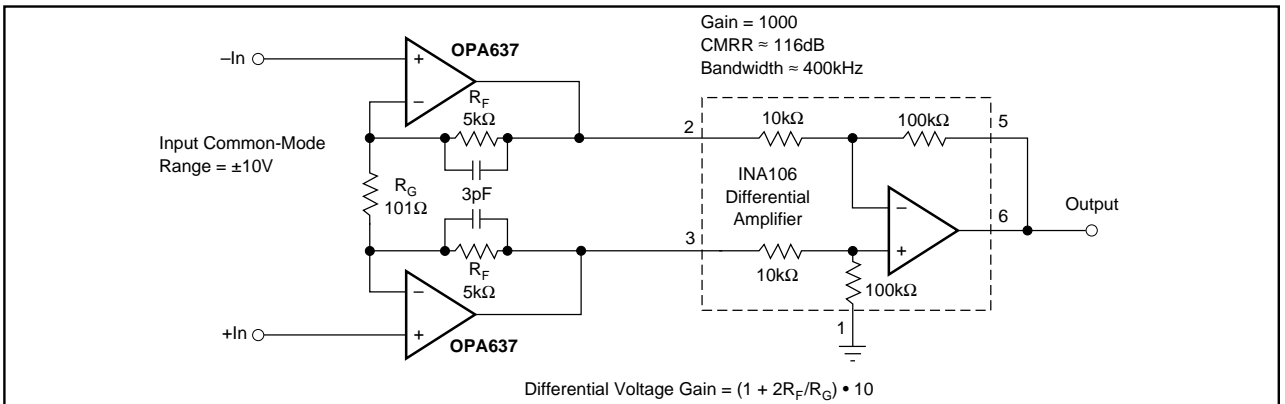


FIGURE 13. High Speed Instrumentation Amplifier, Gain = 1000.

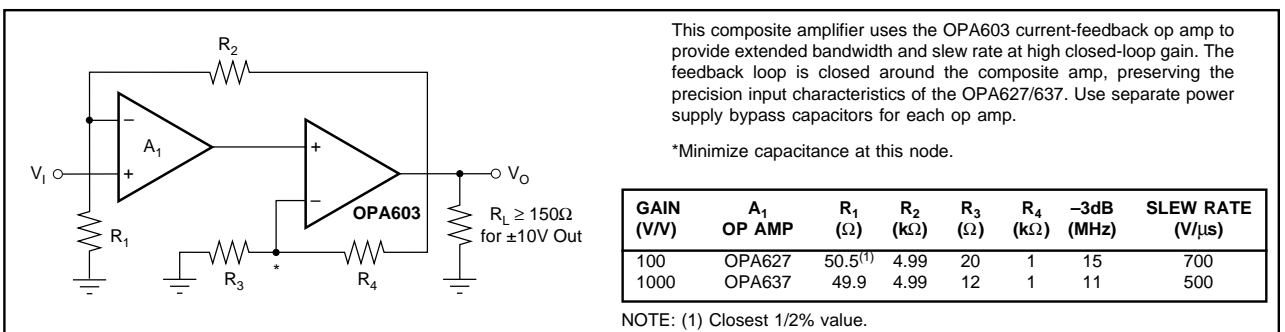
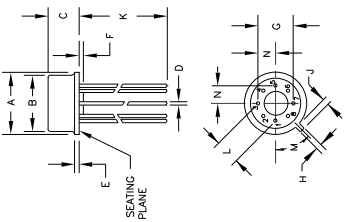


FIGURE 14. Composite Amplifier for Wide Bandwidth.

**PACKAGE DRAWINGS**

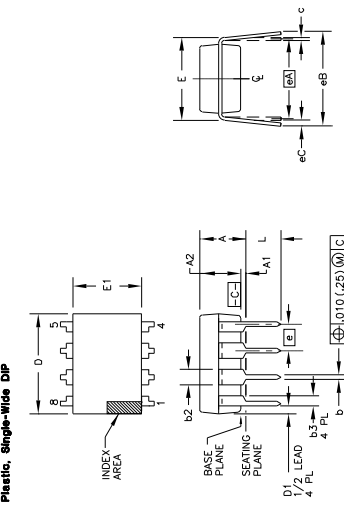
Package Number 001 - Metal TO-99



DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
A	.0532	0.0688	1.35	1.75	1	.000	.000	0.00	0.00	<p>NOTES:</p> <p>1. LEADS IN TRUE POSITION PER ANSI Y14.5M-1982. DIMENSIONS SHALL BE MEASURED AT SEATING PLANE.</p> <p>2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. DIMENSIONS MAY NOT BE MARKED ON PACKAGE.</p>
B	.013	.020	0.33	0.517	2	.000	.000	0.00	0.00	
C	.0075	0.0098	0.20	0.25	3	.000	.000	0.00	0.00	
D	.016	.021	0.41	0.53	4	.000	.000	0.00	0.00	
E	.010	.040	0.25	1.02	5	.000	.000	0.00	0.00	
F	.010	.040	0.25	1.02	6	.000	.000	0.00	0.00	
G	.0200	BASIC	5.08	BASIC	7	.000	.000	0.00	0.00	
H	.028	.034	0.71	0.86	8	.000	.000	0.00	0.00	
J	.029	.045	0.74	1.14	9	.000	.000	0.00	0.00	
K	.010	.060	2.59	4.06	10	.000	.000	0.00	0.00	
L	.010	.060	2.59	4.06	11	.000	.000	0.00	0.00	
M	.045	BASIC	4.43	BASIC	12	.000	.000	0.00	0.00	
N	.095	.105	2.41	2.67	13	.000	.000	0.00	0.00	

PACKAGE NUMBER: Z2001  
JEDEC NUMBER: UNKNOWN  
REV.: B

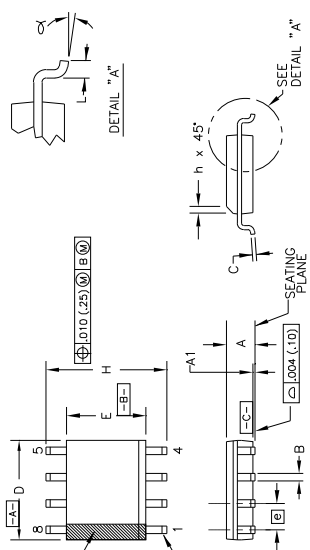
Package Number 006 - 8-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
A	.012	.015	0.30	0.38	1	.000	.000	0.00	0.00	<p>NOTES:</p> <p>1. ALL DIMENSIONS ARE IN INCHES. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M-1982. DIMENSIONS SHALL BE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3. DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. INTER-LEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 IN. (.254 mm).</p> <p>2. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE MEASURED AT SEATING PLANE.</p> <p>3. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.</p> <p>4. FOR AUTOMATIC INSERTION, ANY SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL CENTERLINE.</p> <p>5. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, THE CHAMFER SHALL BE .010 IN. (.254 mm).</p>
B	.014	.022	0.36	0.56	2	.000	.000	0.00	0.00	
C	.030	.045	0.76	1.14	3	.000	.000	0.00	0.00	
D	.008	.014	0.20	0.36	4	.000	.000	0.00	0.00	
E	.005	.007	0.13	0.18	5	.000	.000	0.00	0.00	
F	.005	.007	0.13	0.18	6	.000	.000	0.00	0.00	
G	.005	.007	0.13	0.18	7	.000	.000	0.00	0.00	
H	.005	.007	0.13	0.18	8	.000	.000	0.00	0.00	
I	.005	.007	0.13	0.18	9	.000	.000	0.00	0.00	
J	.005	.007	0.13	0.18	10	.000	.000	0.00	0.00	
K	.005	.007	0.13	0.18	11	.000	.000	0.00	0.00	
L	.005	.007	0.13	0.18	12	.000	.000	0.00	0.00	
M	.005	.007	0.13	0.18	13	.000	.000	0.00	0.00	
N	.005	.007	0.13	0.18	14	.000	.000	0.00	0.00	

PACKAGE NUMBER: Z2006  
JEDEC NUMBER: MS-001-BA  
REV.: E

Package Number 182 - 8-Lead SOIC



DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.		MIN.	MAX.	MIN.	MAX.	
A	.0532	0.0688	1.35	1.75	1	.000	.000	0.00	0.00	<p>NOTES:</p> <p>1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.</p> <p>2. DIMENSION "D" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (.15 mm) PER SIDE.</p> <p>3. INTER-LEAD FLASH OR PROTRUSIONS, INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (.254 mm) PER SIDE.</p> <p>4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, THE CHAMFER SHALL BE .010 IN. (.254 mm).</p>
B	.013	.020	0.33	0.517	2	.000	.000	0.00	0.00	
C	.0075	0.0098	0.20	0.25	3	.000	.000	0.00	0.00	
D	.016	.021	0.41	0.53	4	.000	.000	0.00	0.00	
E	.010	.040	0.25	1.02	5	.000	.000	0.00	0.00	
F	.010	.040	0.25	1.02	6	.000	.000	0.00	0.00	
G	.0200	BASIC	5.08	BASIC	7	.000	.000	0.00	0.00	
H	.028	.034	0.71	0.86	8	.000	.000	0.00	0.00	
I	.029	.045	0.74	1.14	9	.000	.000	0.00	0.00	
J	.010	.060	2.59	4.06	10	.000	.000	0.00	0.00	
K	.010	.060	2.59	4.06	11	.000	.000	0.00	0.00	
L	.010	.060	2.59	4.06	12	.000	.000	0.00	0.00	
M	.045	BASIC	4.43	BASIC	13	.000	.000	0.00	0.00	
N	.095	.105	2.41	2.67	14	.000	.000	0.00	0.00	

PACKAGE NUMBER: Z2182  
JEDEC NUMBER: MS-012-AA  
REV.: C