

# OPA623

## Wide Bandwidth, Current-Feedback OPERATIONAL AMPLIFIER

### FEATURES

- BANDWIDTH: 350MHz, 2.8Vp-p
- HIGH OUTPUT CURRENT:  $\pm 70\text{mA}$
- SLEW RATE:  $2100\text{V}/\mu\text{s}$ , 5Vp-p
- DIFFERENTIAL GAIN/PHASE: 0.12%/0.05°
- LOW QUIESCENT CURRENT:  $\pm 4\text{mA}$
- LOW INPUT BIAS CURRENT:  $1.2\mu\text{A}$
- RISE TIME: 1.9ns, 5Vp-p
- SETTLING TIME: 9ns, 0.1%

### DESCRIPTION

The OPA623 is a current-feedback operational amplifier designed for precision wide-bandwidth systems including high-resolution video, RF and IF circuitry, and communications equipment.

The new circuit design, together with the complementary bipolar process, achieves performance previously unattainable in monolithic integrated circuit technology.

The current-feedback op amp is optimized for wide bandwidth, excellent pulse response, gain flatness, low distortion, and operation at a low quiescent current of  $\pm 4\text{mA}$ .

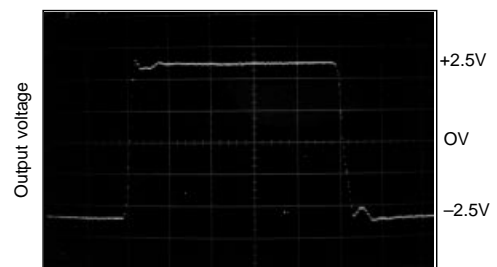
It provides a 350MHz large-signal bandwidth at 2.8Vp-p output voltage, as well as a  $2100\text{V}/\mu\text{s}$  slew rate. The gain flatness of 0.05dB over a 30MHz bandwidth makes it suitable for HDTV designs. Another feature of the op amp is its high output current of  $\pm 70\text{mA}$ , enabling it to drive two back-terminated  $75\Omega$  cables when using the amplifier as a line driver in video routers, distribution amplifiers, and analog and digital communications equipment.

### APPLICATIONS

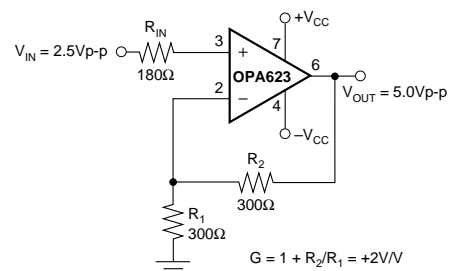
- BROADCAST/HDTV EQUIPMENT
- HIGH-SPEED DIGITAL COMMUNICATIONS
- PULSE/RF AMPLIFIERS
- HIGH-SPEED ANALOG SIGNAL PROCESSING
- LINE DRIVING ( $50\Omega$ ,  $75\Omega$ )
- DISTRIBUTION AMP
- CRT OUTPUT STAGE DRIVER
- ACTIVE FILTER

The OPA623 operates from a  $\pm 5\text{V}$  supply, is specified for the extended industrial temperature range ( $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ), and is available in 8-pin plastic SOIC and 8-pin plastic DIP.

LARGE SIGNAL PULSE RESPONSE



Output Voltage - 5Vp-p, 5ns/DIV



# SPECIFICATIONS

## DC-SPECIFICATION

At  $V_{CC} = \pm 5VDC$ ,  $I_O = \pm 4mA$ ,  $R_L = 100\Omega$ ,  $R_{IN} = 210\Omega$ , and  $T_{AMB} = +25^\circ C$  unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU			UNITS
		MIN	TYP	MAX	
<b>INPUT OFFSET VOLTAGE</b> Initial vs Temperature vs Supply (tracking) vs Supply (non-tracking) vs Supply (non-tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$ $V_{CC} = +4.5V$ to $+5.5V$ $V_{CC} = -4.5V$ to $-5.5V$	45	-8 125 50 47 39	$\pm 25$	mV $\mu V/^\circ C$ dB dB dB
<b>+INPUT BIAS CURRENT</b> Initial vs Temperature			-1.2 7	$\pm 4$	$\mu A$ nA/ $^\circ C$
<b>-INPUT BIAS CURRENT</b> Initial vs Temperature			+4.5 340	$\pm 20$	$\mu A$ nA/ $^\circ C$
<b>INPUT IMPEDANCE</b> +Input			2.74    1		M $\Omega$    pF
<b>INPUT NOISE</b> Voltage Noise Density Signal-to-Noise Ratio	f = 100kHz to 100MHz S/N = $0.7/(V_n \cdot \sqrt{5MHz})$		10 89		nV/ $\sqrt{Hz}$ dB
<b>INPUT VOLTAGE RANGE</b> Common-Mode Input Range Common-Mode Rejection		$\pm 3$ 43	$\pm 3.2$ 50		V dB
<b>RATED OUTPUT</b> Voltage Output Output Current Closed-Loop Output Impedance	$R_L = 100\Omega$ Gain = +2	$\pm 3$	$\pm 3.1$ $\pm 70$ 0.12    1.5		V mA $\Omega$    pF
<b>POWER SUPPLY</b> Rated Voltage Derated Performance Quiescent Current Rejection Ratio	$I_O = 0mA$	$\pm 4.5$ $\pm 4$ $\pm 3.5$ 45	$\pm 4$ 50	$\pm 5.5$ $\pm 6$ $\pm 4.5$	VDC VDC mA dB

## ELECTRICAL (FULL TEMPERATURE RANGE, $-40^\circ C$ to $+85^\circ C$ )

At  $V_{CC} = \pm 5VDC$ ,  $I_O = \pm 4mA$ ,  $R_L = 100\Omega$ , and  $R_{IN} = 210\Omega$  unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU			UNITS
		MIN	TYP	MAX	
<b>INPUT OFFSET VOLTAGE</b>				$\pm 30$	mV
<b>BIAS CURRENT</b> +Input			-1.5	$\pm 5$	$\mu A$
<b>BIAS CURRENT</b> -Input			27	$\pm 50$	$\mu A$
<b>RATED OUTPUT</b> Voltage Output	$R_L = 100\Omega$	$\pm 3$	$\pm 3.1$		V
<b>POWER SUPPLY</b> Quiescent Current	$I_O = 0mA$	$\pm 2$	$\pm 4$	$\pm 7$	mA

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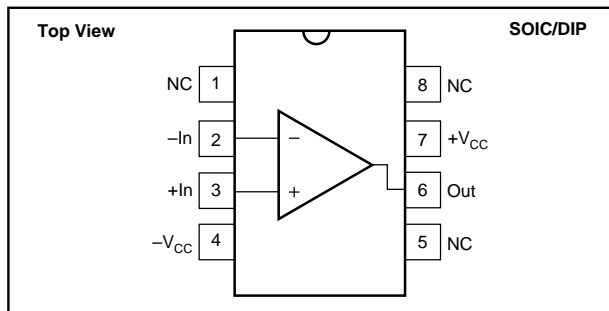
# SPECIFICATIONS

## AC-SPECIFICATION

At  $V_{CC} = \pm 5VDC$ ,  $I_Q = \pm 4mA$ ,  $R_L = 100\Omega$ ,  $R_{IN} = 210\Omega$ , and  $T_{AMB} = +25^\circ C$  unless otherwise specified.

PARAMETER	CONDITIONS	OPA623AP, AU			UNITS
		MIN	TYP	MAX	
<b>FREQUENCY DOMAIN</b>					
<b>Large Signal</b> Closed-Loop Bandwidth (-3dB)	$V_O = 2.8Vp-p$ , Gain = +1V/V		340		MHz
	$V_O = 2.8Vp-p$ , Gain = +2V/V		350		MHz
	$V_O = 2.8Vp-p$ , Gain = +5V/V		260		MHz
	$V_O = 2.8Vp-p$ , Gain = +10V/V		210		MHz
	$V_O = 2.8Vp-p$ , Gain = -1V/V		360		MHz
	$V_O = 2.8Vp-p$ , Gain = -2V/V		330		MHz
	$V_O = 5.0Vp-p$ , Gain = +2V/V		240		MHz
<b>SMALL SIGNAL BANDWIDTH</b>	$V_O = 0.2Vp-p$ , Gain = +2V/V		290		MHz
<b>GROUP DELAY TIME</b>	Pin 3 to Pin 6, Gain = +2V/V		1.2		ns
<b>DIFFERENTIAL GAIN</b>	G = +2V/V, f = 4.43MHz, $R_L = 150\Omega$ $V_O = +1.4V$		0.12		%
<b>DIFFERENTIAL PHASE</b>	G = +2V/V, f = 4.43MHz, $R_L = 150\Omega$ $V_O = +1.4V$		0.05		Degrees
<b>HARMONIC DISTORTION</b>	Gain = +2V/V				
	Second Harmonic f = 10MHz, $V_O = 2.0Vp-p$		-56		dBc
	Third Harmonic f = 30MHz, $V_O = 2.0Vp-p$		-59		dBc
	Second Harmonic f = 30MHz, $V_O = 2.0Vp-p$		-30		dBc
	Third Harmonic f = 50MHz, $V_O = 2.0Vp-p$		-37		dBc
<b>GAIN FLATNESS PEAKING</b>	Gain = +2V/V				
	$V_O = 2.0Vp-p$ , DC to 30MHz $V_O = 2.0Vp-p$ , DC to 100MHz		0.05 0.20		dB dB
<b>TIME DOMAIN</b>					
<b>Rise Time</b>	Gain = +2V/V, 10% to 90%				
	$V_O = 2.0Vp-p$ $V_O = 5.0Vp-p$		1.4 1.9		ns ns
<b>Fall Time</b>	Gain = +2V/V, 10% to 90%				
	$V_O = 2.0Vp-p$ $V_O = 5.0Vp-p$		1.4 2.6		ns ns
<b>SLEW RATE</b>	Gain = +2V/V, Rise Time = 1ns $V_O = 0.2Vp-p$ $V_O = 5.0Vp-p$		140 2100		V/ $\mu s$ V/ $\mu s$
<b>SETTLING TIME</b>	Gain = +2V/V, Rise Time = 2ns $V_O = 2Vp-p$ , 0.1%		9		ns

## PIN CONFIGURATION



## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
OPA623AP	Plastic DIP	006
OPA623AU	Plastic SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## ORDERING INFORMATION

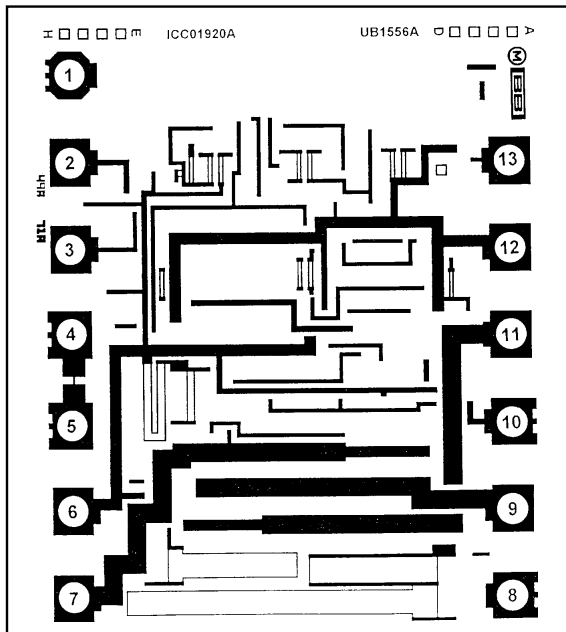
MODEL	PACKAGE	TEMPERATURE RANGE
OPA623AP	8-Pin Plastic DIP	-40°C to +85°C
OPA623AU	8-Pin SOIC	-40°C to +85°C

## ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±6V
Input Voltage <sup>(1)</sup>	±V <sub>CC</sub> ±0.7V
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Inputs are internally diode-clamped to ±V<sub>CC</sub>.

## DICE INFORMATION



OPA623 DIE TOPOGRAPHY

PAD	FUNCTION
1	NC
2	Inverting Input
3	Non-Inverting Input
4	NC
5	NC
6	-5V Supply
7	-5V Supply, Output
8	NC
9	Output
10	OTA Output
11	+5V Supply, Output
12	+5V Supply
13	NC

Substrate Bias: Negative Supply

NC: No Connection

Wire Bonding: Gold wire bonding is recommended.

## MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	57 x 69 ±5	1.44 x 1.76 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02 +0.05, -0.0	0.0005 +0.0013, -0.0
Gold	0.30 ±0.05	0.0076 ±0.0013

## INPUT PROTECTION

The need for protection from static damage has long been recognized for MOSFET devices, but all semiconductor devices deserve protection from this potentially damaging source. The OPA623 incorporates on-chip ESD protection diodes as shown in Figure 1. These diodes eliminate the need for external protection diodes, which can add capacitance and degrade AC performance.

As shown, all input pins of the OPA623 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur when the amplifier loses its power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To ensure long-term reliability, however, the diode current should be limited externally to approximately 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using the Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the amplifier input characteristics without necessarily destroying the device. In precision amplifiers, such changes may degrade offset and drift noticeably. For this reason, static protection is strongly recommended when handling the OPA623.

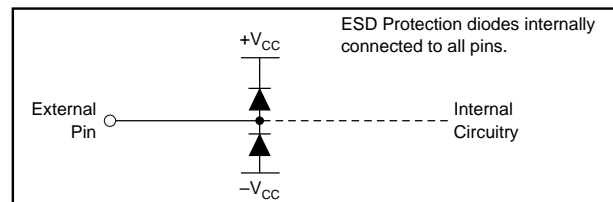
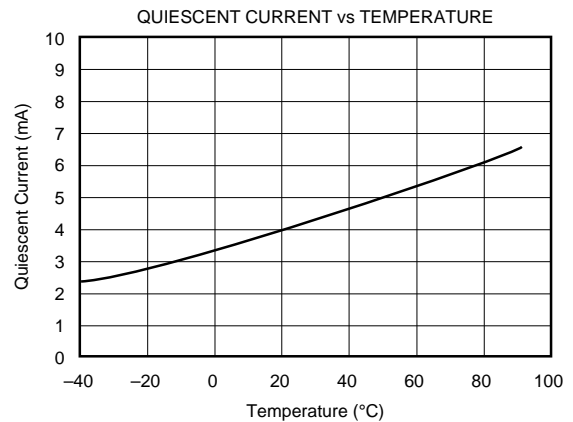
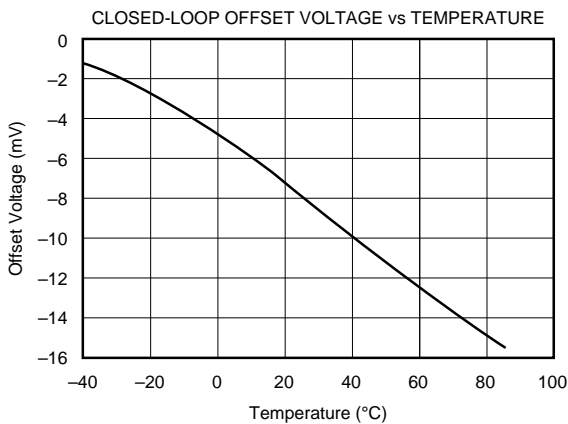
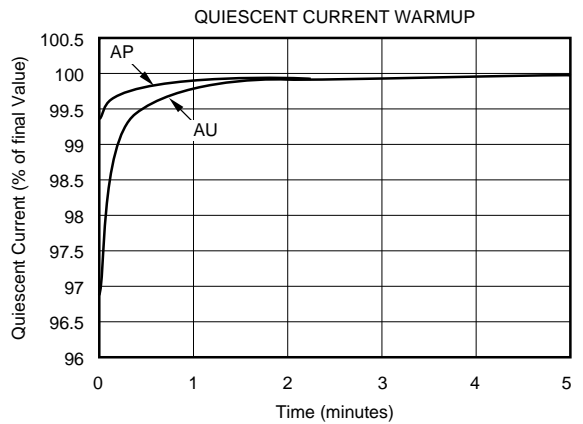
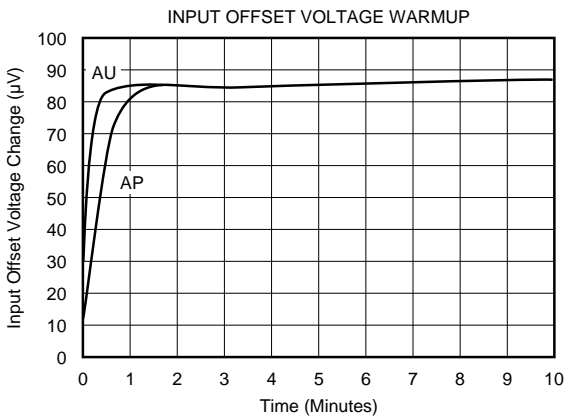
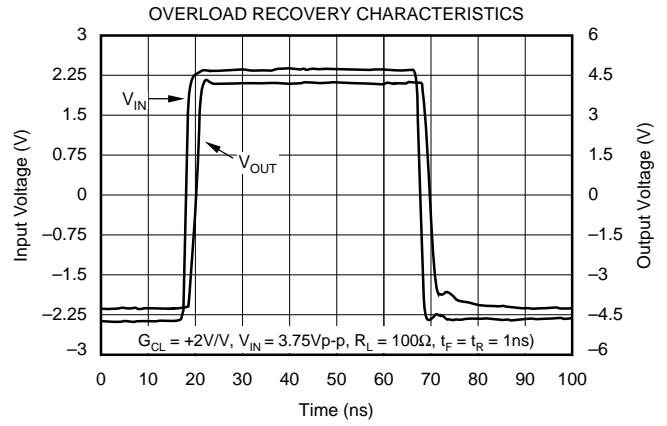
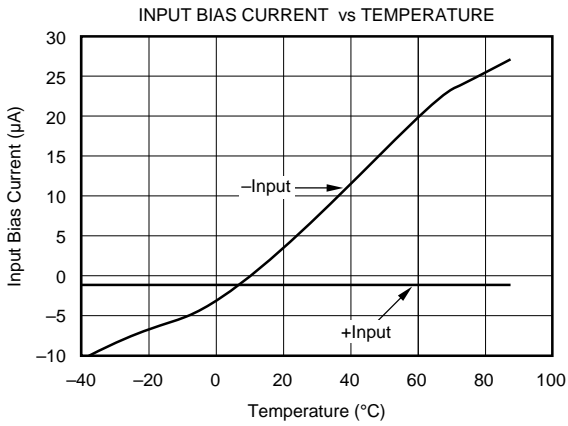


FIGURE 1. Internal ESD Protection.

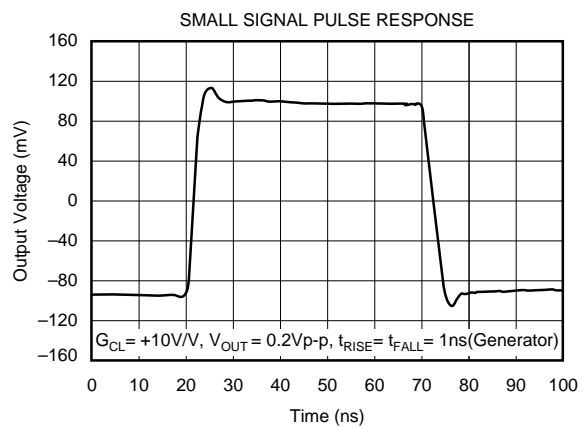
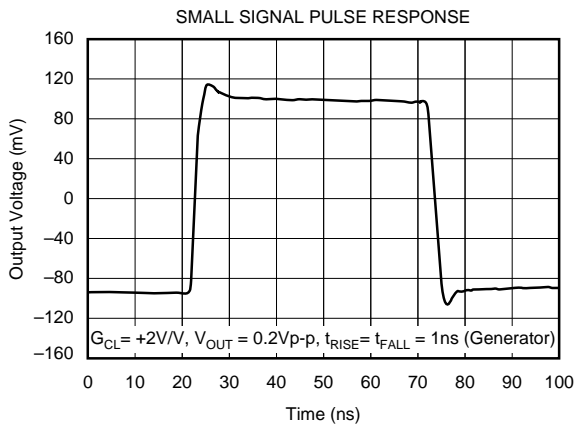
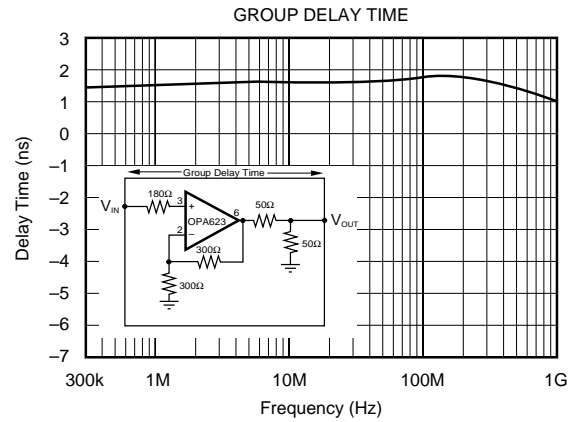
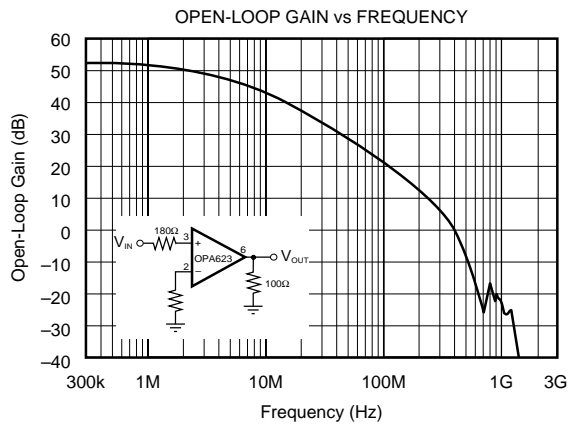
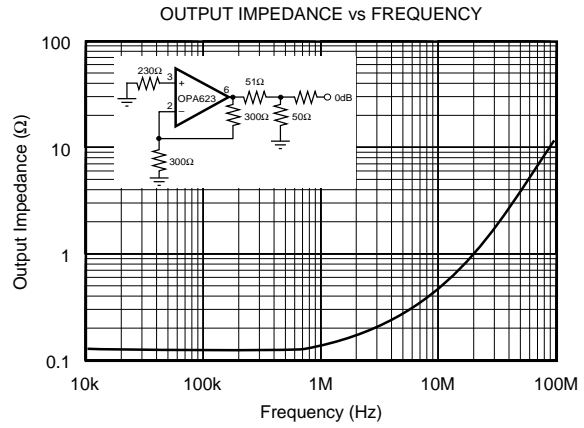
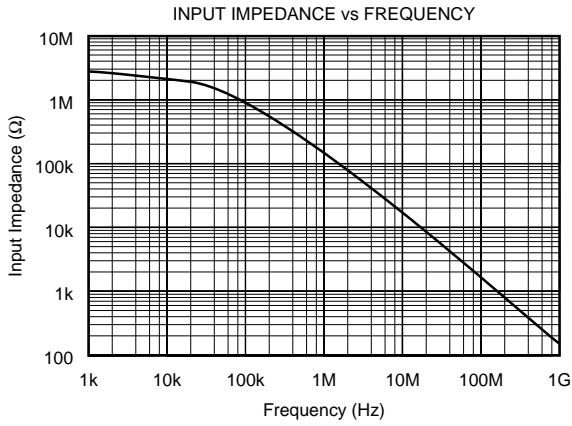
# TYPICAL PERFORMANCE CURVES

At  $V_{CC} = \pm 5VDC$ ,  $R_L = 100\Omega$ ,  $I_Q = \pm 4mA$ ,  $R_{IN} = 150\Omega$ , and  $T_{AMB} = +25^\circ C$  unless otherwise noted.



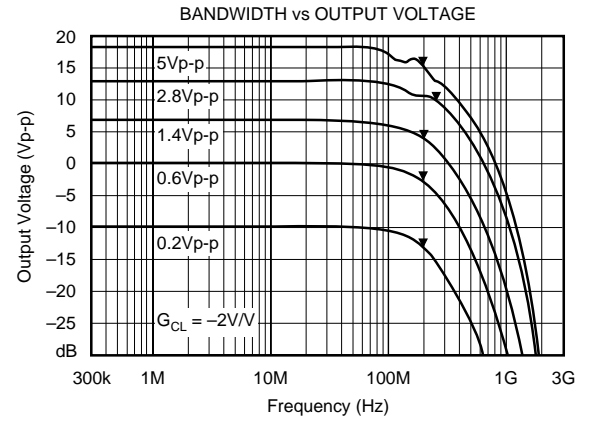
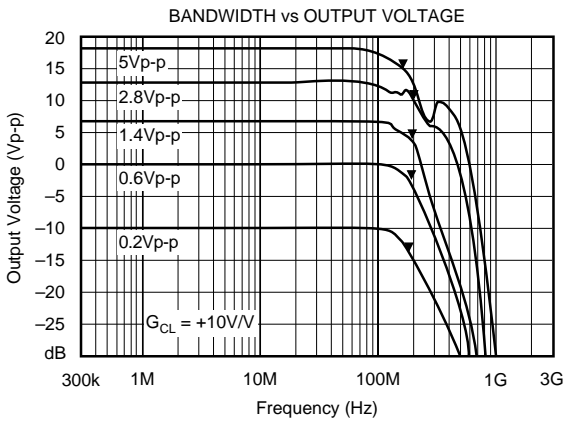
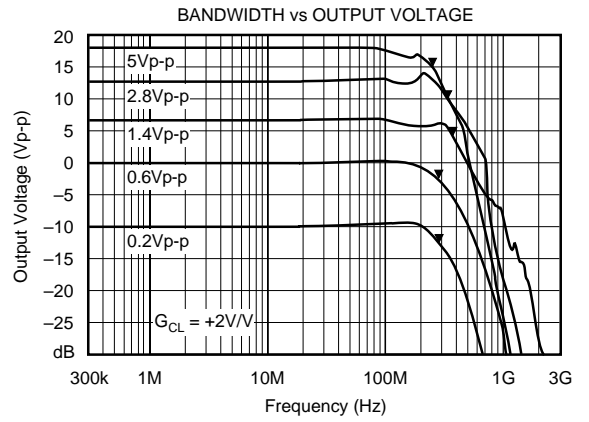
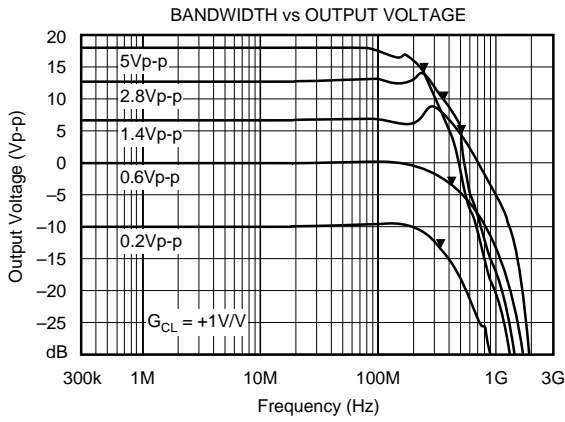
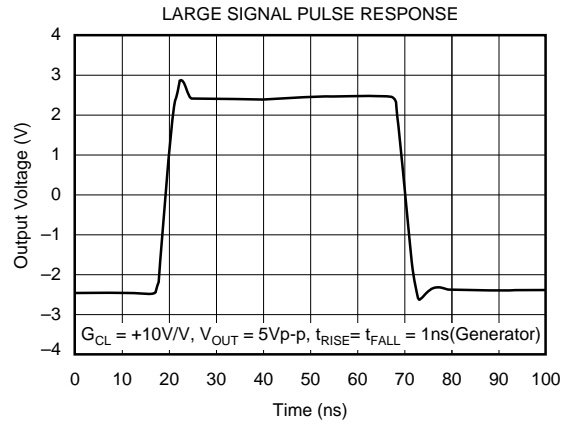
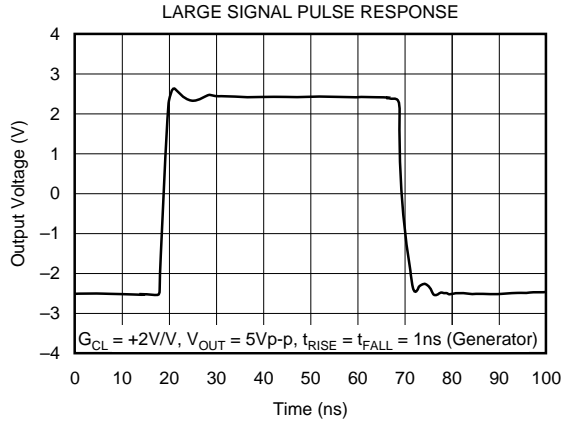
# TYPICAL PERFORMANCE CURVES (CONT)

At  $V_{CC} = \pm 5VDC$ ,  $R_L = 100\Omega$ ,  $I_Q = \pm 4mA$ ,  $R_{IN} = 150\Omega$ , and  $T_{AMB} = +25^\circ C$  unless otherwise noted.



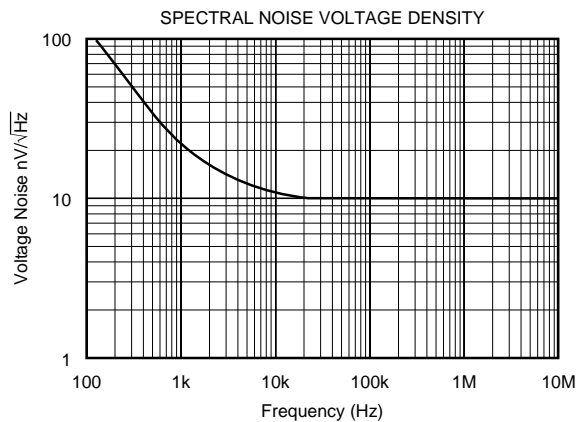
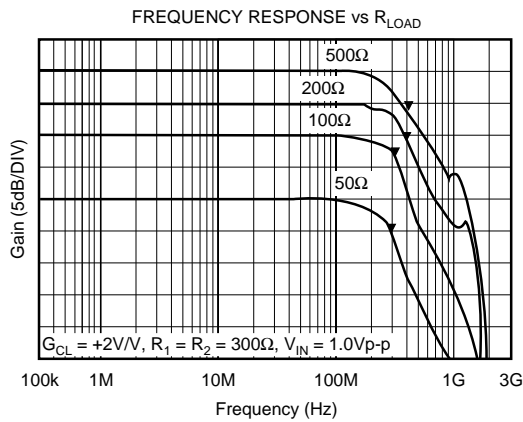
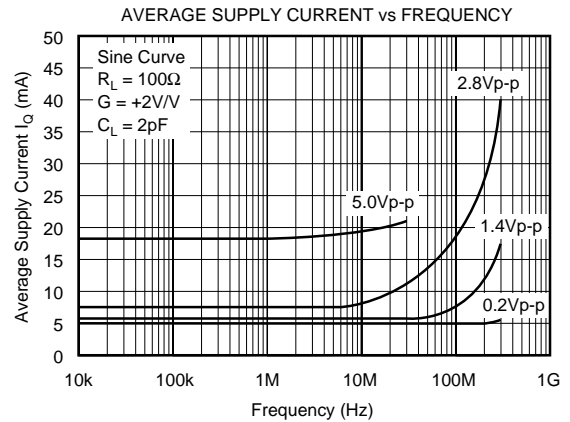
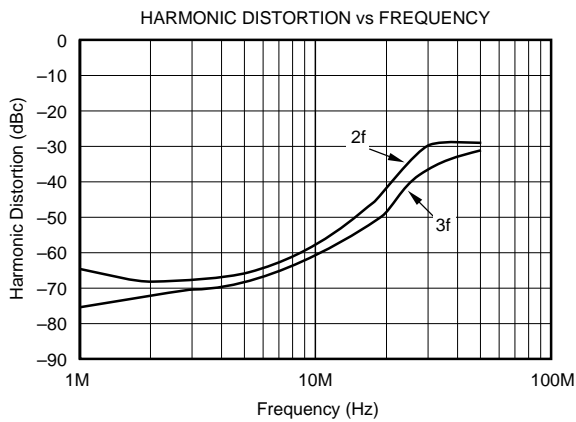
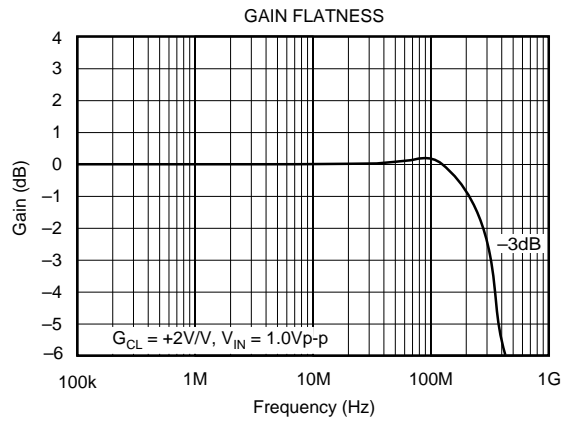
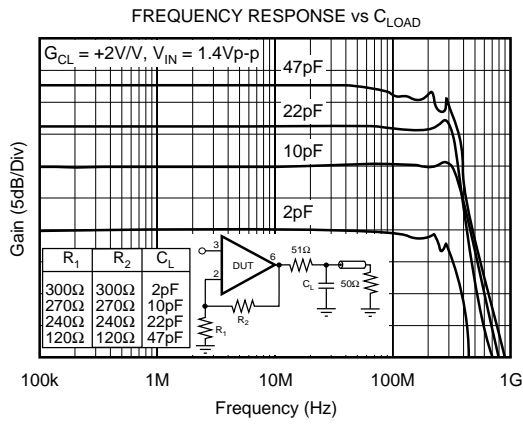
# TYPICAL PERFORMANCE CURVES (CONT)

At  $V_{CC} = \pm 5VDC$ ,  $R_L = 100\Omega$ ,  $I_O = \pm 4mA$ ,  $R_{IN} = 150\Omega$ , and  $T_{AMB} = +25^\circ C$  unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

At  $V_{CC} = \pm 5VDC$ ,  $R_L = 100\Omega$ ,  $I_Q = \pm 4mA$ ,  $R_{IN} = 150\Omega$ , and  $T_{AMB} = +25^\circ C$  unless otherwise noted.





## DISCUSSION OF PERFORMANCE

Requiring very low quiescent power, the OPA623 achieves its exceptional AC performance by using the current-feedback topology. This wide-band monolithic operational amplifier is designed for gain applications of up to 20V/V, where power and cost are of primary concern.

Operating from a  $\pm 5\text{V}$  supply, the OPA623 consumes only 40mW, yet maintains a 350MHz large-signal bandwidth at  $V_{\text{OUT}} = 2.8\text{V}_{\text{p-p}}$  and a 2100V/ $\mu\text{s}$  slew rate. Benefiting from the current-feedback architecture, the OPA623 offers stable operation with no compensation capacitor, even at unity gain.

With its low differential gain and phase errors of typically 0.12% and 0.05° at 4.43MHz, the OPA623 meets the performance and cost requirements of high-volume broadcast and HDTV applications.

The OPA623's large-signal bandwidth, high slew rate, excellent pulse response, and high drive capabilities are features well-suited to wide-band RGB video applications, RF instruments, and even high-speed digital communication systems.

For most circuit configurations, the OPA623 current-feedback op amp can be treated like a conventional op amp. As with a voltage-feedback op amp, the feedback network connected to the inverting input controls the closed-loop gain. But with a current-feedback op amp, the impedance of the feedback network also controls the open-loop gain and frequency response. Feedback resistor values can be selected to provide nearly constant closed-loop bandwidth over a wide range of gains and flat gain adjustment vs frequency.

## DESCRIPTION

A wide-band operational transconductance amplifier (OTA) and an output buffer are the main blocks of a current-feedback op amp. The simplified circuit diagram is illustrated in Figure 2. The OTA consists of a complementary unity-gain amplifier and a subsequent current mirror. The input buffer is connected across the inputs of the op amp. The voltage at the high-impedance +In terminal is transferred to the -In terminal at a low impedance. The current mirrors reflect any current flowing into or out of the +In terminal by a fixed ratio to the high-impedance OTA output, which is directly connected to the complementary output buffer. It is designed to drive low-impedance transmission

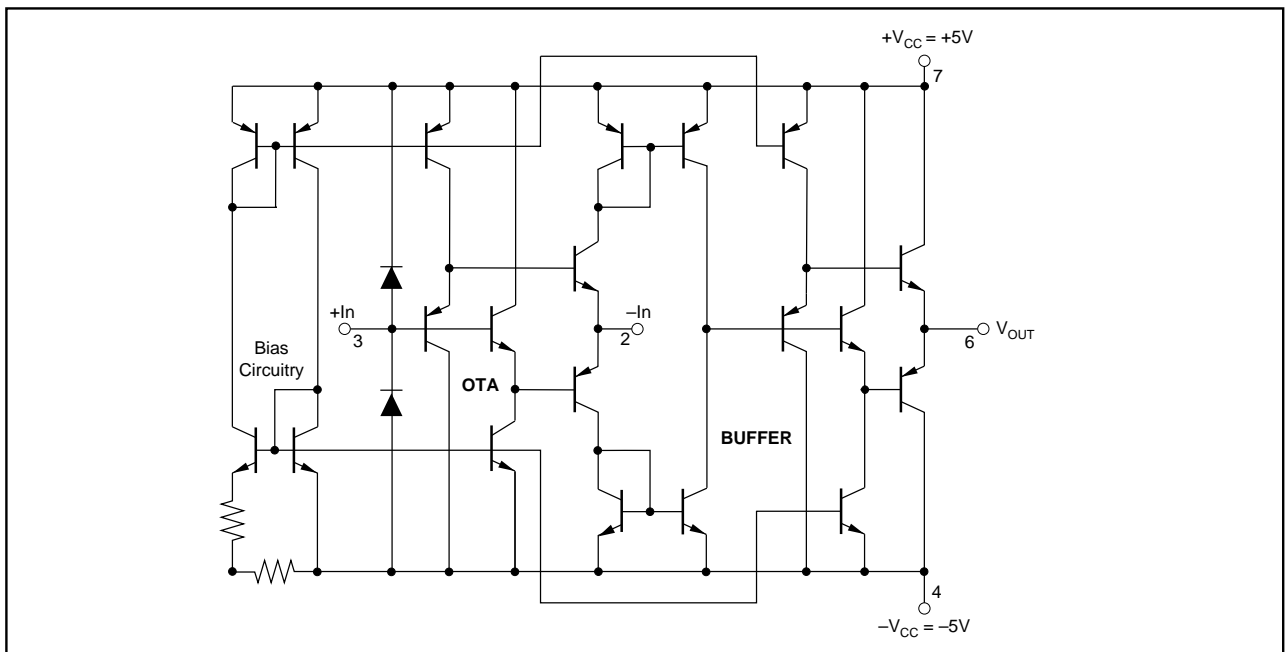


FIGURE 2. Simplified Circuit Diagram.

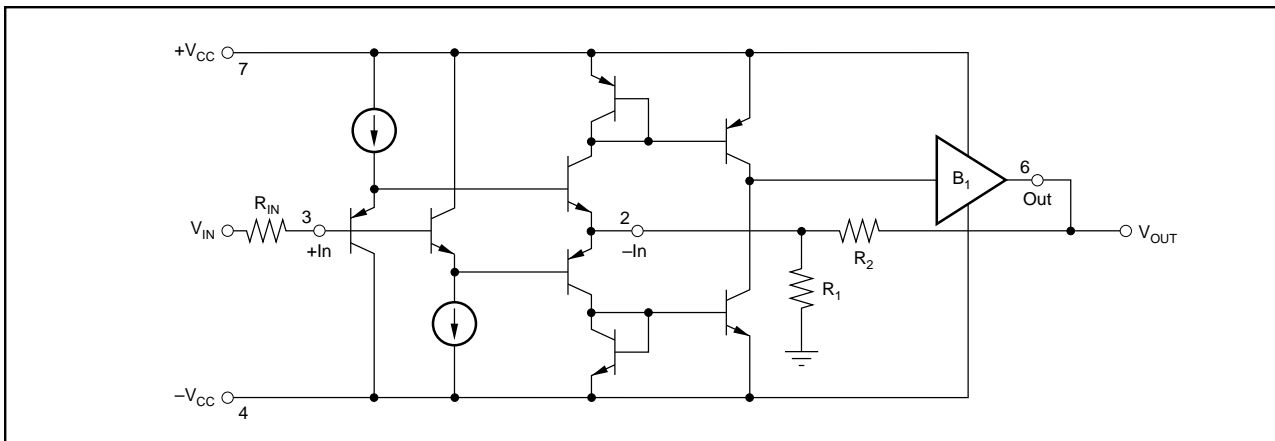


FIGURE 3. Non-Inverting Current-Feedback Op Amp Configuration.

lines or loads. The buffer output is not current-limited or protected.

As can be seen in Figure 3, the feedback in the form of a current is applied through  $R_2$  to the low-impedance inverting input, and the size of  $R_2 \parallel R_1$  determines the open-loop gain of the op amp.

The hybrid model shown in Figure 4 describes the AC behavior of a wide-band current-feedback op amp that is not internally compensated. The open-loop frequency response, which is illustrated in Figure 5 for various  $R_2$  values, is determined by two time constants. The elements R and C between the current source output and the output buffer form the dominant open-loop pole  $T_C$ . The signal delay time  $T_D$  modelled in the output buffer combines several small phase-shifting time constants and delay times. They are distributed throughout the amplifiers and are also present in the feedback loop. As shown in Figure 5, increasing  $R_2 \parallel R_1$  leads to a decreasing open-loop gain. The ratio of the two time constants  $T_C$  and  $T_D$  also determines the product  $G_{OL} \cdot G_{CL}$  for optimal closed-loop frequency response:

$$G_{OL} = G_{CL} \cdot \frac{T_C}{2T_D}$$

The two time constants  $T_C$  and  $T_D$ , however, are fixed by the op amp design. But varying  $R_2 \parallel R_1$  externally in the feedback loop allows for variation of the open-loop gain  $G_{OL}$  versus the closed-loop gain  $G_{CL}$ . This keeps the product  $G_{OL} \cdot G_{CL}$  constant, which is the theoretical condition for optimally flat frequency response.

This variation may be beneficial when driving high capacitive loads. Setting the open-loop gain externally also allows the circuit to be optimized to a wide range of capacitive loads, as shown in Figure 7 for a closed-loop gain of +2V/V and a capacitive load of up to 47pF.

It should be noted here that higher open-loop gain (resulting from lower feedback resistors) also yields lower distortion.

With external control of the open-loop characteristics of the op amp, dynamic behavior can be tailored to individual application requirements, and the open-loop gain selection

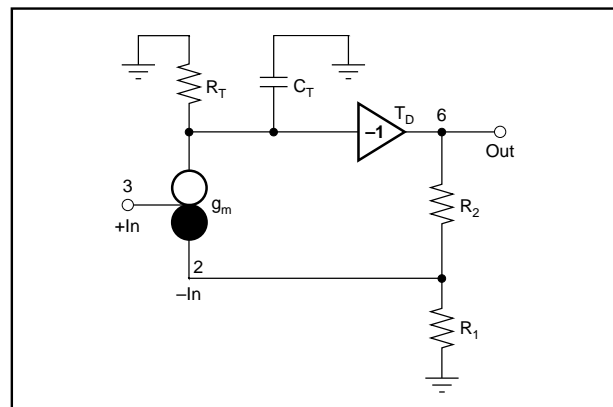


FIGURE 4. Hybrid Model OPA623.

provides a nearly constant closed-loop bandwidth, as shown in Figure 6 for various gains with an optimal flat frequency response. This behavior stands in contrast to op amps that are internally compensated for stable unity-gain operation, where the bandwidth is inversely proportional to the closed-loop gain, sharply limiting the bandwidth and slew rate at high output levels and gains.

In general, lower feedback resistors produce wider bandwidth, more frequency response peaking, and more pulse response overshooting. Higher feedback resistors results in an overdamped response with little or no peaking and overshooting.

Component pin and layout capacitances together with trace and wire board inductances from a resonant IC circuit can lead to oscillations of several hundreds of MHz. This very high frequency oscillation leads to an excessive increase in supply current which can destroy the device.

A resistor (100Ω to 250Ω) in series and close to the high-impedance, non-inverting input damps the LC circuit and generates a safe operation.

## THERMAL CONSIDERATIONS

The OPA623 does not require a heat sink for operation in most environments. The use of a heat sink, however, will

reduce the internal thermal rise, resulting in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. The internal power dissipation is given by the equation  $P_D = P_{DQ} + P_{DL}$ , ( $P_{DQ}$  is the quiescent power dissipation and  $P_{DL}$  is the power dissipation in the output stage due to the load). Although the  $P_{DQ}$  is very low (40mW at  $V_{CC} = \pm 5V$ ), care should be taken when a signal is applied. For high-speed op amps, a more precise approach to determine power consumption is to measure the average total quiescent current for several typical load conditions. The power consumption of the OPA623 is influenced by the kind of signal, the applied signal frequency, the output voltage, load resistor, and the repetition rate of the signal transitions. Figure 8 shows the average supply current versus the frequency of an applied sine wave for various output voltages. Figure 9 illustrates the average supply current versus the repetition frequency of an applied square wave signal.

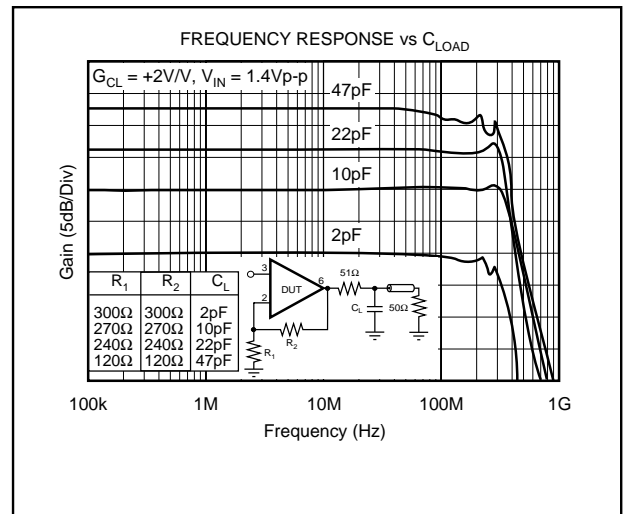


FIGURE 7. Frequency Response vs  $C_{LOAD}$ .

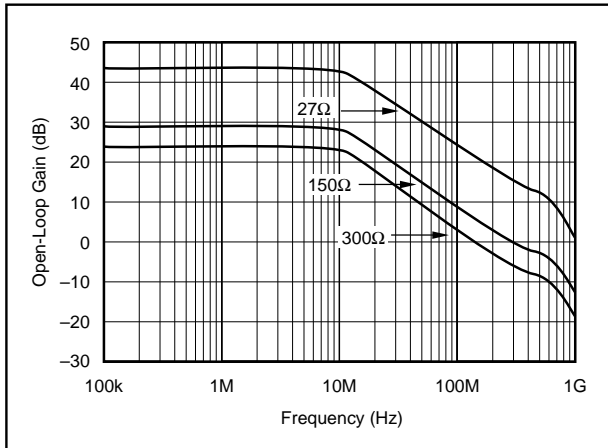


FIGURE 5. Open-Loop Gain vs  $R_2 \parallel R_1$ .

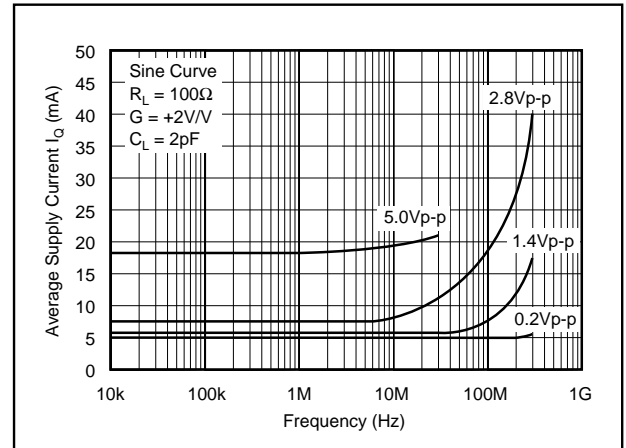


FIGURE 8. Average Supply Current vs Frequency (sinewave).

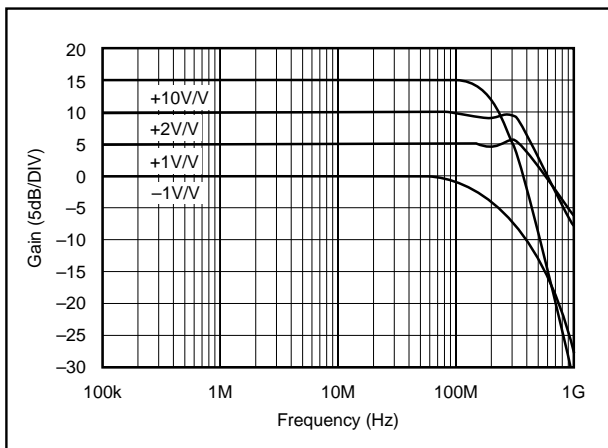


FIGURE 6. Optimum Frequency Response vs Closed-Loop Gain.

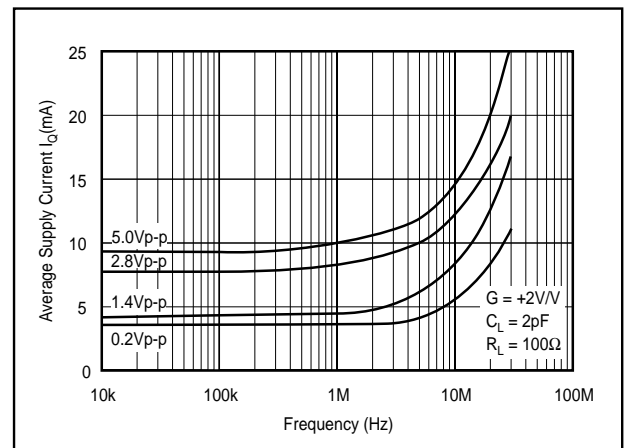


FIGURE 9. Average Supply Current vs Frequency (squarewave).

## CIRCUIT LAYOUT

The high-frequency performance of the operational amplifier OPA623 can be greatly affected by the physical layout of the printed circuit board. The following tips are offered as suggestions. Oscillations, ringing, poor bandwidth and settling, and peaking are all typical problems that plague high-speed components when they are used incorrectly.

- A resistor (100Ω to 250Ω) in series and close to the high-impedance, noninverting input is necessary to reduce peaking; this resistor prevents any very high-frequency oscillations at the op amp input, which can lead to an excessive increase in quiescent current.
- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2μF) with a parallel 470pF ceramic chip capacitor. Surface-mount types are recommended because of their low lead inductance. Although the OPA623 operates at a low quiescent current, high charging and discharging currents flow during steep transitions.
- PC board traces for power lines should be wide to reduce impedance and inductance.
- Make short low-inductance traces. The entire physical circuit should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout, however, do not extend the ground plane under high-impedance nodes such as the amplifier's input terminals, which are sensitive to stray capacitances.

- Sockets are not recommended because they add significant inductance and parasitic capacitance.
- Use low-inductance, surface-mounted components. Circuits using all surface-mount components with the OPA623AU will offer the best AC performance.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential—there are no shortcuts.
- Make the feedback trace as short as possible. The inverting input is sensitive to stray capacitances that lead to peaking in the frequency response. A stray capacitance at the inverting input increases the gain at high frequencies.

## SUGGESTED LAYOUT

A completely assembled and tested demonstration board is available for the OPA623 DIP package in a +2V/V configuration to speed prototyping. This board allows fast and easy performance testing during the design phase and for product qualification. The user can qualify the most important parameters within hours instead of days, while avoiding the hassles of an optimized board layout and power supply bypassing. For the most common gains Table 1 summarizes recommended component values for optimum flat frequency response. The complete AC characterization was performed with this board. Figure 10 shows the schematic and Figure 11 the silk screen and double-sided layout. Request DEM-OPA623-1GC to test the operational amplifier in the 8-pin DIP package.

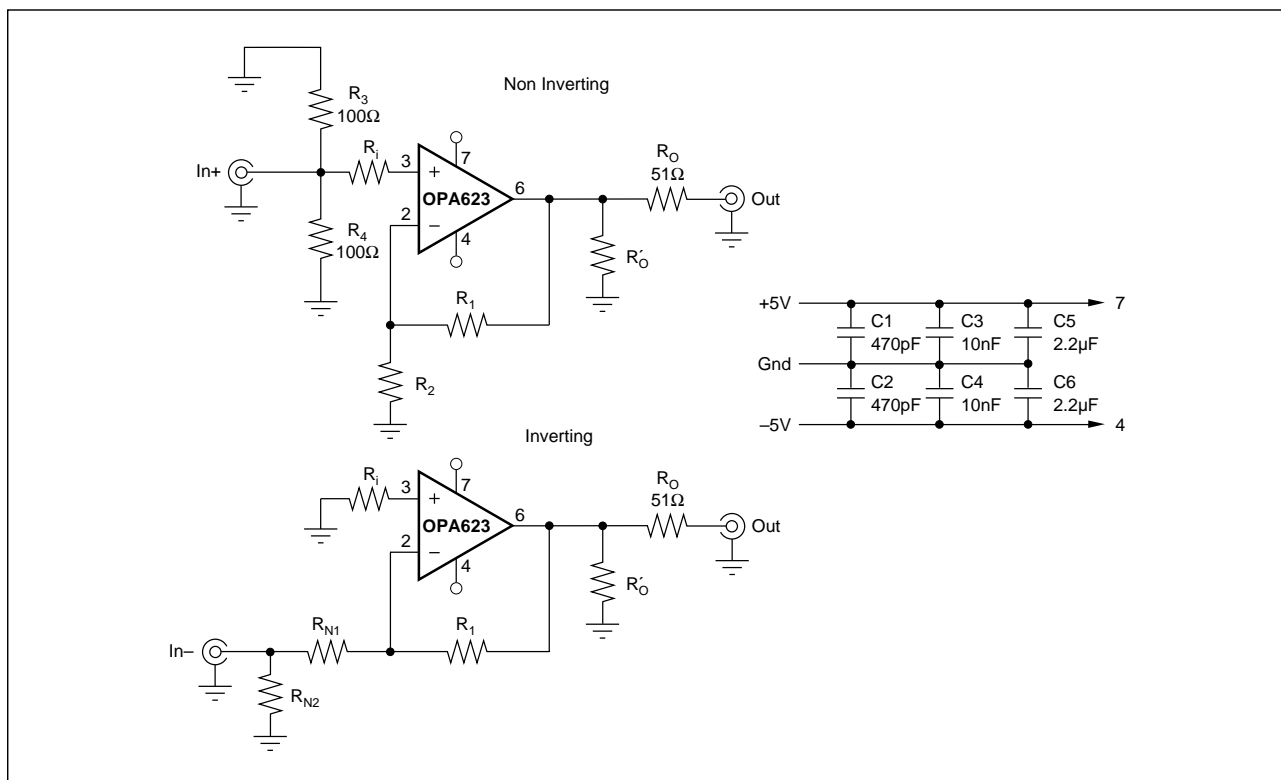


FIGURE 10. Circuit Schematic DEM-OPA623-1GC.

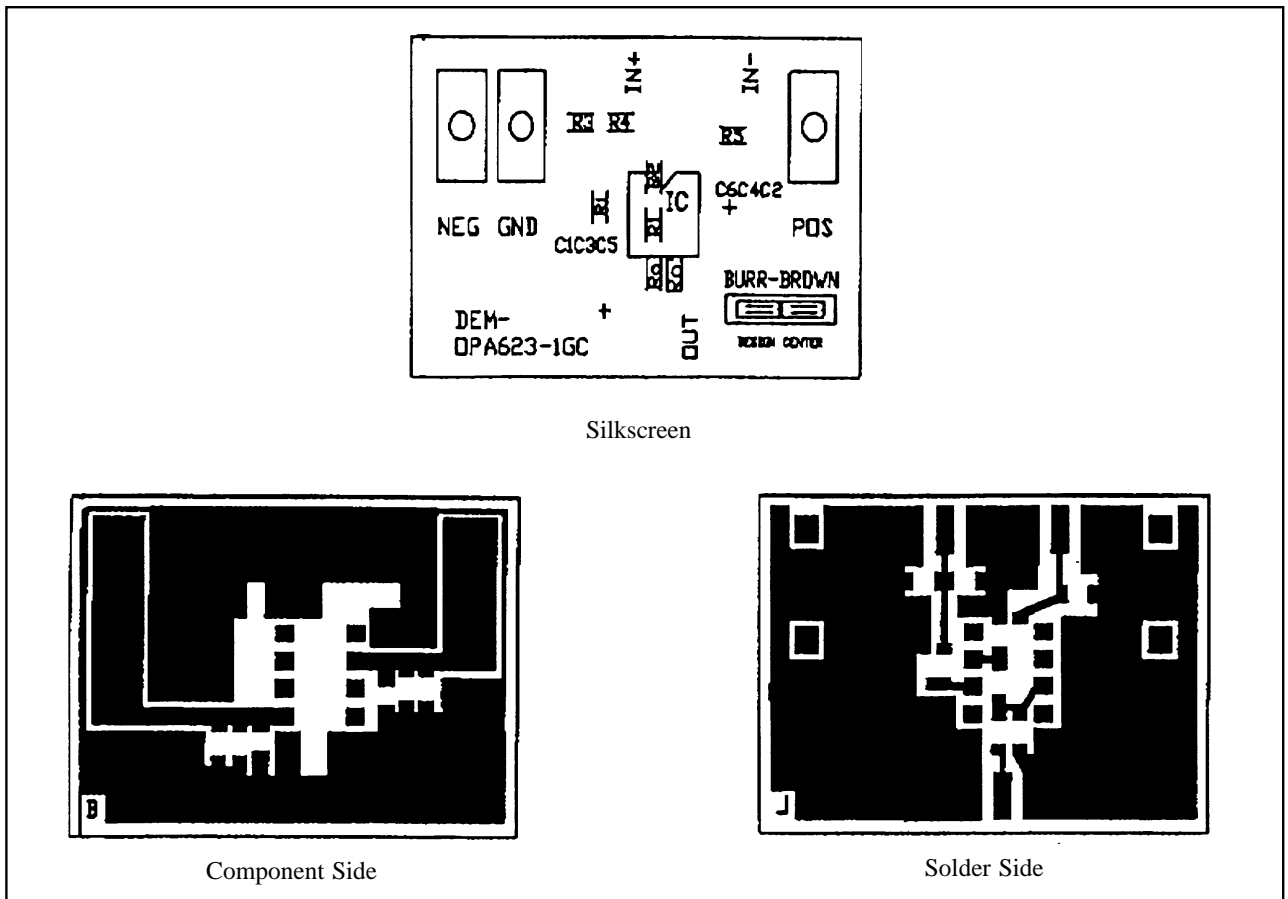


FIGURE 11. Silkscreen and Board Layouts DEM-OPA623-1GC.

COMPONENT	OPA623AP						OPA623AU					
	GAIN						GAIN					
	-2	-1	+1	+2	+5	+10	-2	-1	+1	+2	+5	+10
R <sub>1</sub>	150Ω	150Ω	200Ω	180Ω	100Ω	100Ω	150Ω	150Ω	270Ω	180Ω	100Ω	100Ω
R <sub>1</sub>	390Ω	390Ω	360Ω	300Ω	300Ω	130Ω	390Ω	390Ω	470Ω	300Ω	300Ω	160Ω
R <sub>2</sub>	—	—	—	300Ω	75Ω	15Ω	—	—	—	300Ω	76Ω	18Ω
R <sub>N1</sub>	200Ω	390Ω	—	—	—	—	200Ω	390Ω	—	—	—	—
R <sub>N2</sub>	68Ω	56Ω	—	—	—	—	68Ω	56Ω	—	—	—	—
Typical Bandwidth (MHz)												
V <sub>OUT</sub> = 0.2Vp-p	200	—	320	290	—	170	200	—	320	290	—	170
V <sub>OUT</sub> = 2.8Vp-p	330	360	340	350	260	210	330	360	340	350	260	210

TABLE I. Recommended Component Values.

## APPLICATIONS INFORMATION

The precise pulse response and high slew rate enables the OPA623 to be used in digital communication systems. Figure 12 shows the circuit schematic of an output amplifier with a gain of  $+2V/V$ , which can drive a  $75\Omega$  coaxial cable with a high-speed data stream of 140Mbit/s. Figure 13, for a binary 0, and Figure 14, for a binary 1, shows the pulse masks of the CCITT recommendation G.703 and the corresponding pulse responses of the OPA623. The signal code at the file rate of 139.264Mbit/s is CMI, the signal amplitude is 1Vp-p with  $\pm 1$ dB amplitude limits. Naturally, the OPA623 can also be used for HDB3 encoded 34Mbit/s, 155Mbit/s, STM-1, and 155Mbit/s B-ISDN transmission systems.

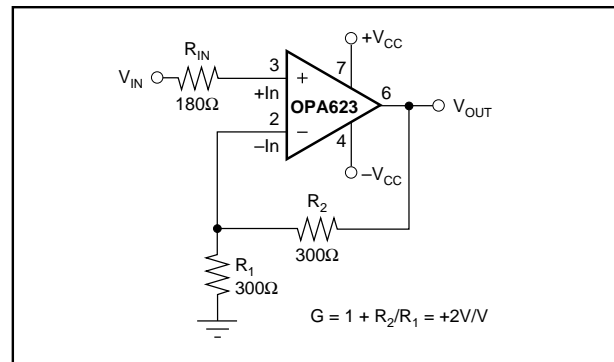


FIGURE 12. Driver Amplifier for a Digital 140Mbit/s Transmission system.

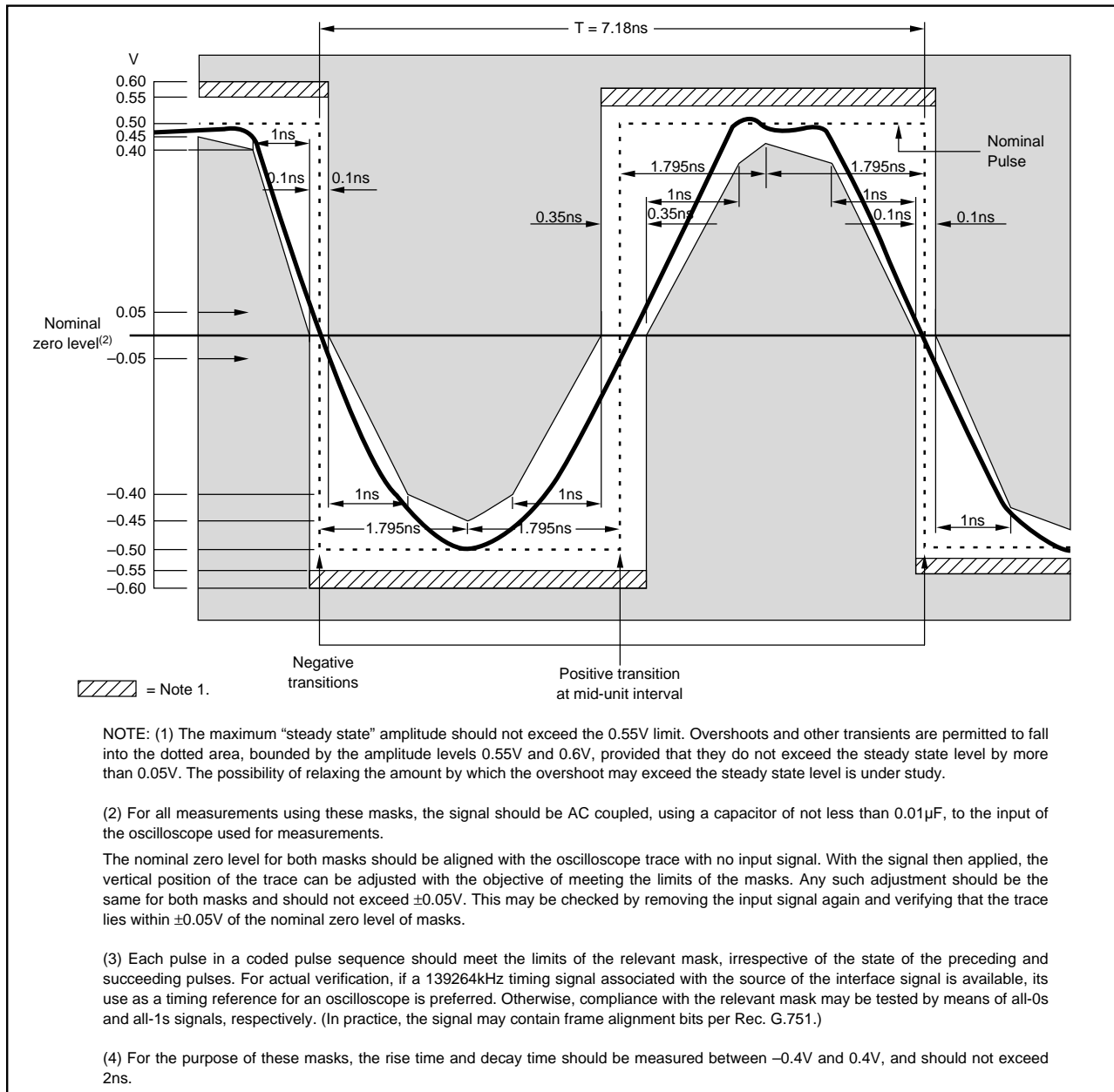


FIGURE 13. Mask of a Pulse Corresponding to a Binary 0 per CCITT Recommendation G.703.

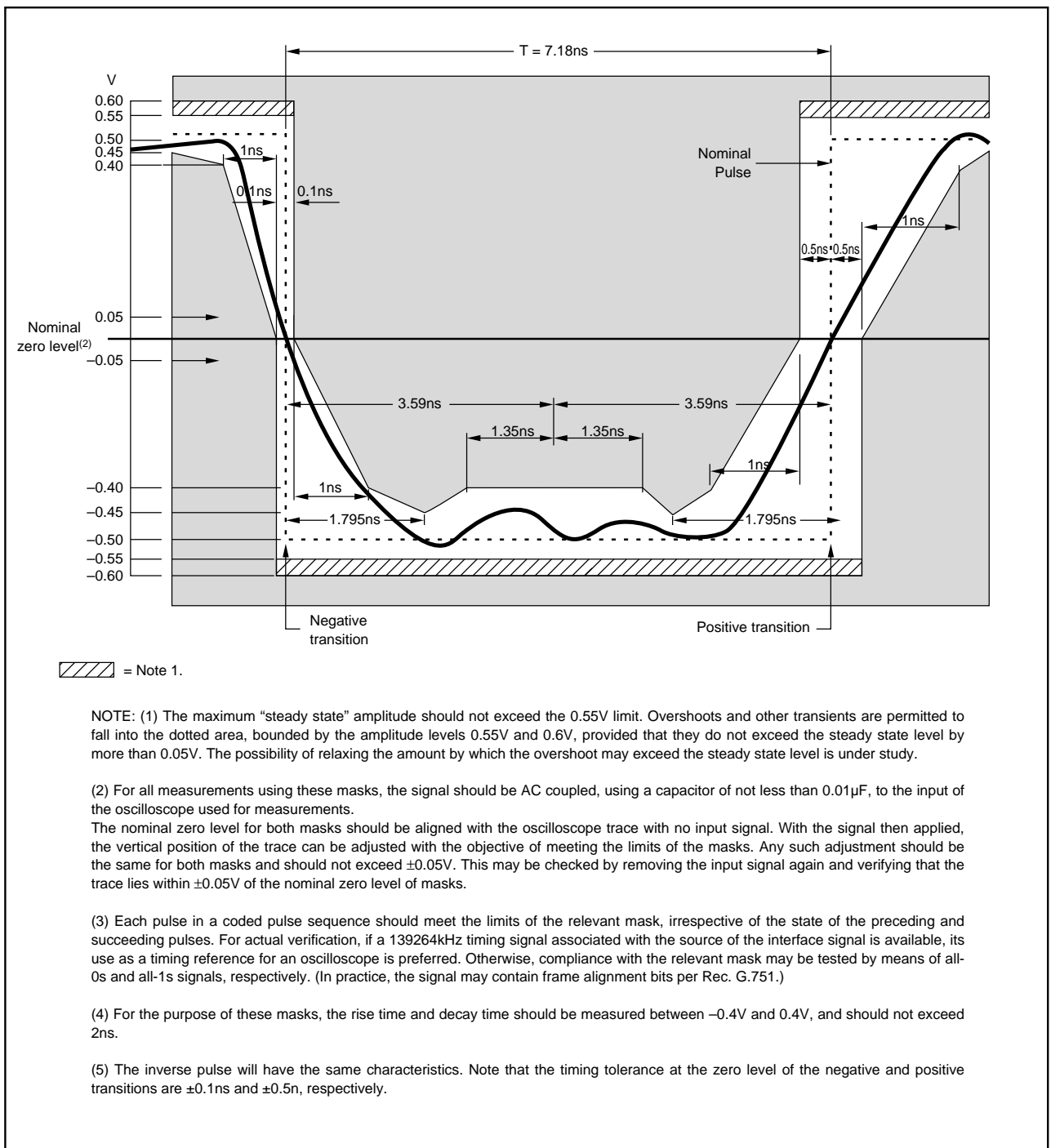


FIGURE 14. Mask of a Pulse Corresponding to a Binary 1 per CCITT Recommendation G.703.

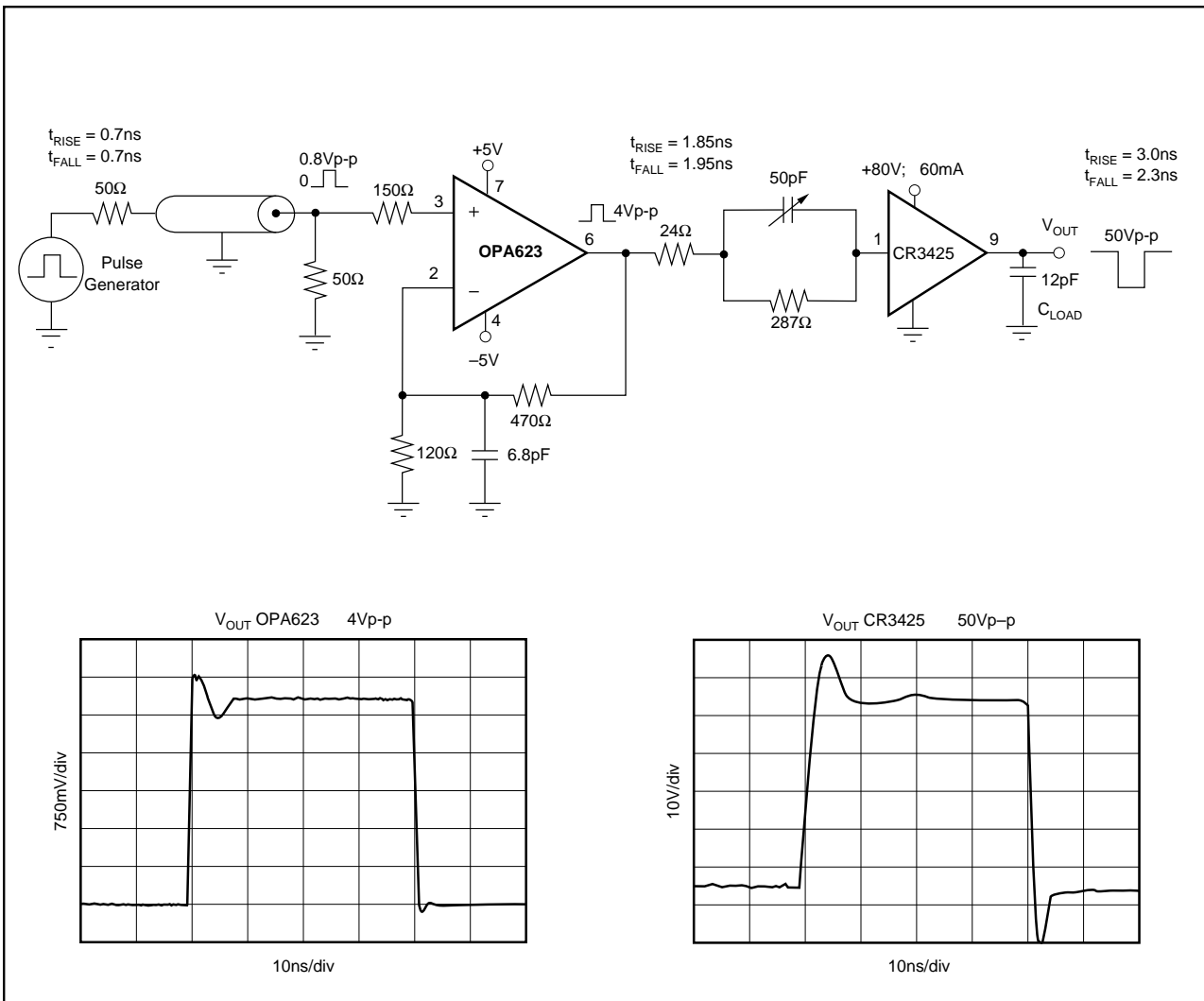


FIGURE 15. Video Amplifier for High Resolution Monitor (1600 x 1200 pixel).

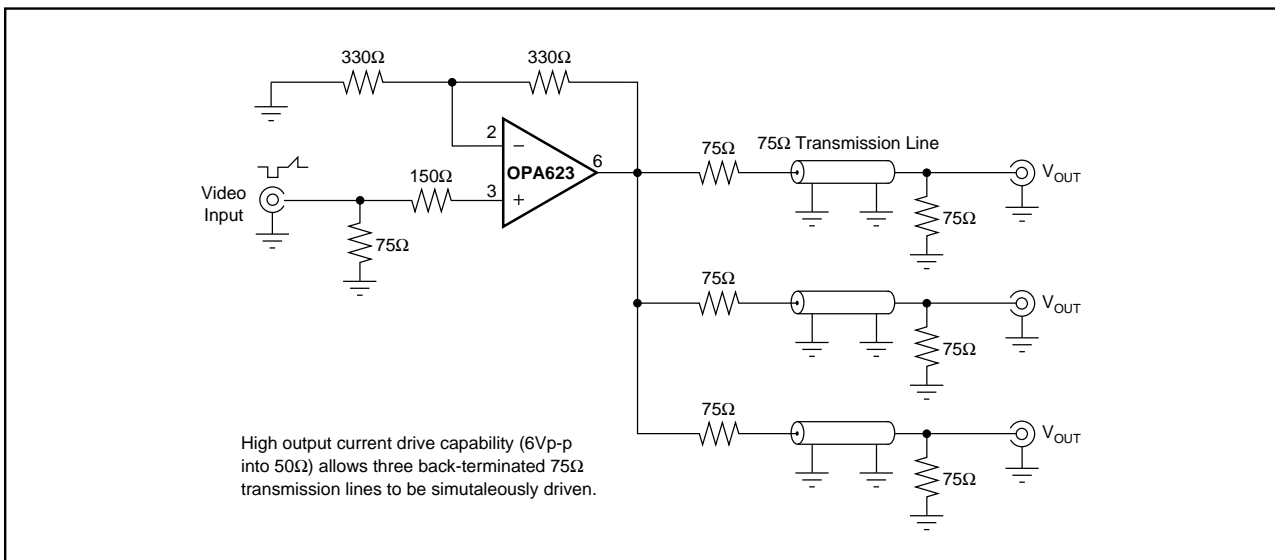
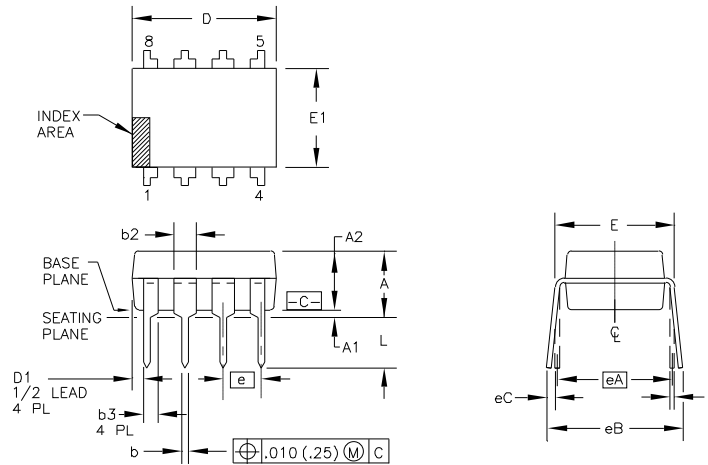


FIGURE 16. Video Distribution Amplifier.



# PACKAGE DRAWINGS

**Package Number 006 - 8-Pin Plastic, Single-Wide DIP**



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.63	BASIC	5
eB	--	.430	--	10.92	6

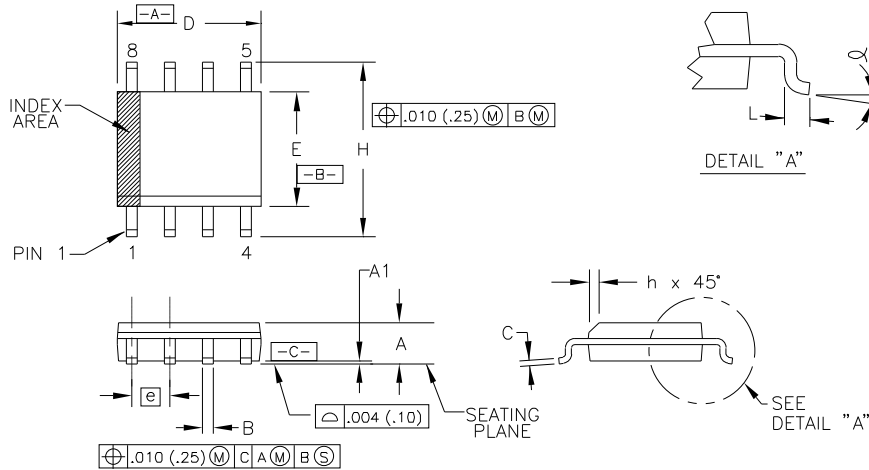
**NOTES:**

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM  $\bar{C}$ .
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.

8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006    REV.: E  
JEDEC NUMBER: MS-001-BA

**Package Number 182 - 8-Lead SOIC**



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050	BASIC	1.27	BASIC	
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	
L	.016	.050	0.41	1.27	5
N	8		8		6
alpha	0°	8°	0°	8°	

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT,

5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182    REV.: G  
JEDEC NUMBER: MS-012-AA