



# OPA621

## Wideband Precision OPERATIONAL AMPLIFIER

### FEATURES

- **LOW NOISE:**  $2.3\text{nV}/\sqrt{\text{Hz}}$
- **LOW DIFFERENTIAL GAIN/PHASE ERROR**
- **HIGH OUTPUT CURRENT:** 150mA
- **FAST SETTLING:** 25ns (0.01%)
- **GAIN-BANDWIDTH:** 500MHz
- **STABLE IN GAINS:**  $\geq 2\text{V/V}$
- **LOW OFFSET VOLTAGE:**  $\pm 100\mu\text{V}$
- **SLEW RATE:** 500V/ $\mu\text{s}$
- **8-PIN DIP, SOIC PACKAGES**

### APPLICATIONS

- **LOW NOISE PREAMPLIFIER**
- **LOW NOISE DIFFERENTIAL AMPLIFIER**
- **HIGH-RESOLUTION VIDEO**
- **LINE DRIVER**
- **HIGH-SPEED SIGNAL PROCESSING**
- **ADC/DAC BUFFER**
- **ULTRASOUND**
- **PULSE/RF AMPLIFIERS**
- **ACTIVE FILTERS**

### DESCRIPTION

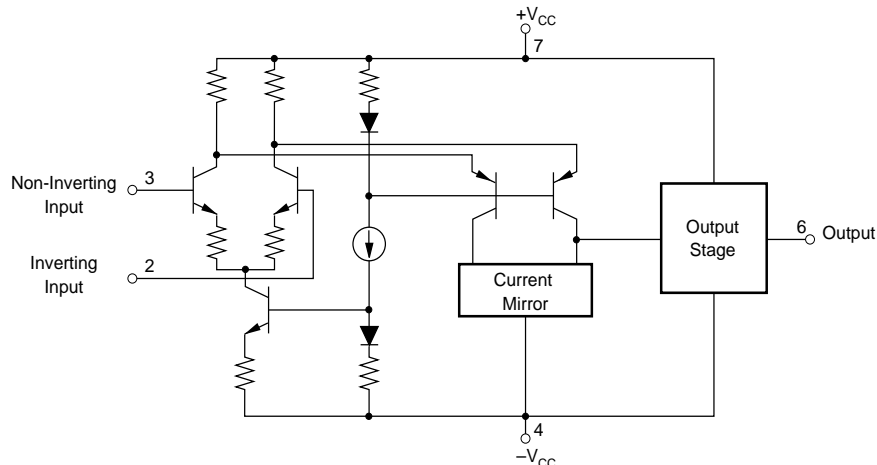
The OPA621 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA621 is stable in gains of  $\pm 2\text{V/V}$  or higher. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback"

amplifier designs, the OPA621 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

The OPA621 is available in plastic, ceramic, and SOIC packages. Two temperature ranges are offered:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  and  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .



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# SPECIFICATIONS

## ELECTRICAL

At  $V_{CC} = \pm 5VDC$ ,  $R_L = 100\Omega$ , and  $T_A = +25^\circ C$  unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP, KU			OPA621KG, SG			OPA621LG			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
<b>INPUT NOISE</b> Voltage: $f_O = 100Hz$ $f_O = 1kHz$ $f_O = 10kHz$ $f_O = 100kHz$ $f_O = 1MHz$ to $100MHz$ $f_B = 100Hz$ to $10MHz$ Current: $f_O = 10kHz$ to $100MHz$	$R_S = 0\Omega$		10 5.5 3.3 2.5 2.3 8.0 2.3			*	*		*	*	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $\mu V, rms$ $pA/\sqrt{Hz}$	
<b>OFFSET VOLTAGE<sup>(1)</sup></b> Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0VDC$ $T_A = T_{MIN}$ to $T_{MAX}$ $\pm V_{CC} = 4.5V$ to $5.5V$		$\pm 200$ $\pm 12$ 60	$\pm 1mV$		*	*		$\pm 100$ *	$\pm 500$	$\mu V$ $\mu V/^\circ C$ dB	
<b>BIAS CURRENT</b> Input Bias Current	$V_{CM} = 0VDC$		18	30		*	*		*	25	$\mu A$	
<b>OFFSET CURRENT</b> Input Offset Current	$V_{CM} = 0VDC$		0.2	2		*	*		*	*	$\mu A$	
<b>INPUT IMPEDANCE</b> Differential Common-Mode	Open-Loop		$15 \parallel 1$ $1 \parallel 1$			*	*		*	*	$k\Omega \parallel pF$ $M\Omega \parallel pF$	
<b>INPUT VOLTAGE RANGE</b> Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 2.5VDC$ , $V_O = 0VDC$	$\pm 3.0$ 65	$\pm 3.5$ 75		*	*		*	*		V dB	
<b>OPEN-LOOP GAIN, DC</b> Open-Loop Voltage Gain	$R_L = 100\Omega$ $R_L = 50\Omega$	50 48	60 58		*	*		55 53	*	*	dB dB	
<b>FREQUENCY RESPONSE</b> Closed-Loop Bandwidth (-3dB)  Gain-Bandwidth Differential Gain Differential Phase Harmonic Distortion <sup>(2)</sup>  Full Power Response <sup>(2)</sup>  Slew Rate <sup>(2)</sup> Overshoot Settling Time: 0.1% 0.01% Phase Margin Rise Time	Gain = +2V/V Gain = +5V/V Gain = +10V/V Gain = +10V/V 3.58MHz, G = +2V/V 3.58MHz, G = +2V/V G = +2V/V, f = 10MHz, $V_O = 2Vp-p$ f = 10MHz, Second Harmonic Third Harmonic $V_O = 5Vp-p$ , Gain = +2V/V $V_O = 2Vp-p$ , Gain = +2V/V 2V Step, Gain = -2V/V 2V Step, Gain = -2V/V 2V Step, Gain = -2V/V  Gain = +2V/V Gain = +2V/V, 10% to 90% $V_O = 100mVp-p$ ; Small Signal $V_O = 6Vp-p$ ; Large Signal		500 100 50 500 0.05 0.05  22 55 350 15 15 25 50  1.8 8									MHz MHz MHz MHz % Degrees  dBc <sup>(3)</sup> dBc MHz MHz V/ $\mu s$ % ns ns Degrees  ns ns
<b>RATED OUTPUT</b> Voltage Output  Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 100\Omega$ $R_L = 50\Omega$ 1MHz, Gain = +2V/V Gain = +2V/V Continuous	$\pm 3.0$ $\pm 2.5$	$\pm 3.5$ $\pm 3.0$ 0.015 15 $\pm 150$		*	*		*	*	*	V V $\Omega$ pF mA	
<b>POWER SUPPLY</b> Rated Voltage Derated Performance Current, Quiescent	$\pm V_{CC}$ $\pm V_{CC}$ $I_O = 0mADC$	4.0	5 26	6.0 28	*	*	*	*	*	*	VDC VDC mA	
<b>TEMPERATURE RANGE</b> Specification: KP, KU, KG, LG, SG Operating: KG, LG, SG KP, KU $\theta_{JA}$ KG, LG, SG KP KU	Ambient Temperature  Ambient Temperature	-40		+85	*		*	*		*	$^\circ C$ $^\circ C$ $^\circ C$ $^\circ C$ $^\circ C/W$ $^\circ C/W$ $^\circ C/W$	

\* Same Specifications as for KP, KU.

# SPECIFICATIONS (CONT)

## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At  $V_{CC} = \pm 5VDC$ ,  $R_L = 100\Omega$ , and  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.

PARAMETER	CONDITIONS	OPA621KP, KU			OPA621KG, SG			OPA621LG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>TEMPERATURE RANGE</b> Specification: KP, KU, KG, LG SG	Ambient Temperature	-40		+85	*		*	*		*	°C °C
<b>OFFSET VOLTAGE<sup>(1)</sup></b> Average Drift Supply Rejection	Full Temperature Range $\pm V_{CC} = 4.5V$ to $5.5V$	45	$\pm 12$ 60		*	*		50	*	*	$\mu V/^\circ C$ dB
<b>BIAS CURRENT</b> Input Bias Current	Full Temperature, $V_{CM} = 0VDC$		18	40		*	*		*	35	$\mu A$
<b>OFFSET CURRENT</b> Input Offset Current	Full Temperature, $V_{CM} = 0VDC$		0.2	5		*	*		*	*	$\mu A$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 2.5VDC$ , $V_O = 0VDC$	$\pm 2.5$ 60	$\pm 3.0$ 75		*	*		*	*		V dB
<b>OPEN LOOP GAIN, DC</b> Open-Loop Voltage Gain	$R_L = 100\Omega$ $R_L = 50\Omega$	46 44	60 58		*	*		52 50	*	*	dB dB
<b>RATED OUTPUT</b> Voltage Output	$R_L = 100\Omega$ $R_L = 50\Omega$	$\pm 3.0$ $\pm 2.5$	$\pm 3.5$ $\pm 3.0$		*	*		*	*		V V
<b>POWER SUPPLY</b> Current, Quiescent	$I_O = 0mADC$		26	30		*	*		*	*	mA

\* Same specifications as for KP/KU.

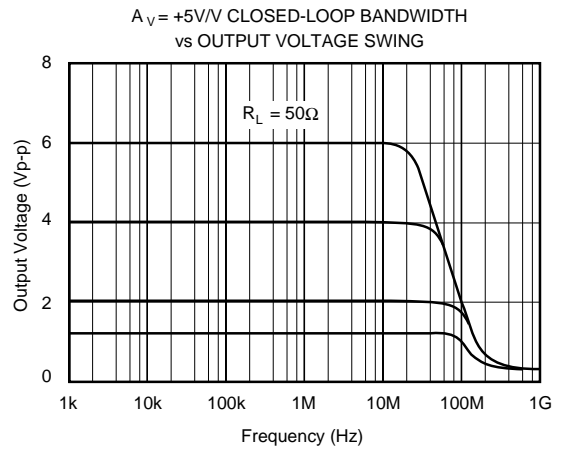
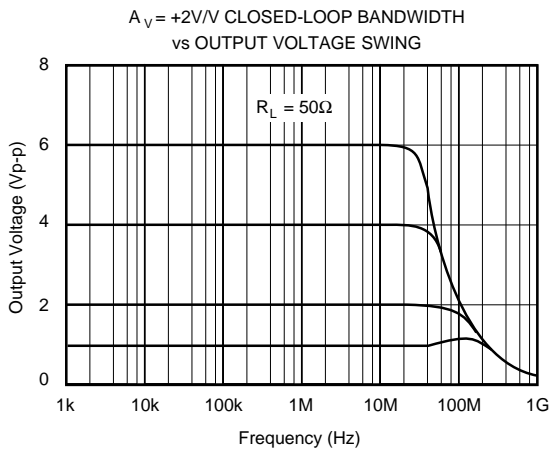
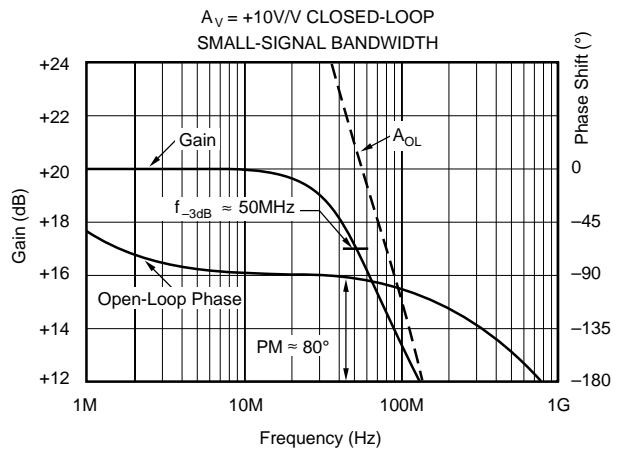
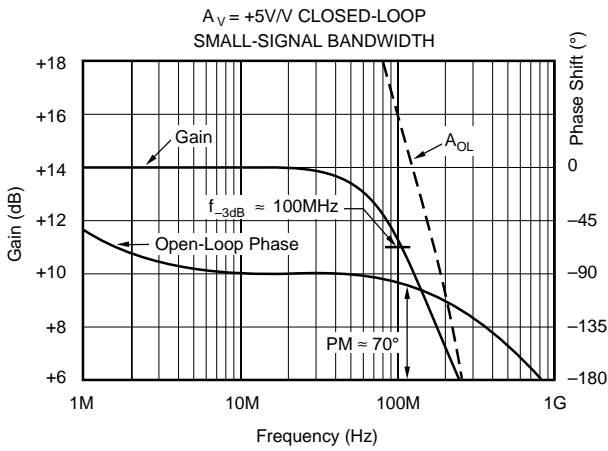
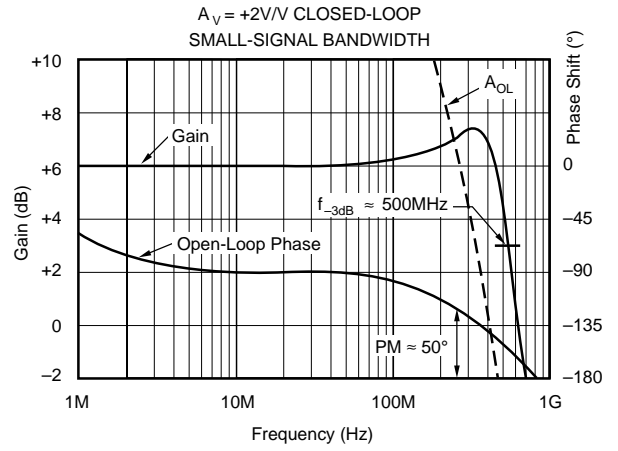
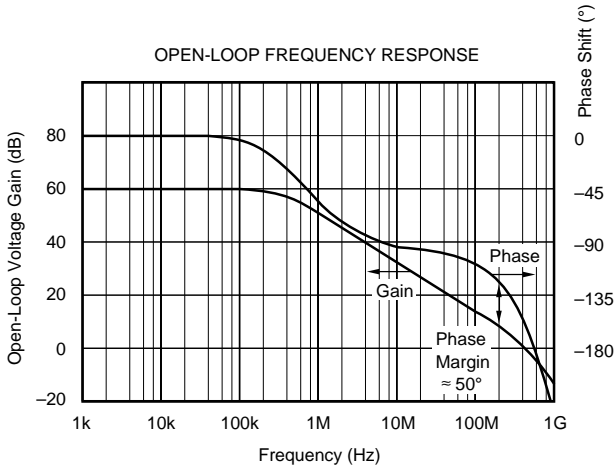
NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB referred to carrier-input signal.

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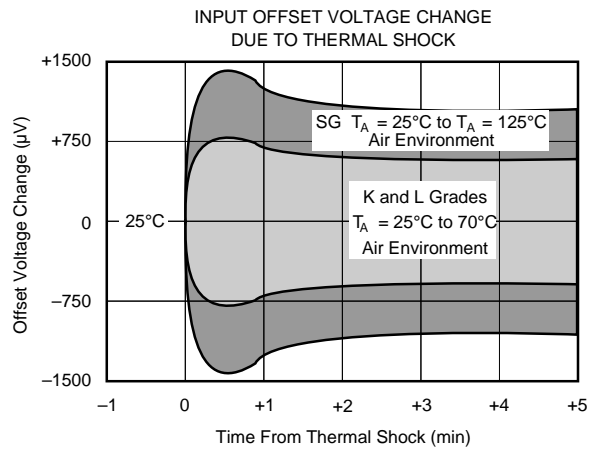
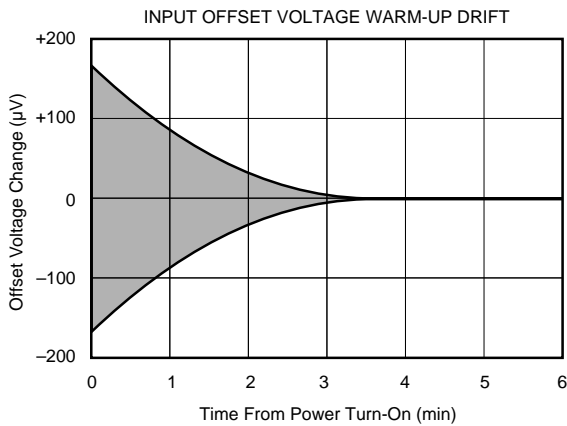
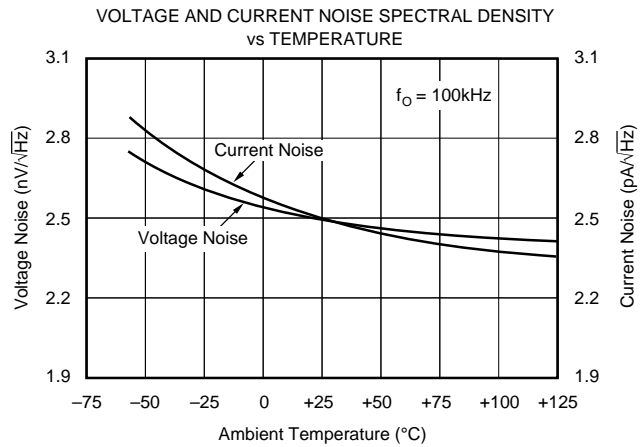
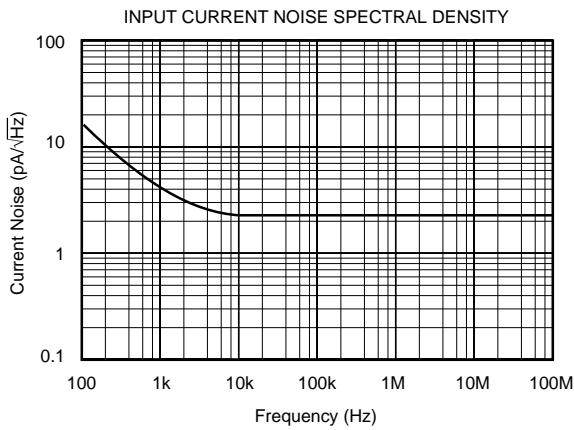
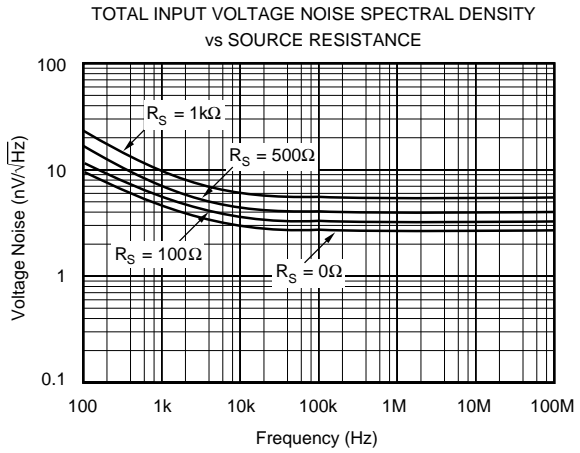
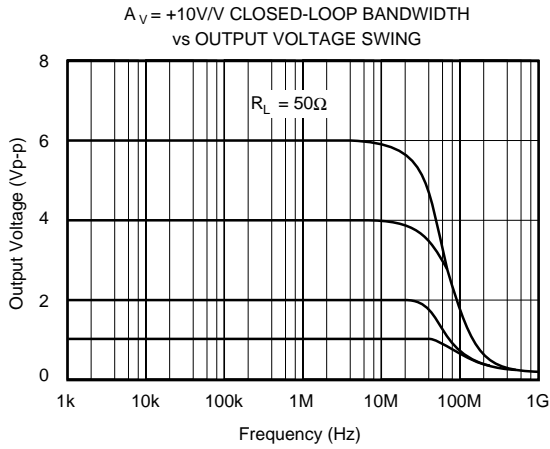
# TYPICAL PERFORMANCE CURVES

At  $V_{CC} = \pm 5VDC$ ,  $R_L = 100\Omega$ , and  $T_A = +25^\circ C$  unless otherwise noted.



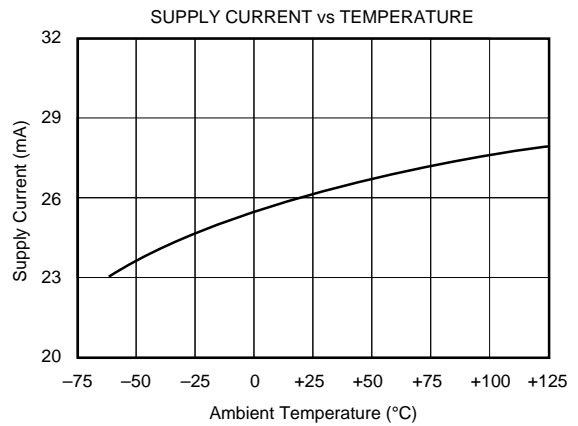
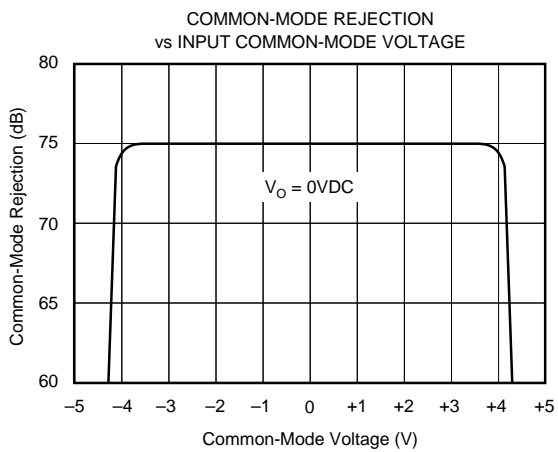
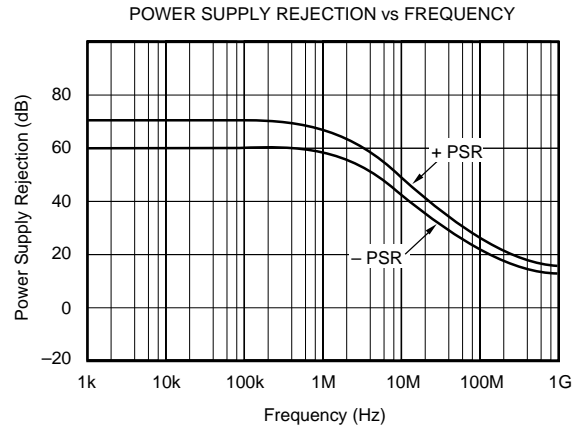
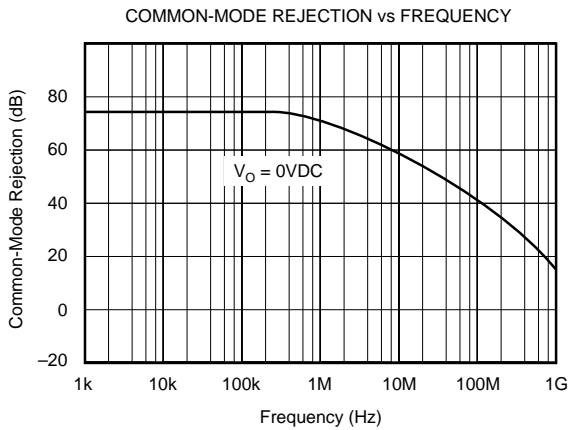
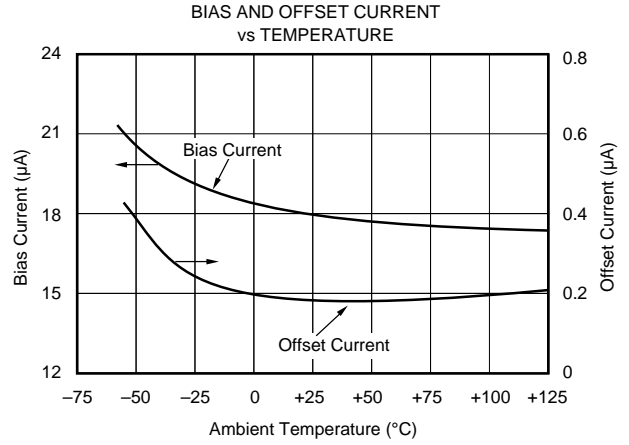
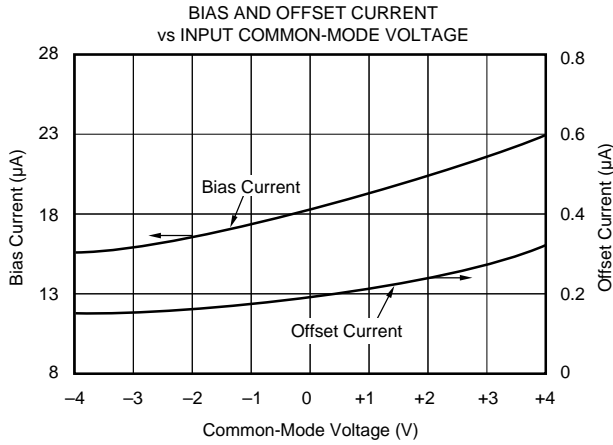
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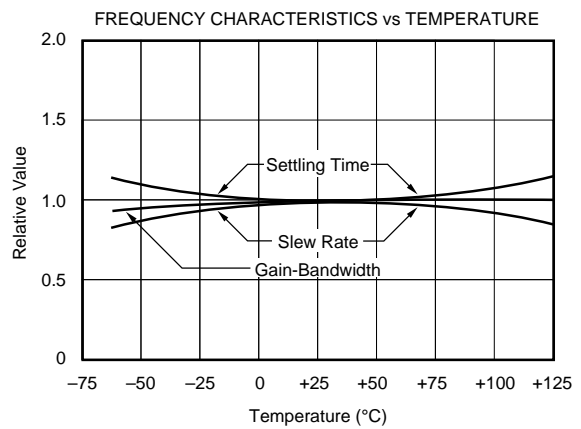
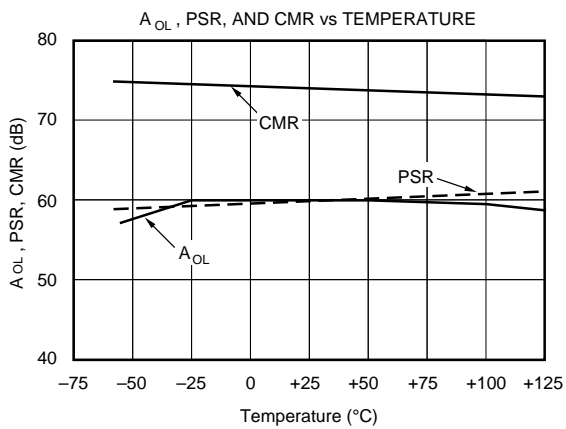
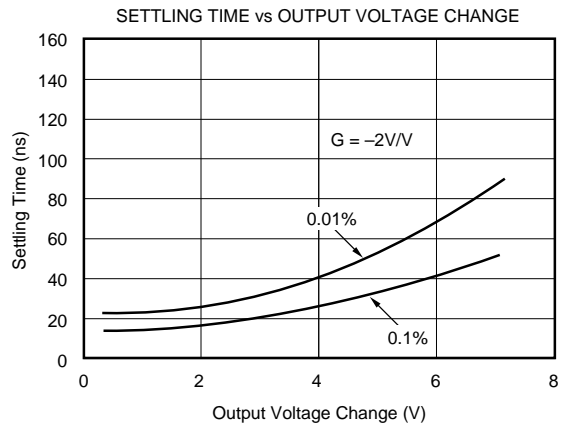
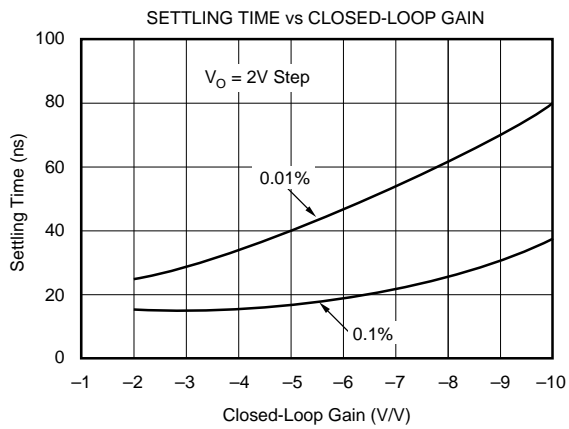
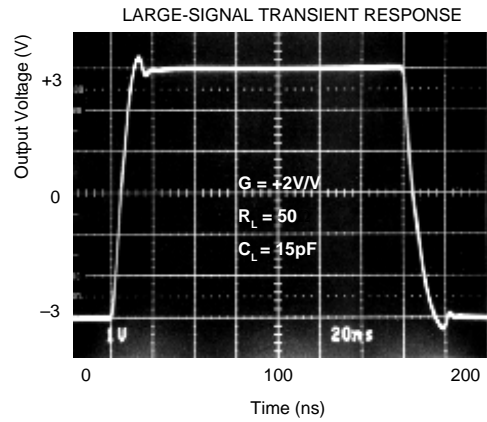
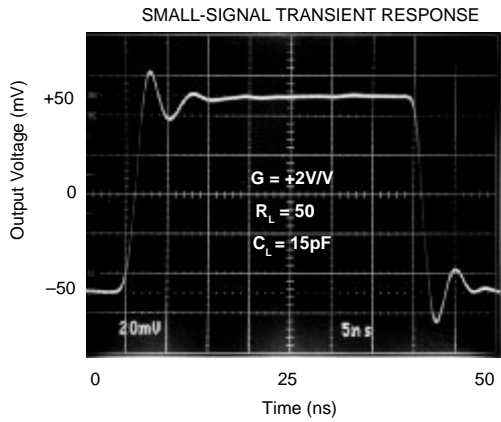
# TYPICAL PERFORMANCE CURVES (CONT)

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# TYPICAL PERFORMANCE CURVES (CONT)

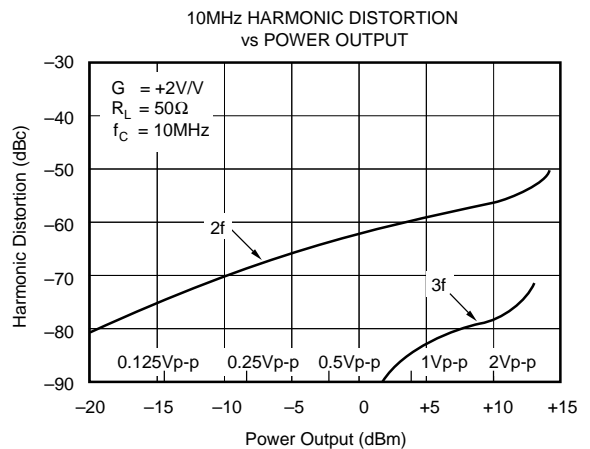
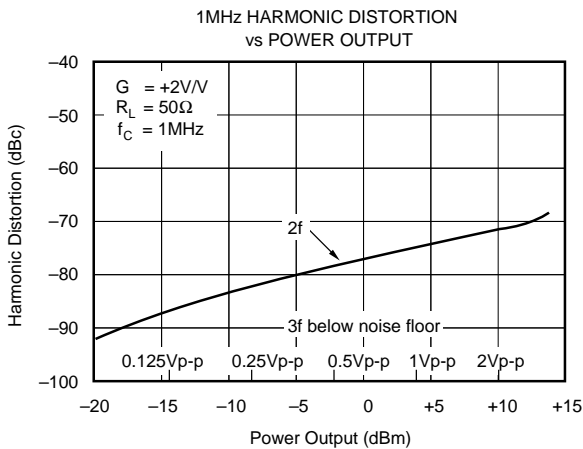
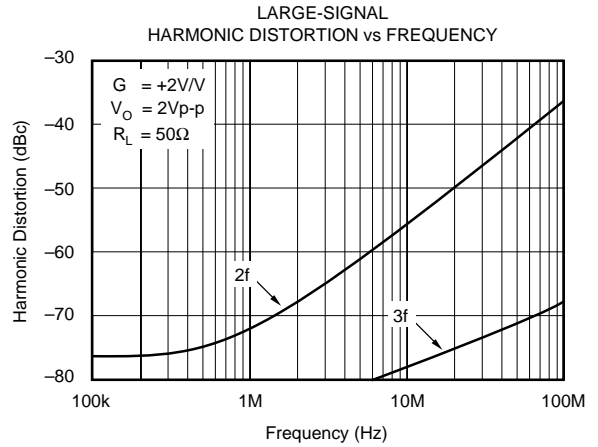
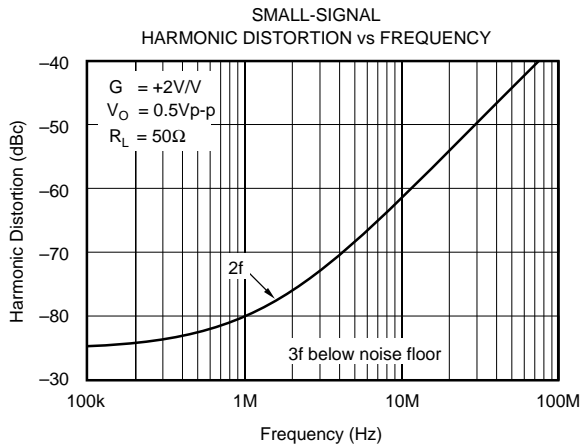
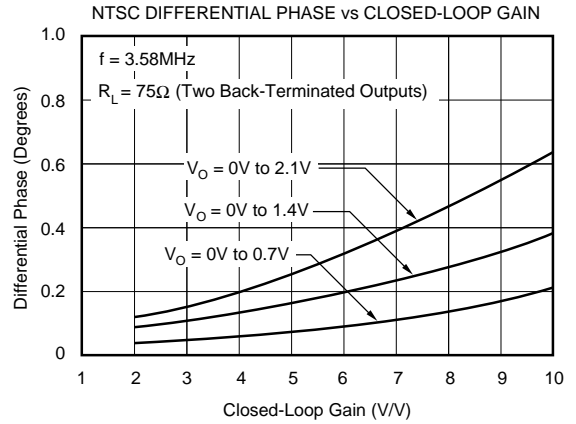
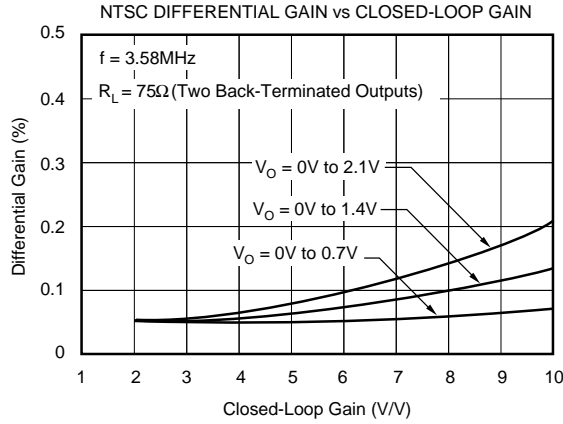
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# TYPICAL PERFORMANCE CURVES (CONT)

At  $V_{CC} = \pm 5VDC$ ,  $R_L = 100\Omega$ , and  $T_A = +25^\circ C$  unless otherwise noted.



# APPLICATIONS INFORMATION

## DISCUSSION OF PERFORMANCE

The OPA621 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA621's design uses a "Classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e. one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 microseconds even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA621's "Classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA621. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 500MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100 $\mu$ V.

## WIRING PRECAUTIONS

Maximizing the OPA621's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA621, as it is with all high-frequency circuits.

Oscillations at frequencies of 500MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2oz copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must always be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1 $\mu$ F to 10 $\mu$ F) with very short leads are recommended. Although not required, a parallel 0.01 $\mu$ F ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

## Points to Remember

- 1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.
- 2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.
- 3) Whenever possible, solder the OPA621 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® stand-offs located close to the amplifier's pins can be used to mount feedback components.
- 4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1k $\Omega$  on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely unacceptable in high-frequency circuits.
- 5) Surface mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface mount components with the OPA621AU (SOIC package) will offer the best AC performance. The parasitic package inductance and capaci-

tance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use  $\pm 5V$  supplies. Although they will operate perfectly well with  $+5V$  and  $-5.2V$ , use of  $\pm 15V$  supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA621's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

### OFFSET VOLTAGE ADJUSTMENT

The OPA621's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with  $R_3$ . This will reduce input bias current errors to the amplifier's offset current, which is typically only  $0.2\mu A$ .

### INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA621 incorporates on-chip ESD protection diodes as shown in Figure 2. This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA621 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about  $0.7V$ . This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of  $30mA$  without destruction. To insure long term reliability, however, diode current should be externally limited to  $10mA$  or so whenever possible.

Teflon® E. I. Du Pont de Nemours & Co.

The internal protection diodes are designed to withstand  $2.5kV$  (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA621.

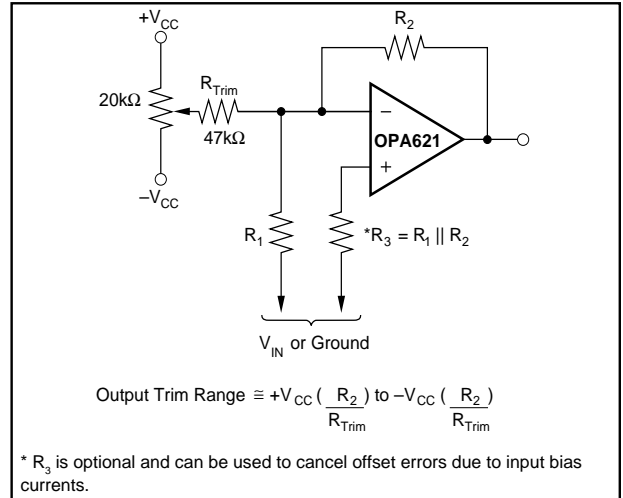


FIGURE 1. Offset Voltage Trim.

### OUTPUT DRIVE CAPABILITY

The OPA621's design uses large output devices and has been optimized to drive  $50\Omega$  and  $75\Omega$  resistive loads. The device can easily drive  $6Vp-p$  into a  $50\Omega$  load. This high-output drive capability makes the OPA621 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about  $150mA$  at  $25^\circ C$ . This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA621 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

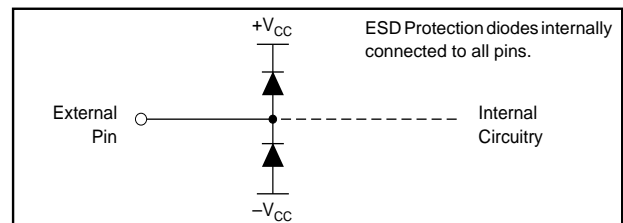


FIGURE 2. Internal ESD Protection.

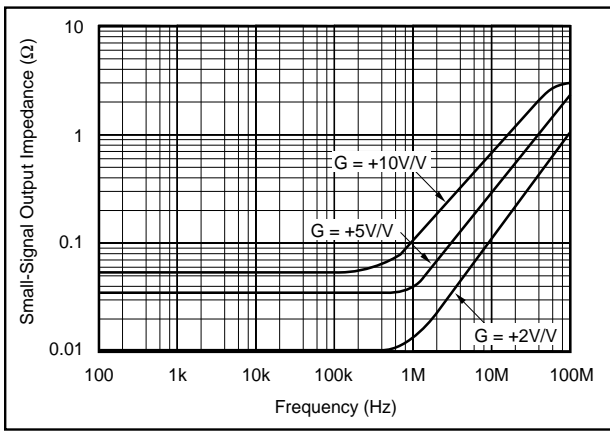


FIGURE 3. Small-Signal Output Impedance vs Frequency.

### THERMAL CONSIDERATIONS

The OPA621 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See “Maximum Power Dissipation” curve, Figure 4.

The internal power dissipation is given by the equation  $P_D = P_{DQ} + P_{DL}$ , where  $P_{DQ}$  is the quiescent power dissipation and  $P_{DL}$  is the power dissipation in the output stage due to the load. (For  $\pm V_{CC} = \pm 5V$ ,  $P_{DQ} = 10V \times 28mA = 280mW$ , max). For the case where the amplifier is driving a grounded load ( $R_L$ ) with a DC voltage ( $\pm V_{OUT}$ ) the maximum value of  $P_{DL}$  occurs at  $\pm V_{OUT} = \pm V_{CC}/2$ , and is equal to  $P_{DL, max} = (\pm V_{CC})^2/4R_L$ . Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common  $P_{DL} = 5V \times 150mA = 750mW$ . Thus,  $P_D = 280mW + 750mW = 1W$ . Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the “Maximum Power Dissipation” curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance,  $\theta_{JA}$ , of each package. The variation of short-circuit current with temperature is shown in Figure 5.

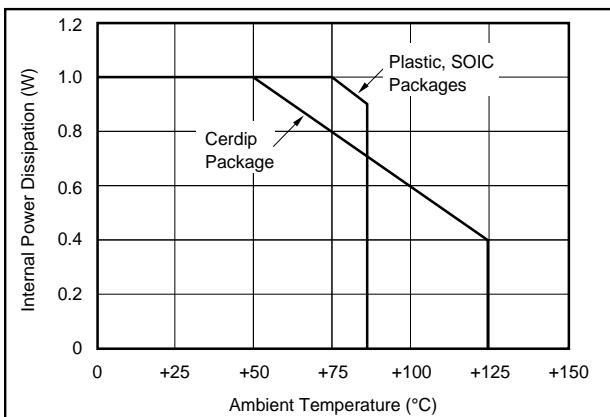


FIGURE 4. Maximum Power Dissipation.

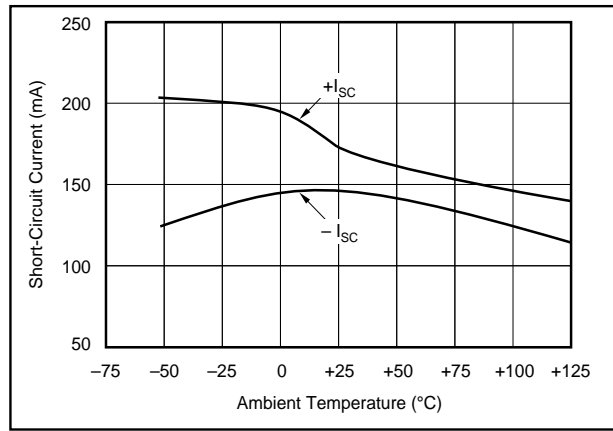


FIGURE 5. Short-Circuit Current vs Temperature.

### CAPACITIVE LOADS

The OPA621’s output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier’s phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 15pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

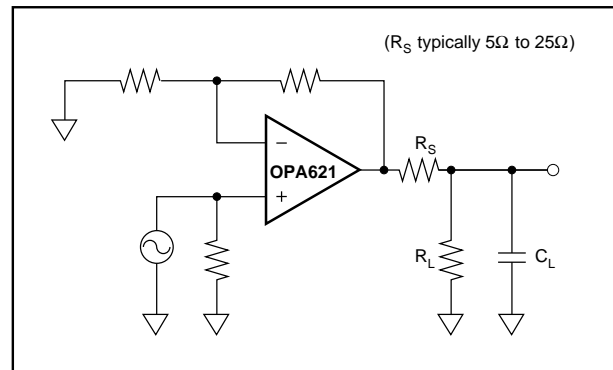


FIGURE 6. Driving Capacitive Loads.

### COMPENSATION

The OPA621 is stable in inverting gains of  $\geq -2V/V$  and in non-inverting gains  $\geq +2V/V$ . Phase margin for both configurations is approximately 50°. Inverting and non-inverting gains of unity should be avoided. The minimum stable gains of +2V/V and -2V/V are the most demanding circuit configurations for loop stability and oscillations are most

likely to occur in these gains. If possible, use the device in a noise gain greater than three to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of  $-2V/V$  is equivalent to a noise gain of 3.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA621 in a good layout is flat with frequency for higher-gain circuits. However, low-gain circuits and configurations where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

## SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of  $\pm 200\mu\text{V}$  centered around the final value of 2V.

Settling time, specified in an inverting gain of two, occurs in only 25ns to 0.01% for a 2V step, making the OPA621 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical

attention to the details as mentioned under “Wiring Precautions.” The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA621 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA621. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional “false-summing junction,” which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope’s built-in calibration source as the input signal.

## DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

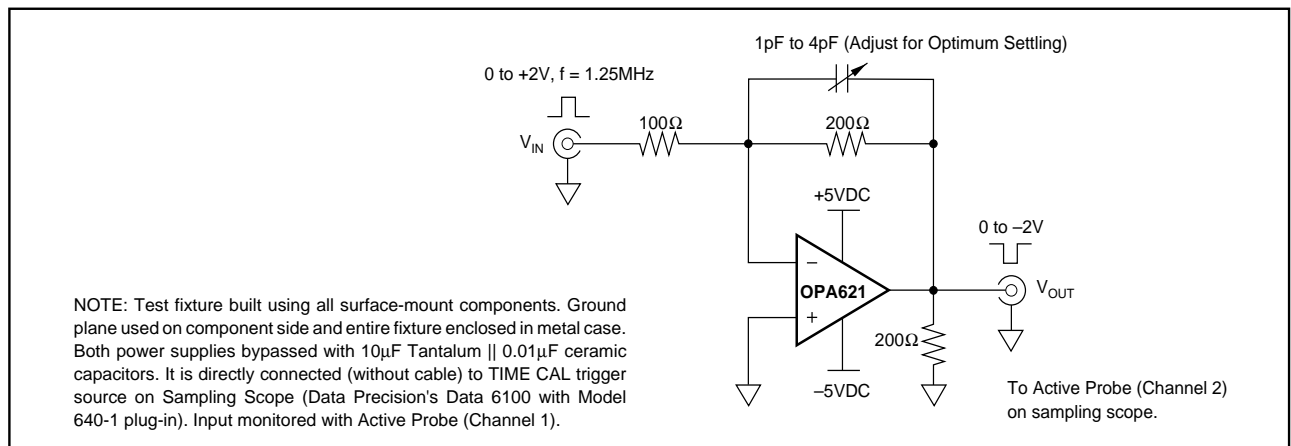


FIGURE 7. Settling Time Test Circuit.

## DISTORTION

The OPA621's Harmonic Distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Two-tone, third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA621's two-tone, third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA621 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +47dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - \text{P}_O)$$

where  $\text{OPI}^3\text{P}$  = third-order output intercept, dBm

$\text{P}_O$  = output level/tone, dBm/tone

Third IMD = third-order intermodulation ratio  
below each output tone, dB

For this case  $\text{OPI}^3\text{P} = 47\text{dBm}$ ,  $\text{P}_O = 10\text{dBm}$ , and the third-order  $\text{IMD} = 2(47 - 10) = 74\text{dB}$  below either 10dBm tone. The OPA621's low IMD makes the device an excellent choice for a variety of RF signal processing applications.

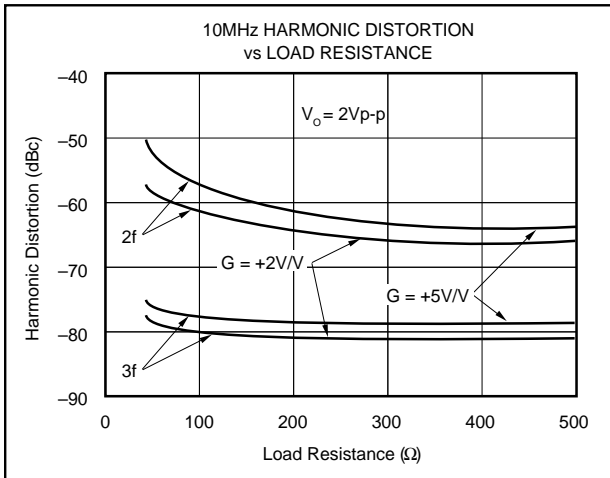


FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

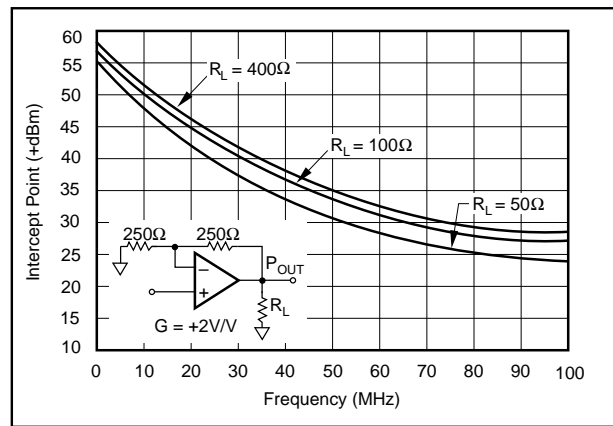


FIGURE 9. Two-Tone Third-Order Intermodulation Intercept vs Frequency.

## NOISE FIGURE

The OPA621's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA621's Noise Figure vs Source Resistance is shown in Figure 10.

## SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA621. Request Burr-Brown Application Bulletin AB-167.

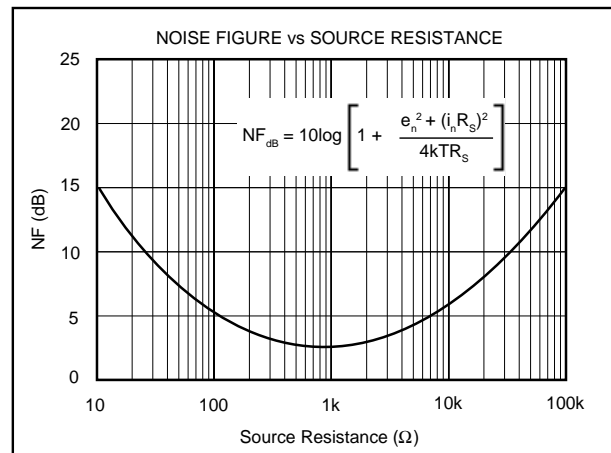


FIGURE 10. Noise Figure vs Source Resistance.

## RELIABILITY DATA

Extensive reliability testing has been performed on the OPA621. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: CerDip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

## ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown “Q-Screening” provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected levels similar to those of MIL-STD-883.

SCREEN	METHOD
Internal Visual	Burr-Brown QC4118
Stabilization Bake	Temperature = 125°C, 24 hrs
Temperature Cycling	Temperature = -55°C to 125°C, 10 cycles
Burn-In Test	Temperature = 125°C, 160 hrs minimum
Hermetic Seal	Fine: He leak rate < 1 X 10 atm cc/s Gross: Perfluorocarbon bubble test
Electrical Tests	As described in specifications tables.
External Visual	Burr-Brown QC5150

NOTE: Q-Screening is available on SG package only.

## DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

## APPLICATIONS

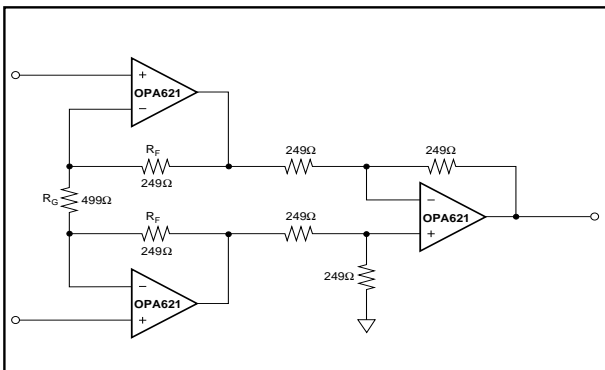


FIGURE 11. Unity Gain Difference Amplifier.

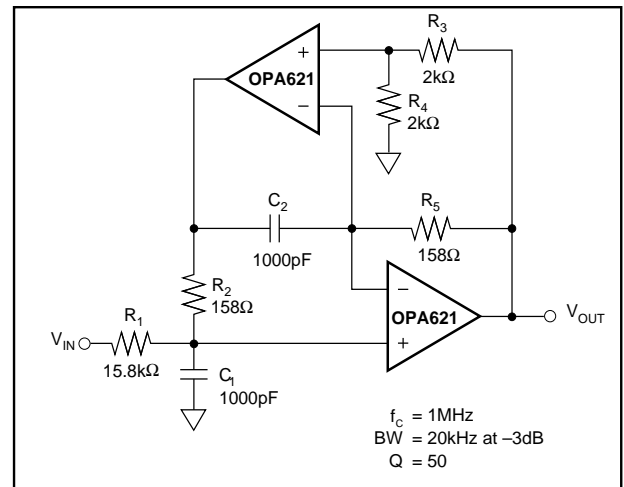


FIGURE 12. High-Q 1MHz Bandpass Filter

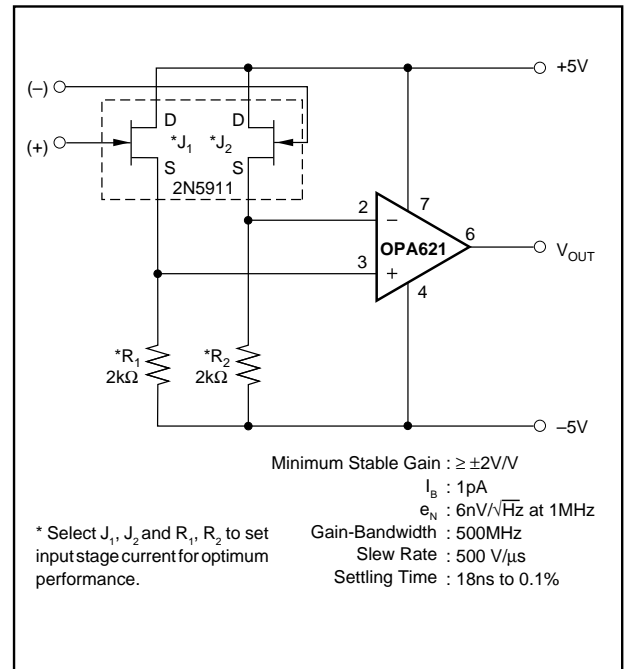


FIGURE 13. Low Noise, Wideband FET Input Op Amp.

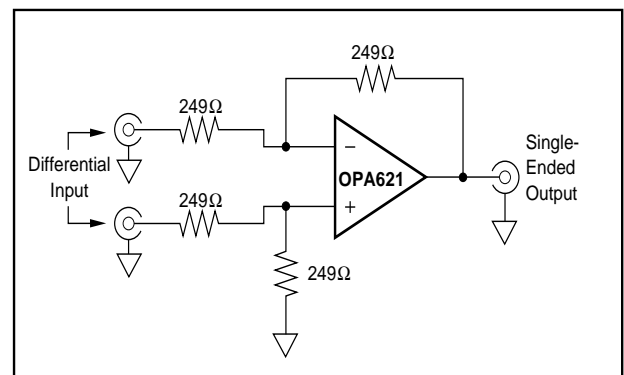


FIGURE 14. Differential Input Buffer Amplifier ( $G = -2V/V$ ).

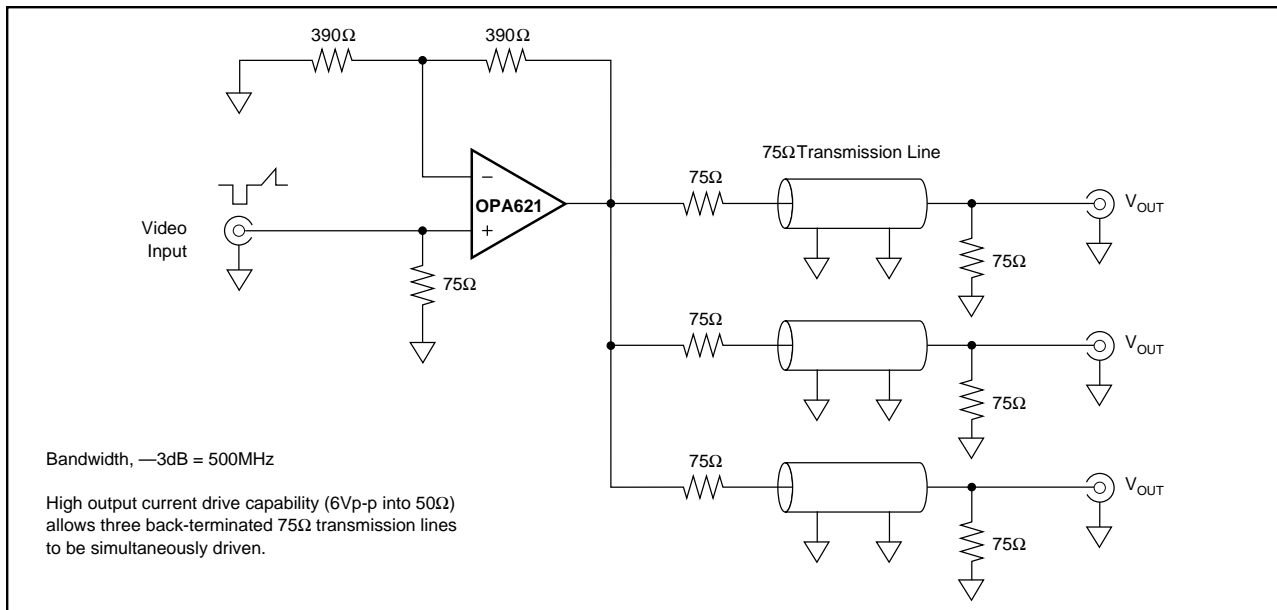
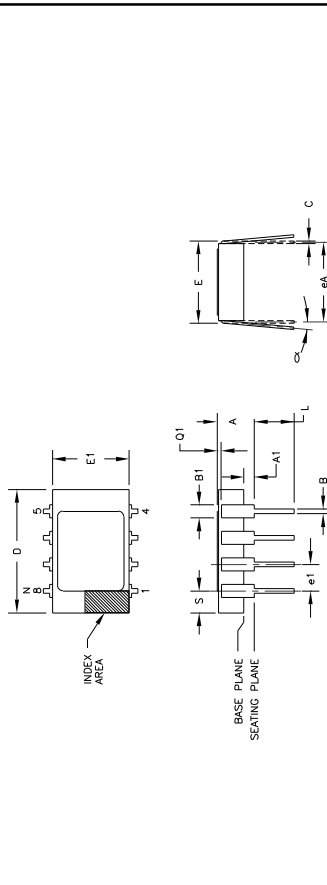


FIGURE 15. Video Distribution Amplifier.



# PACKAGE DRAWINGS

Package Number 187 - 8-Lead, Ceramic Side Brass DP, .300 Wide

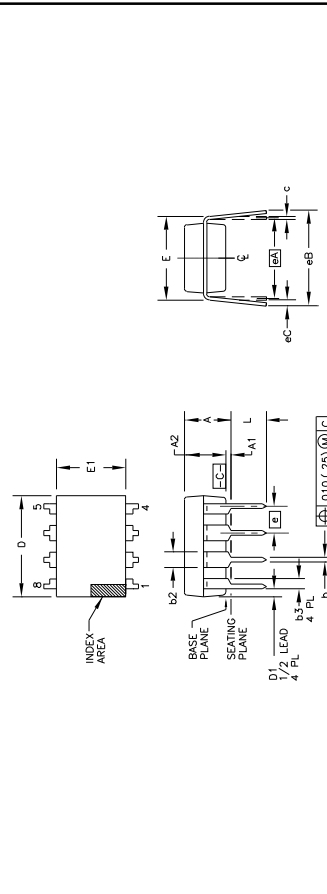


DIM	INCHES		MILLIMETERS		N
	MIN.	MAX.	MIN.	MAX.	
A	.100	.175	2.67	4.45	1
A1	.025	.095	0.64	1.40	3
B	.015	.021	0.38	0.53	5
B1	.038	.060	0.97	1.52	5
C	.008	.012	0.20	0.30	3
D	.380	.550	9.65	13.97	3
E	.290	.325	7.37	8.28	6
F	.100	.100	2.54	2.54	2
EA	.300	TYP.	7.62	TYP.	2
EA	.125	.175	3.18	4.45	4
N	.010	---	2.54	---	4
S	.030	.120	0.76	3.05	5

NOTES:  
 1. DIMENSIONS AND TOLERANCING PER JEDEC STANDARDS Y14.5M-1973.  
 2. LEADS WITHIN .005 IN. (0.13mm) OF TRUE POSITION (TP) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.  
 3.  $\phi$  APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.  
 4. N IS THE NUMBER OF TERMINAL POSITIONS.  
 5. OUTLINES ON WHICH THE SEATING PLANE (A1) OR TERMINAL LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.  
 6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.  
 7. CONTROLLING DIMENSION: INCH.  
 8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: Z1157  
 JEDEC NUMBER: MD-36-AA  
 REV: C

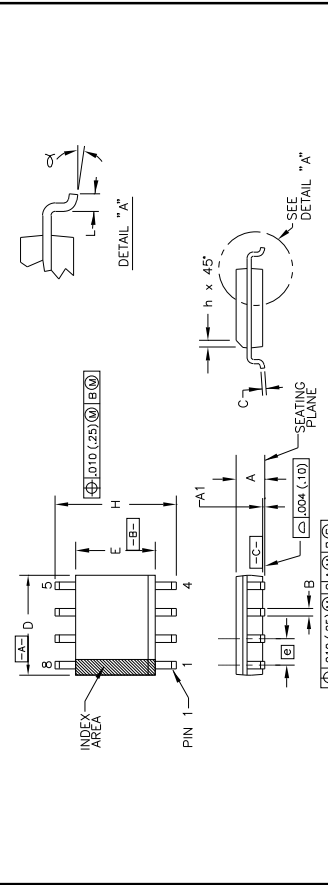
Package Number 008 - 8-Pin Plastic, Single-Wide DP



DIM	INCHES		MILLIMETERS		N
	MIN.	MAX.	MIN.	MAX.	
A	.100	.175	2.54	4.45	1
A1	.015	.021	0.38	0.53	3
A2	.115	.195	2.92	4.95	3
B	.045	.070	1.14	1.78	9
B1	.030	.045	0.76	1.14	9
B2	.008	.014	0.20	0.36	4
C	.355	.400	9.02	10.16	4
D	.005	.005	0.13	0.13	4
E	.240	.280	6.10	7.11	4
EA	.100	BASIC	2.54	BASIC	5
EA	.300	BASIC	7.63	BASIC	5
EB	---	4.30	---	10.92	6

NOTES:  
 1. ALL DIMENSIONS ARE IN INCHES.  
 2. DIMENSIONS AND TOLERANCING PER JEDEC STANDARDS Y14.5M-1973.  
 3. DIMENSIONS -1927, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.  
 4. INCLUDE MOLD FLASH OR PROTRUSIONS, MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).  
 5. CONstrained TO BE PERPENDICULAR TO DATUM [C].  
 6. LEAD TIPS WITH THE LEADS UNCONSTRAINED.  
 7. N IS THE MAXIMUM OF TERMINAL POSITIONS.  
 8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.  
 9. B2 AND B3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS, EXCEED .010 (0.25mm).  
 10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS SHALL NOT BE LESS THAN .005 (0.13mm).  
 11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.  
 12. THE PACKAGE SHALL BE ASYMMETRICAL ABOUT THE LATERAL SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL CENTERLINES.  
 PACKAGE NUMBER: Z2006  
 JEDEC NUMBER: MS-001-BA  
 REV: E

Package Number 182 - 8-Lead 80C



DIM	INCHES		MILLIMETERS		N
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	1
A1	.004	.0098	0.10	0.23	3
B	.013	.020	0.33	0.51	17
C	.0075	.0098	0.20	0.25	5
D	.189	.1968	4.80	4.98	2
E	.145	.152	3.68	3.90	3
F	.100	.100	2.54	2.54	2
H	.2284	.244	5.80	6.20	2
L	.0099	.0196	0.25	0.50	5
L	.016	.050	0.41	1.27	5
N	0	0	0	0	6

NOTES:  
 1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M-1982.  
 2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.  
 3. DIMENSIONS "E" AND "F" DO NOT INCLUDE PROTRUSIONS, INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm).  
 4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, REFER TO DETAIL "A".  
 5. VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.  
 6. "N" IS THE NUMBER OF TERMINAL POSITIONS.  
 7. MEASURED WITH "18" OR GREATER ABOVE THE SEATING PLANE. SHALL NOT EXCEED A VALUE OF .024 IN. (0.61 mm).  
 8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.  
 PACKAGE NUMBER: Z1187  
 JEDEC NUMBER: MS-012-AA  
 REV: G