BURR - BROWN®

# OPA620

# Wideband Precision OPERATIONAL AMPLIFIER

## FEATURES

- LOW NOISE: 2.3nV/√Hz
- HIGH OUTPUT CURRENT: 100mA
- FAST SETTLING: 25ns (0.01%)
- GAIN-BANDWIDTH: 200MHz
- UNITY-GAIN STABLE
- LOW OFFSET VOLTAGE: ±100µV
- LOW DIFFERENTIAL GAIN/PHASE ERROR
- 8-PIN DIP, SOIC PACKAGES

## APPLICATIONS

- LOW NOISE PREAMPLIFIER
- LOW NOISE DIFFERENTIAL AMPLIFIER
- HIGH-RESOLUTION VIDEO
- HIGH-SPEED SIGNAL PROCESSING
- LINE DRIVER
- ADC/DAC BUFFER
- ULTRASOUND
- PULSE/RF AMPLIFIERS
- ACTIVE FILTERS

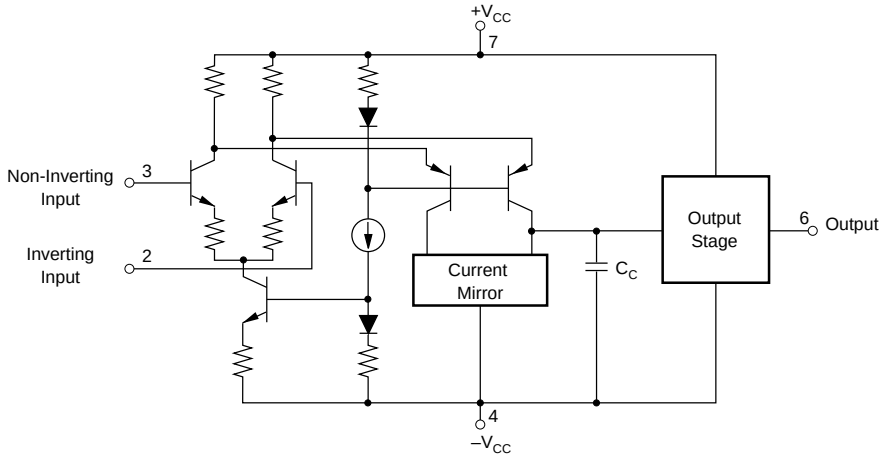
## DESCRIPTION

The OPA620 is a precision wideband monolithic operational amplifier featuring very fast settling time, low differential gain and phase error, and high output current drive capability.

The OPA620 is internally compensated for unity-gain stability. This amplifier has a very low offset, fully symmetrical differential input due to its "classical" operational amplifier circuit architecture. Unlike "current-feedback" amplifier designs, the OPA620 may be used in all op amp applications requiring high speed and precision.

Low noise and distortion, wide bandwidth, and high linearity make this amplifier suitable for RF and video applications. Short-circuit protection is provided by an internal current-limiting circuit.

The OPA620 is available in plastic, ceramic, and SOIC packages. Two temperature ranges are offered: –40°C to +85°C and –55°C to +125°C.




International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132



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# SPECIFICATIONS

## ELECTRICAL

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C unless otherwise noted.

| PARAMETER | CONDITIONS | OPA620KP, KU, KG | | | OPA620SG | | | OPA620LG | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **INPUT NOISE** | | | | | | | | | | | |
| Voltage: $f_O$ = 100Hz | $R_S$ = 0Ω | | 10 | | | * | | | * | | nV/√Hz |
| $f_O$ = 1kHz | | | 5.5 | | | * | | | * | | nV/√Hz |
| $f_O$ = 10kHz | | | 3.3 | | | * | | | * | | nV/√Hz |
| $f_O$ = 100kHz | | | 2.5 | | | * | | | * | | nV/√Hz |
| $f_O$ = 1MHz to 100MHz | | | 2.3 | | | * | | | * | | nV/√Hz |
| $f_B$ = 100Hz to 10MHz | | | 8.0 | | | * | | | * | | µV, rms |
| Current: $f_O$ = 10kHz to 100MHz | | | 2.3 | | | * | | | * | | pA/√Hz |
| **OFFSET VOLTAGE**[1] | | | | | | | | | | | |
| Input Offset Voltage | $V_{CM}$ = 0VDC | | ±200 | ±1mV | | * | * | | ±100 | ±500 | µV |
| Average Drift | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | ±8 | | | * | | | * | | µV/°C |
| Supply Rejection | ±$V_{CC}$ = 4.5V to 5.5V | 50 | 60 | | * | * | | 55 | * | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | $V_{CM}$ = 0VDC | | 15 | 30 | | * | * | | * | 25 | µA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | $V_{CM}$ = 0VDC | | 0.2 | 2 | | * | * | | * | * | µA |
| **INPUT IMPEDANCE** | | | | | | | | | | | |
| Differential | Open-Loop | | 15 \|\| 1 | | | * | | | * | | kΩ \|\| pF |
| Common-Mode | | | 1 \|\| 1 | | | * | | | * | | MΩ \|\| pF |
| **INPUT VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±3.0 | ±3.5 | | * | * | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±2.5VDC, $V_O$ = 0VDC | 65 | 75 | | * | * | | 70 | * | | dB |
| **OPEN-LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 100Ω | 50 | 60 | | * | * | | 55 | * | | dB |
| | $R_L$ = 50Ω | 48 | 58 | | * | * | | 53 | * | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | | | |
| Closed-Loop Bandwidth | Gain = +1V/V | | 300 | | | * | | | * | | MHz |
| (–3dB) | Gain = +2V/V | | 100 | | | * | | | * | | MHz |
| | Gain = +5V/V | | 40 | | | * | | | * | | MHz |
| | Gain = +10V/V | | 20 | | | * | | | * | | MHz |
| Gain-Bandwidth | Gain = +10V/V | | 200 | | | * | | | * | | MHz |
| Differential Gain | 3.58MHz, G = +1V/V | | 0.05 | | | * | | | * | | % |
| Differential Phase | 3.58MHz, G = +1V/V | | 0.05 | | | * | | | * | | Degrees |
| Harmonic Distortion[2] | G = +2V/V, f = 10MHz, $V_O$ = 2Vp-p | | | | | | | | | | |
| | Second Harmonic | | –61 | –50 | | * | * | | * | * | dBc[3] |
| | Third Harmonic | | –65 | –55 | | * | * | | * | * | dBc |
| Full Power Response[2] | $V_O$ = 5Vp-p, Gain = +1V/V | 11 | 16 | | * | * | | * | * | | MHz |
| | $V_O$ = 2Vp-p, Gain = +1V/V | 27 | 40 | | * | * | | * | * | | MHz |
| Slew Rate[2] | 2V Step, Gain = –1V/V | 175 | 250 | | * | * | | * | * | | V/µs |
| Overshoot | 2V Step, Gain = –1V/V | | 10 | | | * | | | * | | % |
| Settling Time: 0.1% | 2V Step, Gain = –1V/V | | 13 | | | * | | | * | | ns |
| 0.01% | | | 25 | | | * | | | * | | ns |
| Phase Margin | Gain = +1V/V | | 60 | | | * | | | * | | Degrees |
| Rise Time | Gain = +1V/V, 10% to 90% | | | | | | | | * | | |
| | $V_O$ = 100mVp-p; Small Signal | | 2 | | | * | | | * | | ns |
| | $V_O$ = 6Vp-p; Large Signal | | 22 | | | * | | | * | | ns |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | $R_L$ = 100Ω | ±3.0 | ±3.5 | | * | * | | * | * | | V |
| | $R_L$ = 50Ω | ±2.5 | ±3.0 | | * | * | | * | * | | V |
| Output Resistance | 1MHz, Gain = +1V/V | | 0.015 | | | * | | | * | | Ω |
| Load Capacitance Stability | Gain = +1V/V | | 20 | | | * | | | * | | pF |
| Short Circuit Current | Continuous | | ±150 | | | * | | | * | | mA |
| **POWER SUPPLY** | | | | | | | | | | | |
| Rated Voltage | ±$V_{CC}$ | | 5 | | | * | | | * | | VDC |
| Derated Performance | ±$V_{CC}$ | 4.0 | | 6.0 | * | | * | * | | * | VDC |
| Current, Quiescent | $I_O$ = 0mADC | | 21 | 23 | | * | * | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification: KP, KU, KG, LG | Ambient Temperature | –40 | | +85 | * | | * | * | | * | °C |
| SG | | | | | –55 | | +125 | | | | °C |
| Operating: KG, LG, SG | Ambient Temperature | | | | –55 | | +125 | –55 | | +125 | °C |
| KP, KU | | –40 | | +85 | | | | | | | °C |
| $\theta_{JA}$ | | | | | | | | | | | |
| KG, LG, SG | | | | | | 125 | | | 125 | | °C/W |
| KP | | | 90 | | | | | | | | °C/W |
| KU | | | 100 | | | | | | | | °C/W |

* Same specifications as for KP/KU.

# SPECIFICATIONS (CONT)

## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.

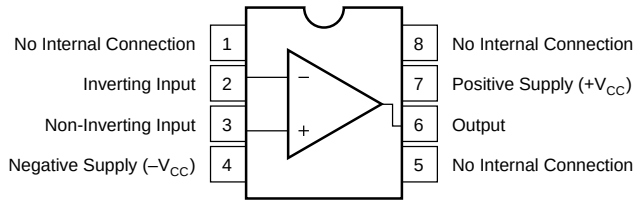
| PARAMETER | CONDITIONS | OPA620KP, KU, KG | | | OPA620SG | | | OPA620LG | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **TEMPERATURE RANGE** | | | | | | | | | | | |
| Specification: KP, KU, KG, LG | Ambient Temperature | –40 | | +85 | * | | * | * | | * | °C |
| SG | | | | | –55 | | +125 | | | | °C |
| **OFFSET VOLTAGE(1)** | | | | | | | | | | | |
| Average Drift | Full Temp. | | ±8 | | | * | | | * | | µV/°C |
| Supply Rejection | 0°C to +70°C ±$V_{CC}$ = 4.5V to 5.5V | 45 | 60 | | * | * | | 50 | * | | dB |
| | Full Temp., ±$V_{CC}$ = 4.5 to 5.5V | 40 | 55 | | * | * | | 45 | * | | dB |
| **BIAS CURRENT** | | | | | | | | | | | |
| Input Bias Current | Full Temp., $V_{CM}$ = 0VDC | | 15 | 40 | | * | * | | * | 35 | µA |
| **OFFSET CURRENT** | | | | | | | | | | | |
| Input Offset Current | Full Temp., $V_{CM}$ = 0VDC | | 0.2 | 5 | | * | * | | * | * | µA |
| **INPUT VOLTAGE RANGE** | | | | | | | | | | | |
| Common-Mode Input Range | | ±2.5 | ±3.0 | | * | * | | * | * | | V |
| Common-Mode Rejection | $V_{IN}$ = ±2.5VDC, $V_O$ = 0VDC | 60 | 75 | | * | * | | 65 | * | | dB |
| **OPEN LOOP GAIN, DC** | | | | | | | | | | | |
| Open-Loop Voltage Gain | $R_L$ = 100Ω | 46 | 60 | | * | * | | 52 | * | | dB |
| | $R_L$ = 50Ω | 44 | 58 | | * | * | | 50 | * | | dB |
| **RATED OUTPUT** | | | | | | | | | | | |
| Voltage Output | 0°C to +70°C, $R_L$ = 100Ω | ±3.0 | ±3.5 | | * | * | | * | * | | V |
| | –40°C to +85°C, $R_L$ = 100Ω | ±2.75 | ±3.25 | | * | * | | * | * | | V |
| | 0°C to +70°C, $R_L$ = 50Ω | ±2.5 | ±3.0 | | * | * | | * | * | | V |
| | –40°C to +85°C, $R_L$ = 50Ω | ±2.25 | ±2.7 | | * | * | | * | * | | V |
| **POWER SUPPLY** | | | | | | | | | | | |
| Current, Quiescent | $I_O$ = 0mADC | | 21 | 25 | | * | * | | * | * | mA |

* Same specifications as for KP/KU.

NOTES: (1) Offset Voltage specifications are also guaranteed with units fully warmed up. (2) Parameter is sample tested. (3) dBc = dB referred to carrier-input signal.

## PIN CONFIGURATION

**Top View** — **8-Pin DIP** **8-Pin SOIC**




## ORDERING INFORMATION

**OPA620 ( ) ( ) (Q)**

- Basic Model Number
- Performance Grade Code
  - K, L = –40°C to +85°C
  - S = –55°C to +125°C
- Package Code
  - G = 8-pin Ceramic DIP
  - P = 8-pin Plastic DIP
  - U = 8-pin Plastic SOIC
- Reliability Screening
  - Q = Q-Screened

## PACKAGE INFORMATION

| MODEL | PACKAGE | PACKAGE DRAWING NUMBER(1) |
|---|---|---|
| OPA620KP | 8-Pin Plastic DIP | 006 |
| OPA620KU | 8-pin Plastic SOIC | 182 |
| OPA602KG | 8-pin Ceramic DIP | 157 |
| OPA620LG | 8-Pin Ceramic DIP | 157 |
| OPA620SG | 8-Pin Ceramic DIP | 157 |

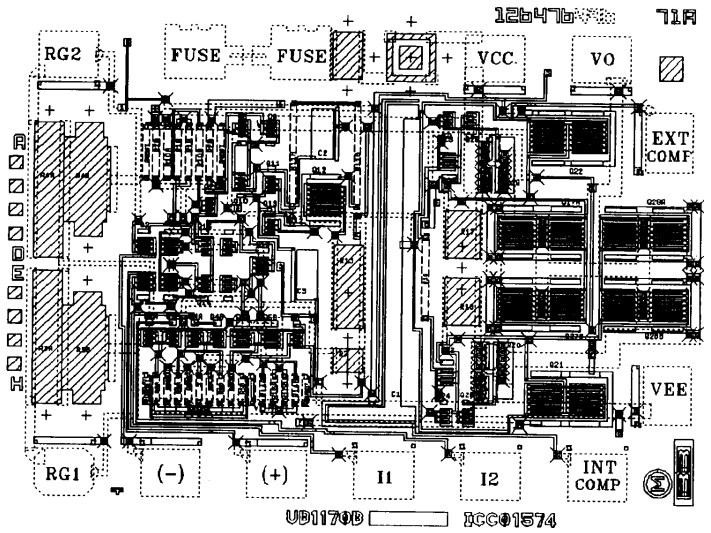
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply | ±7VDC |
| Internal Power Dissipation(1) | See Applications Information |
| Differential Input Voltage | Total $V_{CC}$ |
| Input Voltage Range | See Applications Information |
| Storage Temperature Range: KG, LG, SG | –65°C to +150°C |
| KP, KU | –40°C to +125°C |
| Lead Temperature (soldering, 10s) | +300°C |
| (soldering, SOIC 3s) | +260°C |
| Output Short Circuit to Ground (+25°C) | Continuous to Ground |
| Junction Temperature ($T_J$) | +175°C |

NOTE: (1) Packages must be derated based on specified $\theta_{JA}$. Maximum $T_J$ must be observed.

## DICE INFORMATION




**OPA620 DIE TOPOGRAPHY**

| PAD | FUNCTION | PAD | FUNCTION |
|---|---|---|---|
| 1 | NC | 7 | $-V_{CC}$ |
| 2 | –Input | 8 | NC |
| 3 | +Input | 9 | $V_{OUT}$ |
| 4 | NC | 10 | $+V_{CC}$ |
| 5 | NC | 11 | NC |
| 6 | NC | 12 | NC |
| | | 13 | NC |

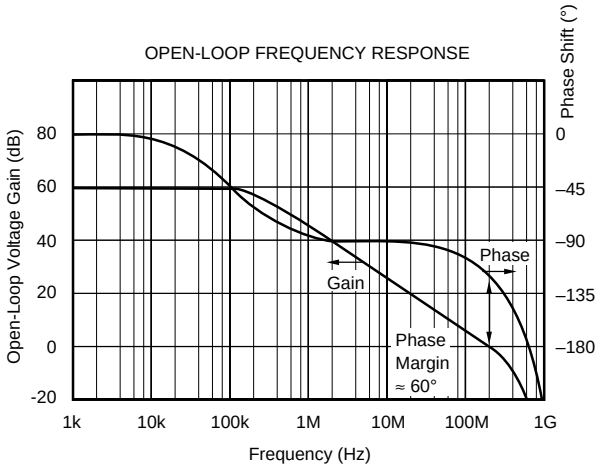
**Substrate Bias:** Negative Supply $-V_{CC}$.

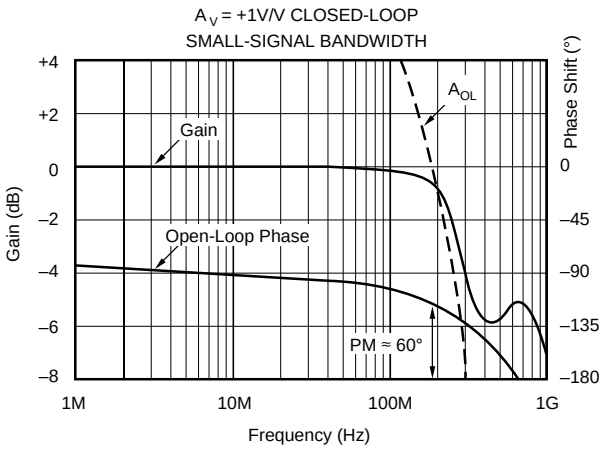
### MECHANICAL INFORMATION

| | MILS (0.001") | MILLIMETERS |
|---|---|---|
| Die Size | 63 x 47 ±5 | 1.22 x 1.83 ±0.13 |
| Die Thickness | 20 ±3 | 0.51 ±0.08 |
| Min. Pad Size | 4 x 4 | 0.10 x 0.10 |
| Backing | | Gold |
| Metalization | | Gold |

# TYPICAL PERFORMANCE CURVES

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C unless otherwise noted.

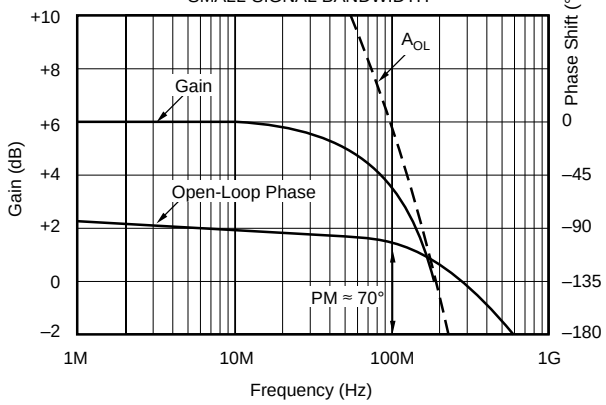


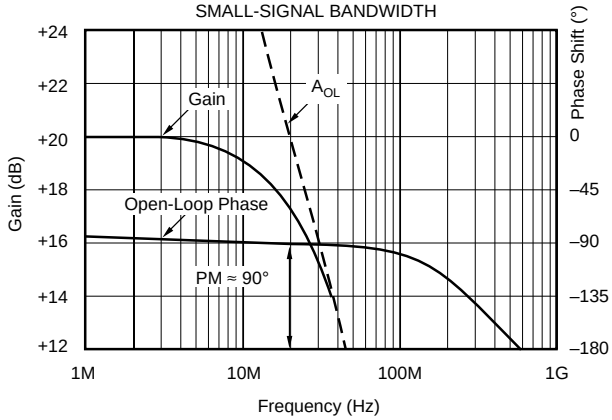
# TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C unless otherwise noted.

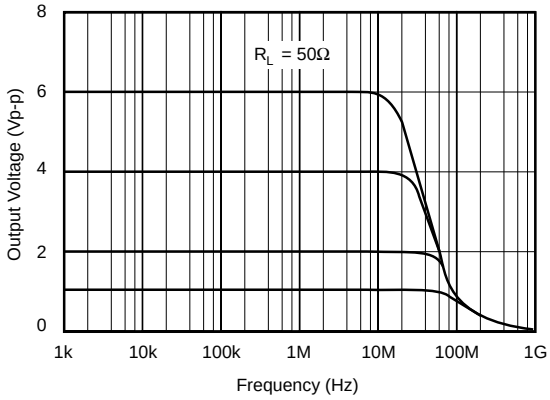
$A_V$ = +2V/V CLOSED-LOOP
SMALL-SIGNAL BANDWIDTH



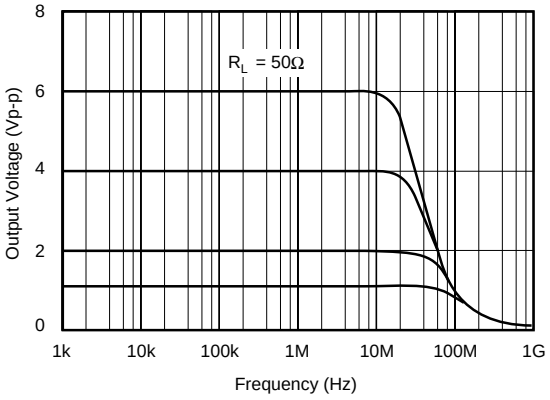

$A_V$ = +10V/V CLOSED-LOOP
SMALL-SIGNAL BANDWIDTH



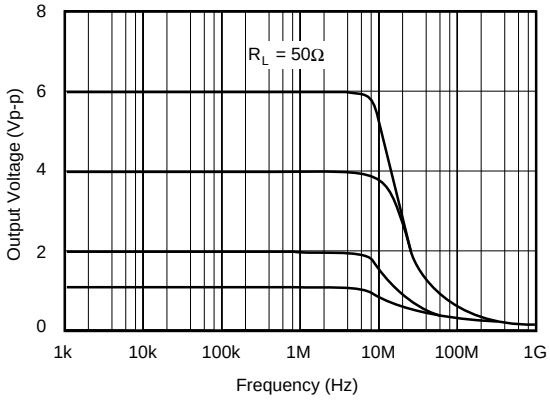

$A_V$ = +1V/V CLOSED-LOOP BANDWIDTH
vs OUTPUT VOLTAGE SWING



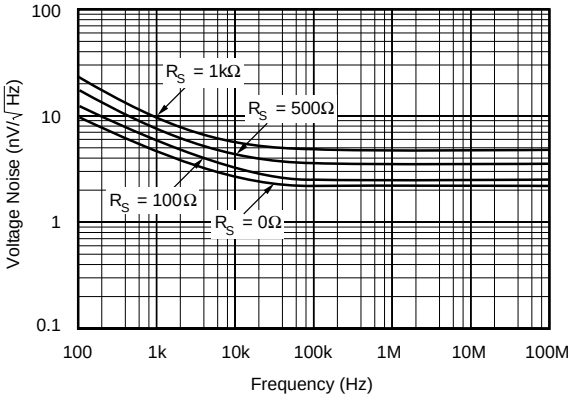

$A_V$ = +2V/V CLOSED-LOOP BANDWIDTH
vs OUTPUT VOLTAGE SWING




$A_V$ = +10V/V CLOSED-LOOP BANDWIDTH
vs OUTPUT VOLTAGE SWING



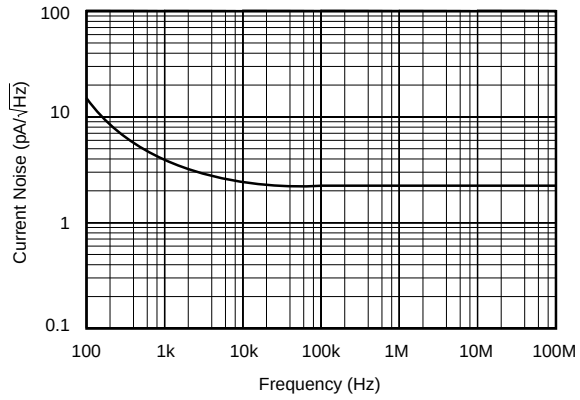

TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY
vs SOURCE RESISTANCE



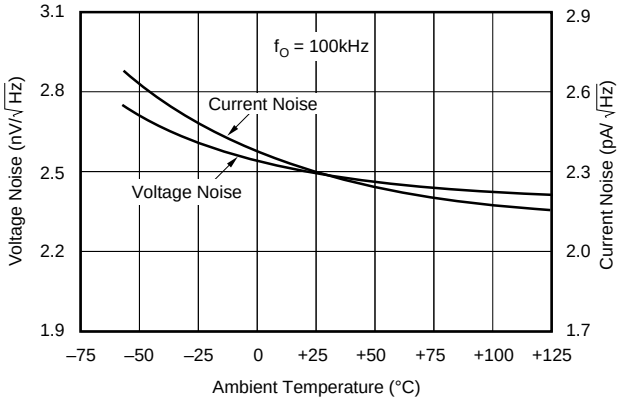
# TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C unless otherwise noted.

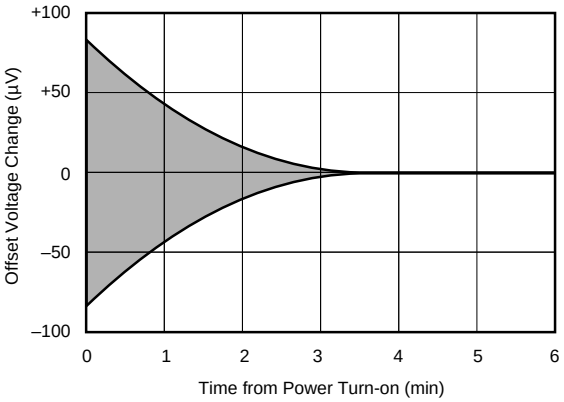
INPUT CURRENT NOISE SPECTRAL DENSITY



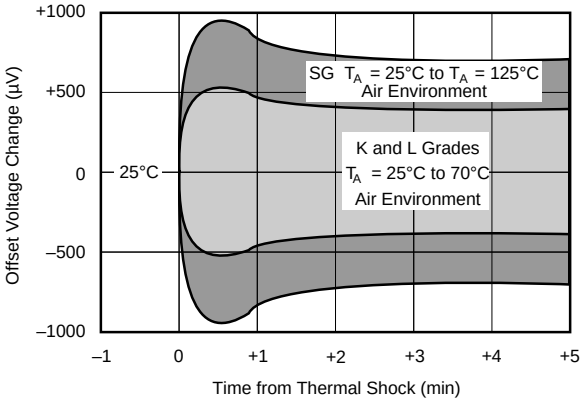

VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



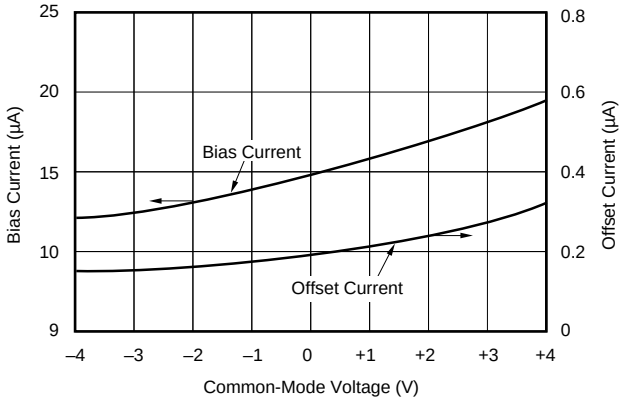

INPUT OFFSET VOLTAGE WARM-UP DRIFT



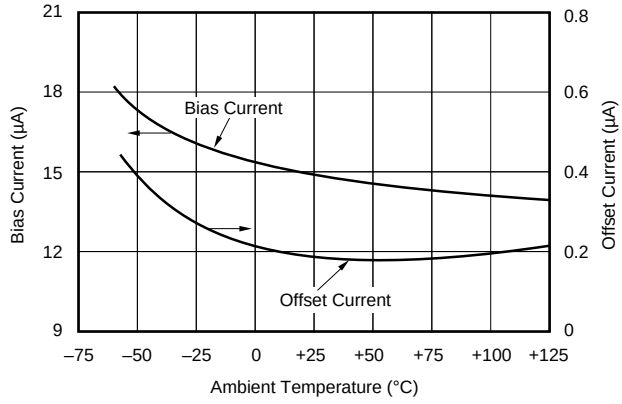

INPUT OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK




BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



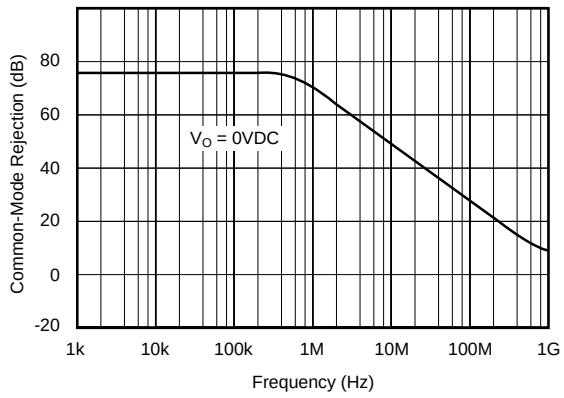

BIAS AND OFFSET CURRENT vs TEMPERATURE



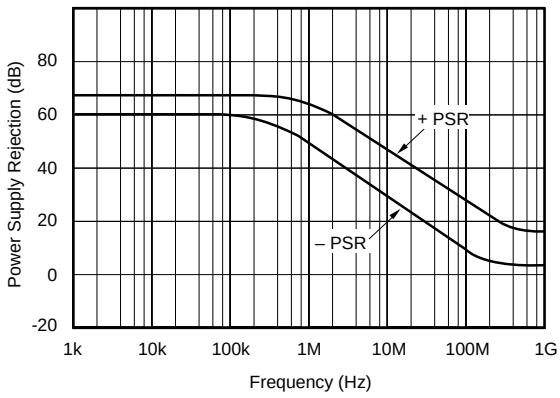
# TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C unless otherwise noted.

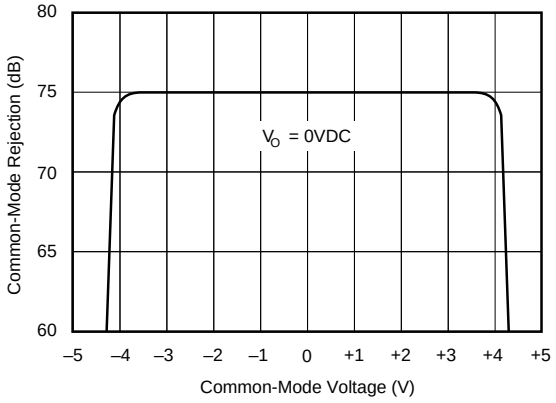
COMMON-MODE REJECTION vs FREQUENCY



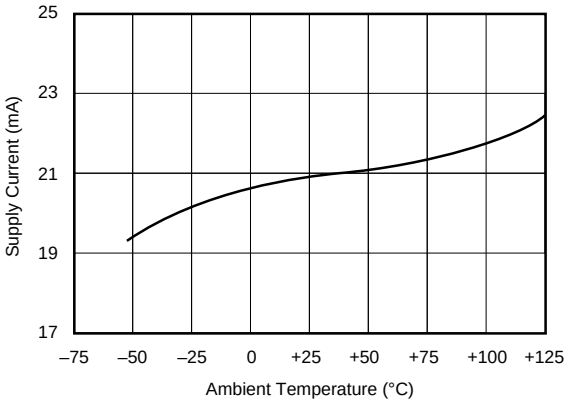

POWER SUPPLY REJECTION vs FREQUENCY



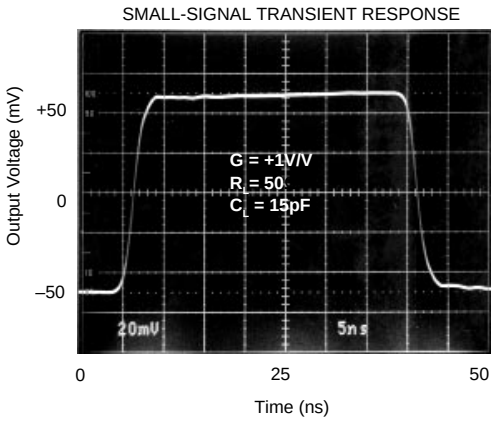

COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



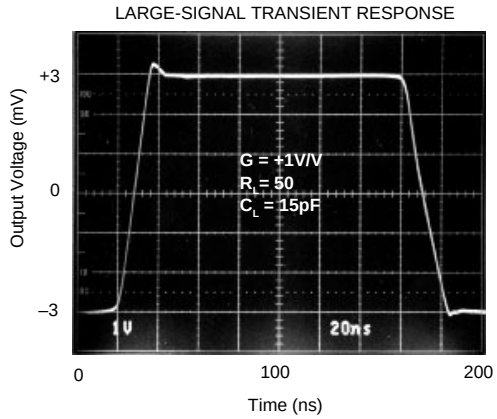

SUPPLY CURRENT vs TEMPERATURE




SMALL-SIGNAL TRANSIENT RESPONSE



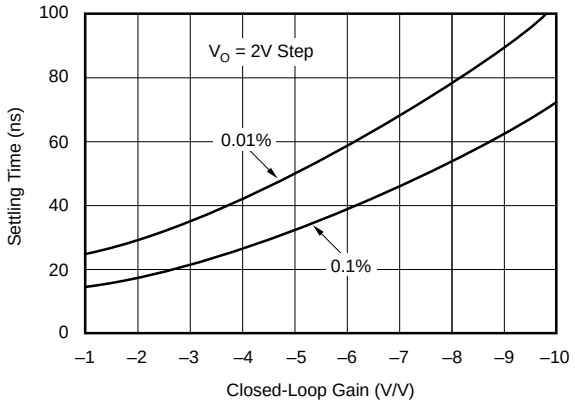

LARGE-SIGNAL TRANSIENT RESPONSE



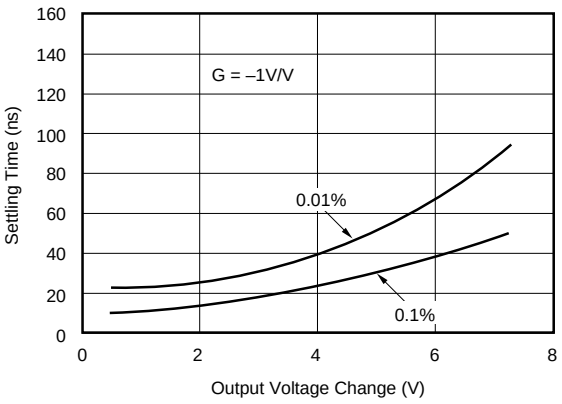
# TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C unless otherwise noted.

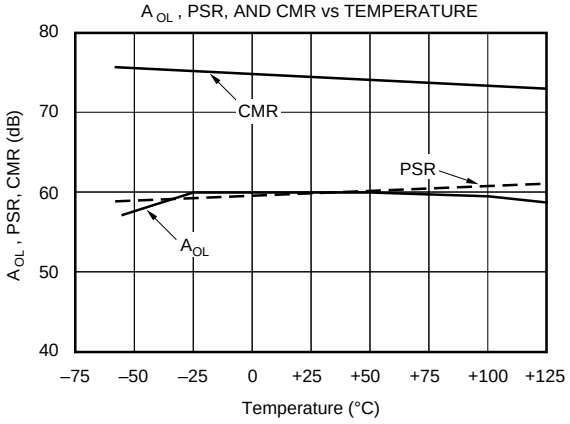
SETTLING TIME vs CLOSED-LOOP GAIN



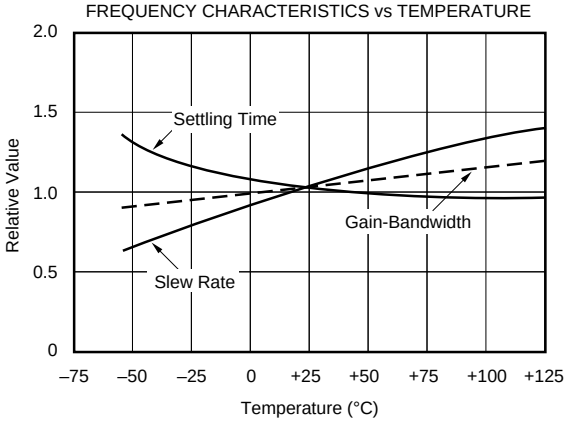

SETTLING TIME vs OUTPUT VOLTAGE CHANGE



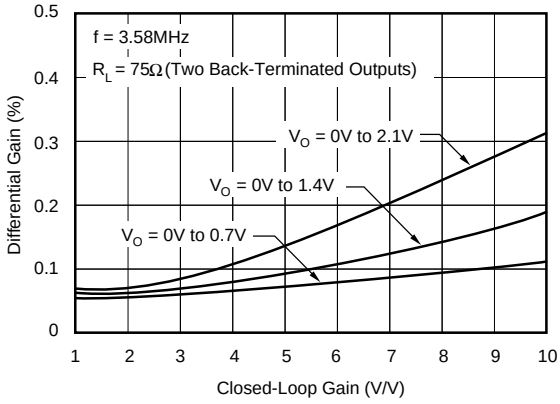

$A_{OL}$, PSR, AND CMR vs TEMPERATURE



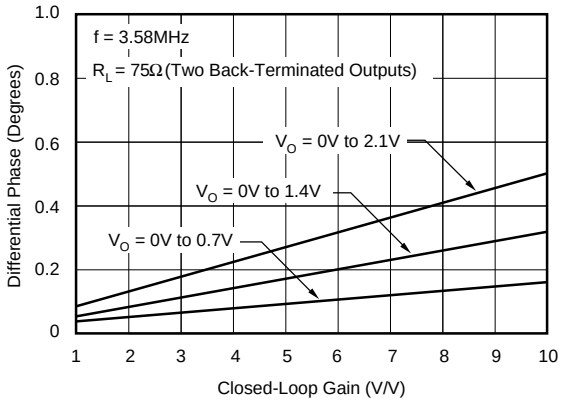

FREQUENCY CHARACTERISTICS vs TEMPERATURE




NTSC DIFFERENTIAL GAIN vs CLOSED-LOOP GAIN



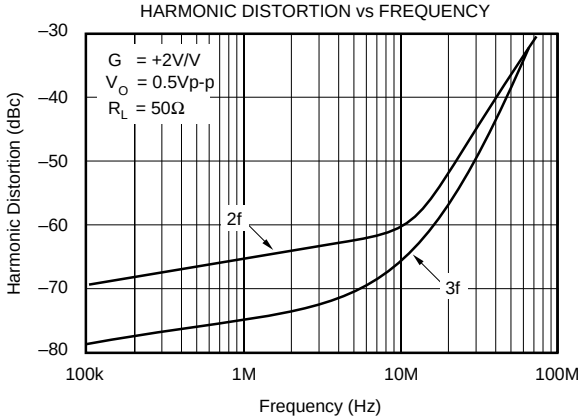

NTSC DIFFERENTIAL PHASE vs CLOSED-LOOP GAIN



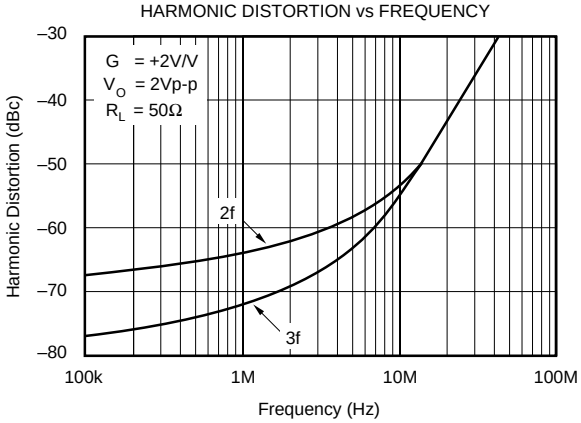
# TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC}$ = ±5VDC, $R_L$ = 100Ω, and $T_A$ = +25°C unless otherwise noted.

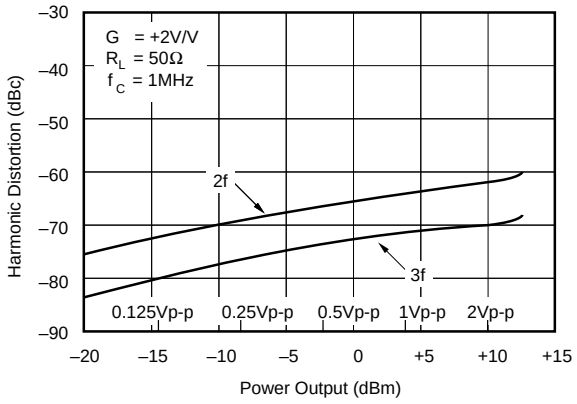
SMALL-SIGNAL
HARMONIC DISTORTION vs FREQUENCY



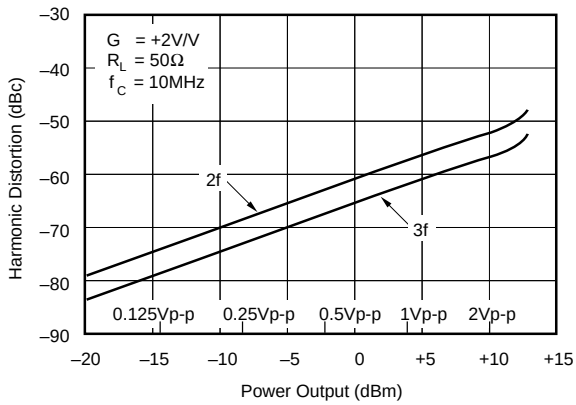

LARGE-SIGNAL
HARMONIC DISTORTION vs FREQUENCY




1MHz HARMONIC DISTORTION
vs POWER OUTPUT




10MHz HARMONIC DISTORTION
vs POWER OUTPUT




# APPLICATIONS INFORMATION

## DISCUSSION OF PERFORMANCE

The OPA620 provides a level of speed and precision not previously attainable in monolithic form. Unlike current feedback amplifiers, the OPA620's design uses a "classical" operational amplifier architecture and can therefore be used in all traditional operational amplifier applications. While it is true that current feedback amplifiers can provide wider bandwidth at higher gains, they offer many disadvantages. The asymmetrical input characteristics of current feedback amplifiers (i.e., one input is a low impedance) prevents them from being used in a variety of applications. In addition, unbalanced inputs make input bias current errors difficult to correct. Bias current cancellation through matching of inverting and non-inverting input resistors is impossible because the input bias currents are uncorrelated. Current noise is also asymmetrical and is usually significantly higher on the inverting input. Perhaps most important, settling time to 0.01% is often extremely poor due to internal design tradeoffs. Many current feedback designs exhibit settling times to 0.01% in excess of 10 *microseconds* even though 0.1% settling times are reasonable. Such amplifiers are completely inadequate for fast settling 12-bit applications.

The OPA620's "classical" operational amplifier architecture employs true differential and fully symmetrical inputs to eliminate these troublesome problems. All traditional circuit configurations and op amp theory apply to the OPA620. The use of low-drift thin-film resistors allows internal operating currents to be laser-trimmed at wafer-level to optimize AC performance such as bandwidth and settling time, as well as DC parameters such as input offset voltage and drift. The result is a wideband, high-frequency monolithic operational amplifier with a gain-bandwidth product of 200MHz, a 0.01% settling time of 25ns, and an input offset voltage of 100µV.

## WIRING PRECAUTIONS

Maximizing the OPA620's capability requires some wiring precautions and high-frequency layout techniques. Oscillation, ringing, poor bandwidth and settling, gain

peaking, and instability are typical problems plaguing all high-speed amplifiers when they are improperly used. In general, all printed circuit board conductors should be wide to provide low resistance, low impedance signal paths. They should also be as short as possible. The entire physical circuit should be as small as practical. Stray capacitances should be minimized, especially at high impedance nodes, such as the amplifier's input terminals. Stray signal coupling from the output or power supplies to the inputs should be minimized. All circuit element leads should be no longer than 1/4 inch (6mm) to minimize lead inductance, and low values of resistance should be used. This will minimize time constants formed with the circuit capacitances and will eliminate stray, parasitic circuits.

Grounding is the most important application consideration for the OPA620, as it is with all high-frequency circuits. Oscillations at frequencies of 200MHz and above can easily occur if good grounding techniques are not used. A heavy ground plane (2 oz. copper recommended) should connect all unused areas on the component side. Good ground planes can reduce stray signal pickup, provide a low resistance, low inductance common return path for signal and power, and can conduct heat from active circuit package pins into ambient air by convection.

Supply bypassing is extremely critical and must *always* be used, especially when driving high current loads. Both power supply leads should be bypassed to ground as close as possible to the amplifier pins. Tantalum capacitors (1µF to 10µF) with very short leads are recommended. Although not required, a parallel 0.01µF ceramic may be added if desired. Surface mount bypass capacitors will produce excellent results due to their low lead inductance. Additionally, suppression filters can be used to isolate noisy supply lines. Properly bypassed and modulation-free power supply lines allow full amplifier output and optimum settling time performance.

**Points to Remember**

1) Don't use point-to-point wiring as the increase in wiring inductance will be detrimental to AC performance. However, if it must be used, very short, direct signal paths are required. The input signal ground return, the load ground return, and the power supply common should all be connected to the same physical point to eliminate ground loops, which can cause unwanted feedback.

2) Good component selection is essential. Capacitors used in critical locations should be a low inductance type with a high quality dielectric material. Likewise, diodes used in critical locations should be Schottky barrier types, such as HP5082-2835 for fast recovery and minimum charge storage. Ordinary diodes will not be suitable in RF circuits.

3) Whenever possible, solder the OPA620 directly into the PC board without using a socket. Sockets add parasitic capacitance and inductance, which can seriously degrade AC performance or produce oscillations. If sockets must be used, consider using zero-profile solderless sockets such as Augat part number 8134-HC-5P2. Alternately, Teflon® standoffs located close to the amplifier's pins can be used to mount feedback components.

4) Resistors used in feedback networks should have values of a few hundred ohms for best performance. Shunt capacitance problems limit the acceptable resistance range to about 1kΩ on the high end and to a value that is within the amplifier's output drive limits on the low end. Metal film and carbon resistors will be satisfactory, but wirewound resistors (even "non-inductive" types) are absolutely *unacceptable* in high-frequency circuits.

5) Surface-mount components (chip resistors, capacitors, etc) have low lead inductance and are therefore strongly recommended. Circuits using all surface-mount components with the OPA620KU (SOIC package) will offer the best AC performance. The parasitic package inductance and capacitance for the SOIC is lower than the both the Cerdip and 8-lead Plastic DIP.

6) Avoid overloading the output. Remember that output current must be provided by the amplifier to drive its own feedback network as well as to drive its load. Lowest distortion is achieved with high impedance loads.

7) Don't forget that these amplifiers use ±5V supplies. Although they will operate perfectly well with +5V and –5.2V, use of ±15V supplies will destroy the part.

8) Standard commercial test equipment has not been designed to test devices in the OPA620's speed range. Benchtop op amp testers and ATE systems will require a special test head to successfully test these amplifiers.

9) Terminate transmission line loads. Unterminated lines, such as coaxial cable, can appear to the amplifier to be a capacitive or inductive load. By terminating a transmission line with its characteristic impedance, the amplifier's load then appears purely resistive.

10) Plug-in prototype boards and wire-wrap boards will not be satisfactory. A clean layout using RF techniques is essential; there are no shortcuts.

## OFFSET VOLTAGE ADJUSTMENT

The OPA620's input offset voltage is laser-trimmed and will require no further adjustment for most applications. However, if additional adjustment is needed, the circuit in Figure 1 can be used without degrading offset drift with temperature. Avoid external adjustment whenever possible since extraneous noise, such as power supply noise, can be inadvertently coupled into the amplifier's inverting input terminal. Remember that additional offset errors can be created by the amplifier's input bias currents. Whenever possible, match the impedance seen by both inputs as is shown with $R_3$. This will reduce input bias current errors to the amplifier's offset current, which is typically only 0.2µA.

## INPUT PROTECTION

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The OPA620 incorporates on-chip ESD protection diodes as shown in Figure 2.

Teflon® E. I. Du Pont de Nemours & Co.

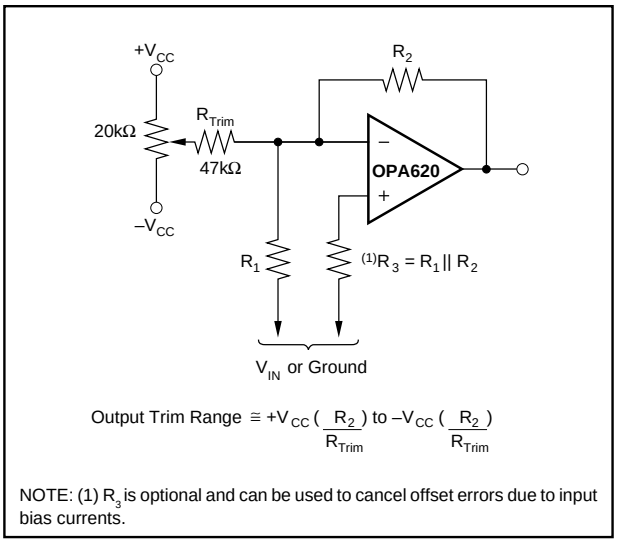



FIGURE 1. Offset Voltage Trim.

This eliminates the need for the user to add external protection diodes, which can add capacitance and degrade AC performance.

All pins on the OPA620 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or so whenever possible.

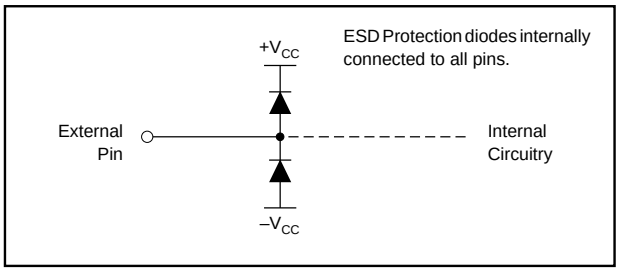



FIGURE 2. Internal ESD Protection.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA620.

## OUTPUT DRIVE CAPABILITY

The OPA620's design uses large output devices and has been optimized to drive 50Ω and 75Ω resistive loads. The device can easily drive 6Vp-p into a 50Ω load. This high-output drive capability makes the OPA620 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Internal current-limiting circuitry limits output current to about 150mA at 25°C. This prevents destruction from accidental shorts to common and eliminates the need for external current-limiting circuitry. Although the device can withstand momentary shorts to either power supply, it is not recommended.

Many demanding high-speed applications such as ADC/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash A/D converters. As shown in Figure 3, the OPA620 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

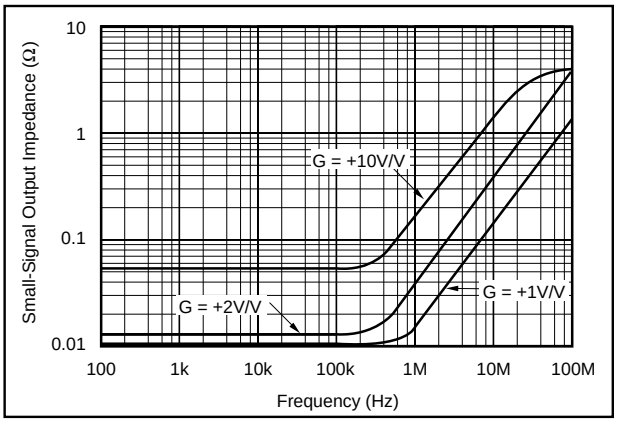



FIGURE 3. Small-Signal Output Impedance vs Frequency.

## THERMAL CONSIDERATIONS

The OPA620 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler, more reliable operation. At extreme temperatures and under full load conditions a heat sink is necessary. See "Maximum Power Dissipation" curve, Figure 4.

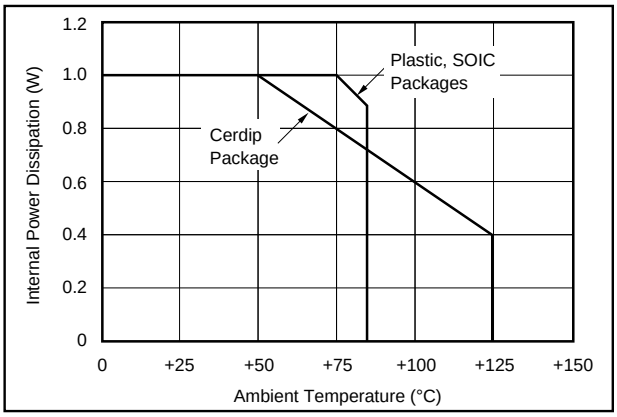



FIGURE 4. Maximum Power Dissipation.

The internal power dissipation is given by the equation $P_D = P_{DQ} + P_{DL}$, where $P_{DQ}$ is the quiescent power dissipation and $P_{DL}$ is the power dissipation in the output stage due to the load. (For $\pm V_{CC} = \pm 5V$, $P_{DQ} = 10V \times 23mA = 230mW$, max). For the case where the amplifier is driving a grounded load ($R_L$) with a DC voltage ($\pm V_{OUT}$) the maximum value of $P_{DL}$ occurs at $\pm V_{OUT} = \pm V_{CC}/2$, and is equal to $P_{DL}$, max = $(\pm V_{CC})^2/4R_L$. Note that it is the voltage across the output transistor, and not the load, that determines the power dissipated in the output stage.

When the output is shorted to common $P_{DL} = 5V \times 150mA = 750mW$. Thus, $P_D = 230mW + 750mW \approx 1W$. Note that the short-circuit condition represents the maximum amount of internal power dissipation that can be generated. Thus, the "Maximum Power Dissipation" curve starts at 1W and is derated based on a 175°C maximum junction temperature and the junction-to-ambient thermal resistance, $\theta_{JA}$, of each package. The variation of short-circuit current with temperature is shown in Figure 5.

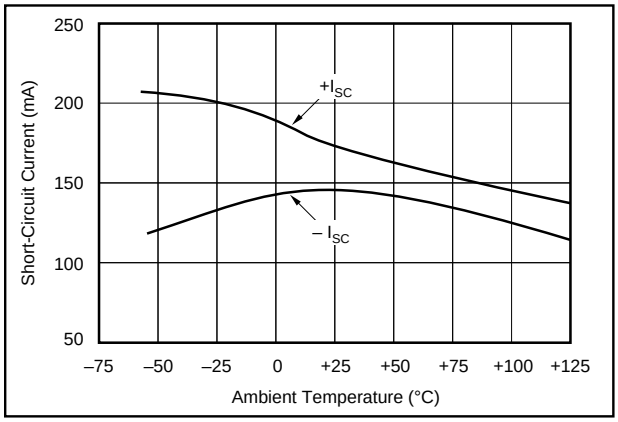



FIGURE 5. Short-Circuit Current vs Temperature.

## CAPACITIVE LOADS

The OPA620's output stage has been optimized to drive resistive loads as low as 50Ω. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high frequency peaking or oscillations. Capacitive loads greater than 20pF should be buffered by connecting a small resistance, usually 5Ω to 25Ω, in series with the output as shown in Figure 6. This is particularly important when driving high capacitance loads such as flash A/D converters.

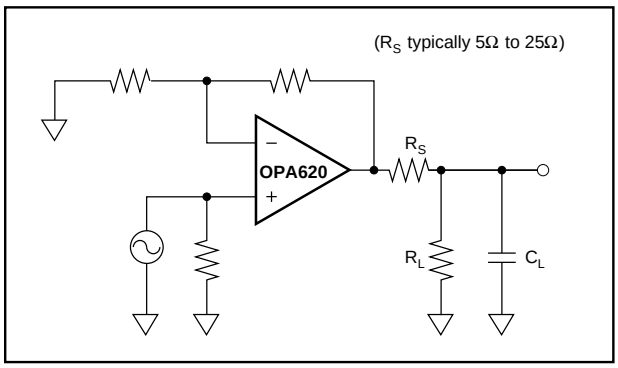



FIGURE 6. Driving Capacitive Loads.

In general, capacitive loads should be minimized for optimum high frequency performance. Coax lines can be driven if the cable is properly terminated. The capacitance of coax cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated in its characteristic impedance.

## COMPENSATION

The OPA620 is internally compensated and is stable in unity gain with a phase margin of approximately 60°. However, the unity gain buffer is the most demanding circuit configuration for loop stability and oscillations are most likely to occur in this gain. If possible, use the device in a noise gain of two or greater to improve phase margin and reduce the susceptibility to oscillation. (Note that, from a stability standpoint, an inverting gain of –1V/V is equivalent to a noise gain of 2.) Gain and phase response for other gains are shown in the Typical Performance Curves.

The high-frequency response of the OPA620 in a good layout is very flat with frequency. However, some circuit configurations such as those where large feedback resistances are used, can produce high-frequency gain peaking. This peaking can be minimized by connecting a small capacitor in parallel with the feedback resistor. This capacitor compensates for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier (typically 2pF after PC board mounting), and the input and feedback resistors. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. Using small resistor values will preserve the phase margin and avoid peaking by keeping the break frequency of this zero sufficiently high. When high closed-loop gains are required, a three-resistor attenuator (tee network) is recommended to avoid using large value resistors with large time constants.

## SETTLING TIME

Settling time is defined as the total time required, from the input signal step, for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the value of the output transition, a 2V step. Thus, settling time to 0.01% requires an error band of ±200µV centered around the final value of 2V.

Settling time, specified in an inverting gain of one, occurs in only 25ns to 0.01% for a 2V step, making the OPA620 one of the fastest settling monolithic amplifiers commercially available. Settling time increases with closed-loop gain and output voltage change as described in the Typical Performance Curves. Preserving settling time requires critical attention to the details as mentioned under "Wiring Precautions." The amplifier also recovers quickly from input overloads. Overload recovery time to linear operation from a 50% overload is typically only 30ns.

In practice, settling time measurements on the OPA620 prove to be very difficult to perform. Accurate measurement is next to impossible in all but the very best equipped labs. Among other things, a fast flat-top generator and high speed oscilloscope are needed. Unfortunately, fast flat-top generators, which settle to 0.01% in sufficient time, are scarce and expensive. Fast oscilloscopes, however, are more commonly available. For best results, a sampling oscilloscope is recommended. Sampling scopes typically have bandwidths that are greater than 1GHz and very low capacitance inputs. They also exhibit faster settling times in response to signals that would tend to overload a real-time oscilloscope.

Figure 7 shows the test circuit used to measure settling time for the OPA620. This approach uses a 16-bit sampling oscilloscope to monitor the input and output pulses. These waveforms are captured by the sampling scope, averaged, and then subtracted from each other in software to produce the error signal. This technique eliminates the need for the traditional "false-summing junction," which adds extra parasitic capacitance. Note that instead of an additional flat-top generator, this technique uses the scope's built-in calibration source as the input signal.

## DIFFERENTIAL GAIN AND PHASE

Differential Gain (DG) and Differential Phase (DP) are among the more important specifications for video applications. DG is defined as the percent change in closed-loop gain over a specified change in output voltage level. DP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both DG and DP are specified at the NTSC sub-carrier frequency of 3.58MHz. DG and DP increase with closed-loop gain and output voltage transition as shown in the Typical Performance Curves. All measurements were performed using a Tektronix model VM700 Video Measurement Set.

## DISTORTION

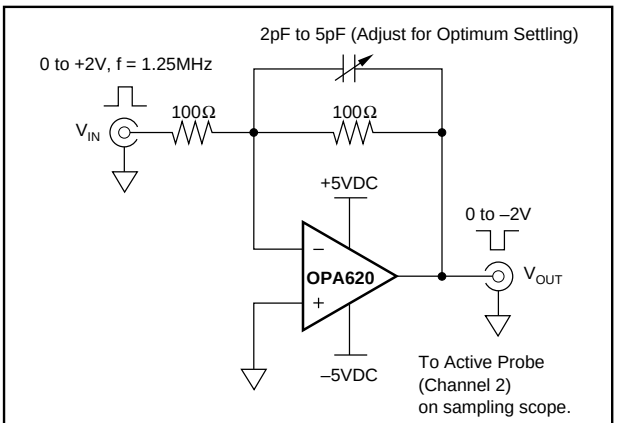
The OPA620's harmonic distortion characteristics into a 50Ω load are shown vs frequency and power output in the Typical Performance Curves. Distortion can be further improved by increasing the load resistance as illustrated in Figure 8. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

Two-tone third-order intermodulation distortion (IM) is an important parameter for many RF amplifier applications. Figure 9 shows the OPA620's two-tone third-order IM intercept vs frequency. For these measurements, tones were spaced 1MHz apart. This curve is particularly useful for determining the magnitude of the third-order IM products as a function of frequency, load resistance, and gain. For example, assume that the application requires the OPA620 to operate in a gain of +2V/V and drive 2Vp-p into 50Ω at a frequency of 10MHz. Referring to Figure 9 we find that the intercept point is +40dBm. The magnitude of the third-order IM products can now be easily calculated from the expression:

$$\text{Third IMD} = 2(\text{OPI}^3\text{P} - P_O)$$

where $\text{OPI}^3\text{P}$ = third-order output intercept, dBm
$P_O$ = output level/tone, dBm/tone
Third IMD = third-order intermodulation ratio below each output tone, dB

For this case $\text{OPI}^3\text{P}$ = 40dBm, $P_O$ = 10dBm, and the third-order IMD = 2(40 – 10) = 60dB below either 10dBm tone. The OPA620's low IMD makes the device an excellent choice for a variety of RF signal processing applications.




NOTE: Test fixture built using all surface-mount components. Ground plane used on component side and entire fixture enclosed in metal case. Both power supplies bypassed with 10µF Tantalum || 0.01µF ceramic capacitors. It is directly connected (without cable) to TIME CAL trigger source on Sampling Scope (Data Precision's Data 6100 with Model 640-1 plug-in). Input monitored with Active Probe (Channel 1).

FIGURE 7. Settling Time Test Circuit.

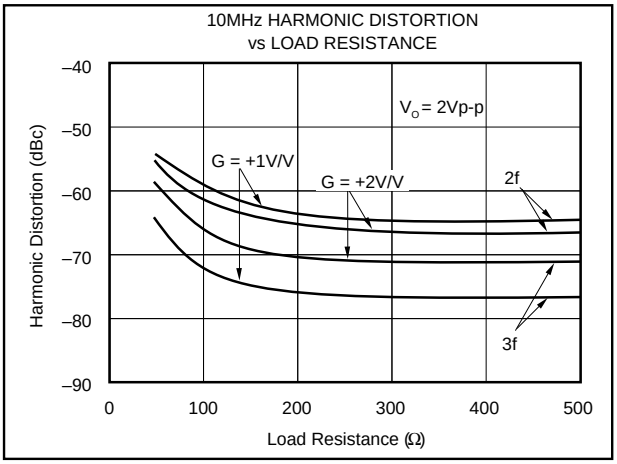



FIGURE 8. 10MHz Harmonic Distortion vs Load Resistance.

## NOISE FIGURE

The OPA620's voltage and current noise spectral densities are specified in the Typical Performance Curves. For RF applications, however, Noise Figure (NF) is often the preferred noise specification since it allows system noise performance to be more easily calculated. The OPA620's Noise Figure vs Source Resistance is shown in Figure 10.

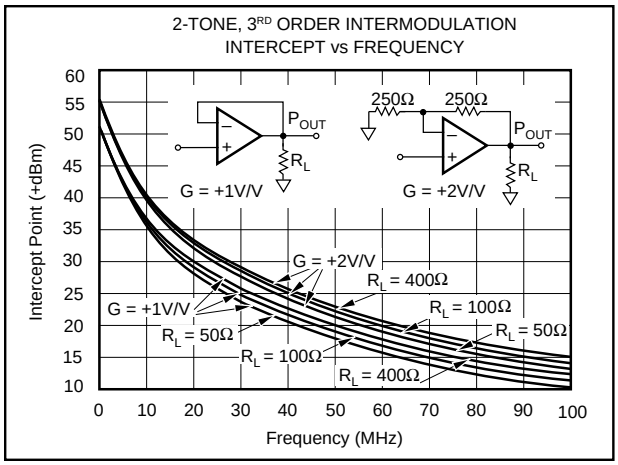



FIGURE 9. 2-Tone, 3rd Order Intermodulation Intercept vs Frequency.

## SPICE MODELS

Computer simulation using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. SPICE models using MicroSim Corporation's PSpice are available for the OPA620. Request Burr-Brown Application Bulletin AB-167.

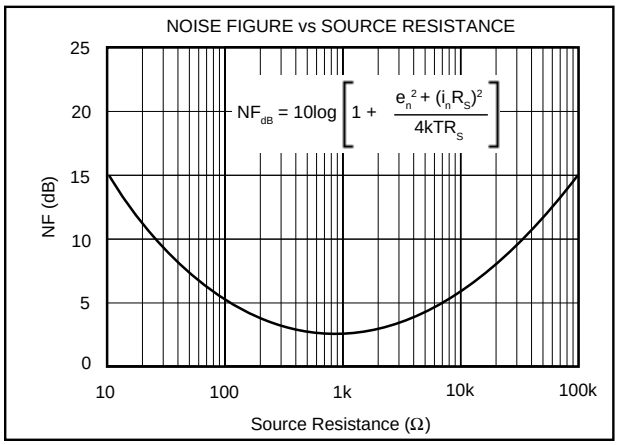



FIGURE 10. Noise Figure vs Source Resistance.

## RELIABILITY DATA

Extensive reliability testing has been performed on the OPA620. Accelerated life testing (2000 hours) at maximum operating temperature was used to calculate MTTF at an ambient temperature of 25°C. These test results yield MTTF of: Cerdip package = 1.31E+9 Hours, Plastic DIP = 5.02E+7 Hours, and SOIC = 2.94E+7 Hours. Additional tests such as PCT have also been performed. Reliability reports are available upon request for each of the package options offered.

## ENVIRONMENTAL (Q) SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown "Q-Screening" provides environmental screening to our standard industrial products, thus enhancing reliability. The screening illustrated in the following table is performed to selected levels similar to those of MIL-STD-883.

| SCREEN | METHOD |
|---|---|
| Internal Visual | Burr-Brown QC4118 |
| Stabilization Bake | Temperature = 125°C, 24 hrs |
| Temperature Cycling | Temperature = –55°C to 125°C, 10 cycles |
| Burn-In Test | Temperature = 125°C, 160 hrs minimum |
| Hermetic Seal | Fine: He leak rate < 1 X 10 atm cc/s<br>Gross: per Fluorocarbon bubble test |
| Electrical Tests | As described in specifications tables. |
| External Visual | Burr-Brown QC5150 |

NOTE: Q-Screening is available on SG package only.

## DEMONSTRATION BOARDS

Demonstration boards to speed prototyping are available. Request DEM1135 for 8-Pin DIP, and DEM1136 for SOIC package.

# APPLICATIONS

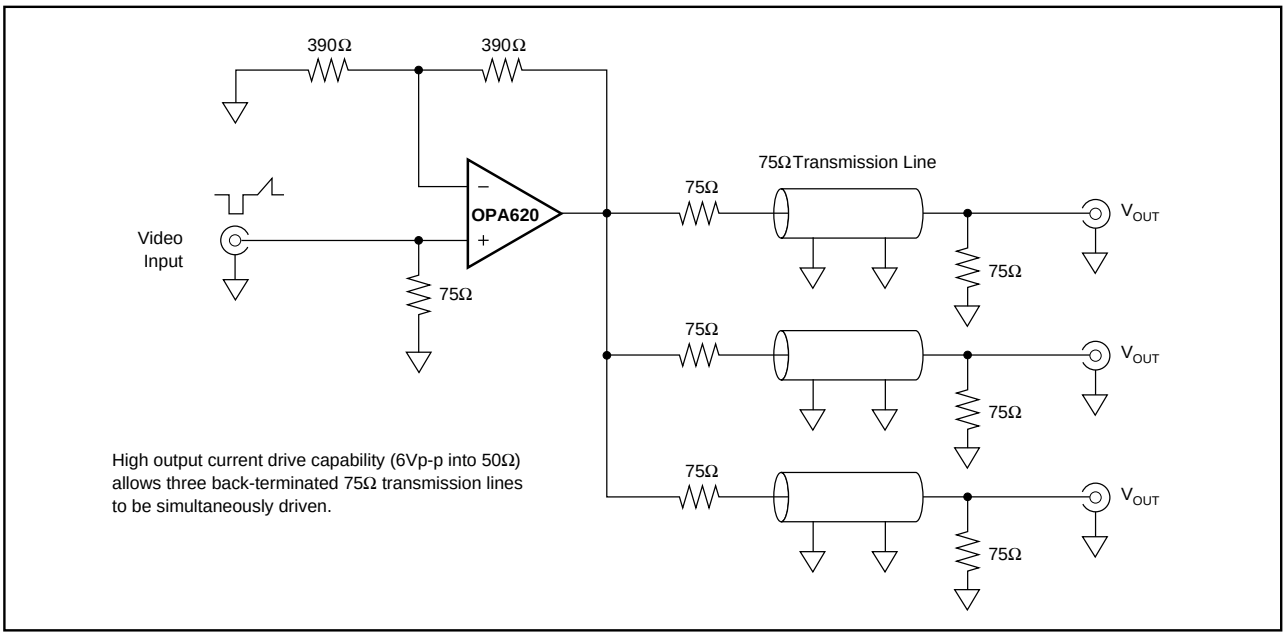



FIGURE 11. Video Distribution Amplifier.

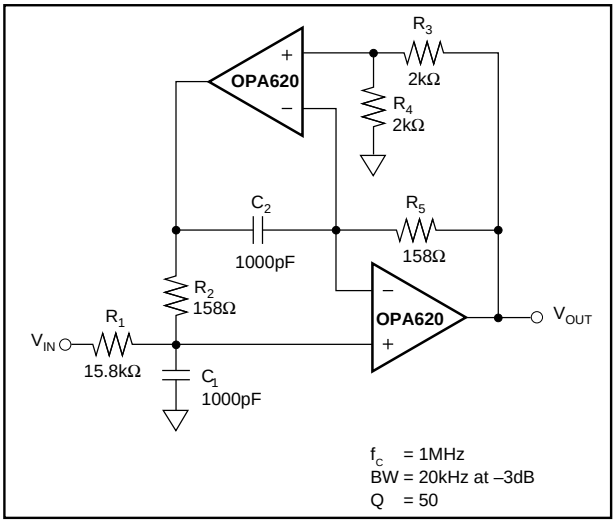



FIGURE 12. High-Q 1MHz Bandpass Filter.

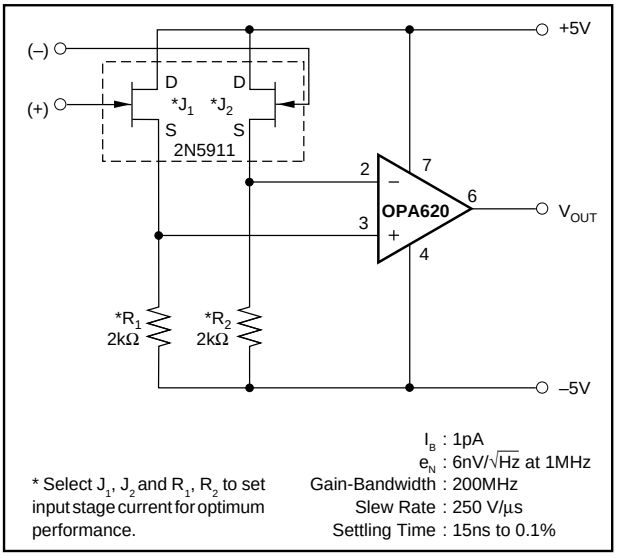



FIGURE 13. Low Noise, Wideband FET Input Op Amp.

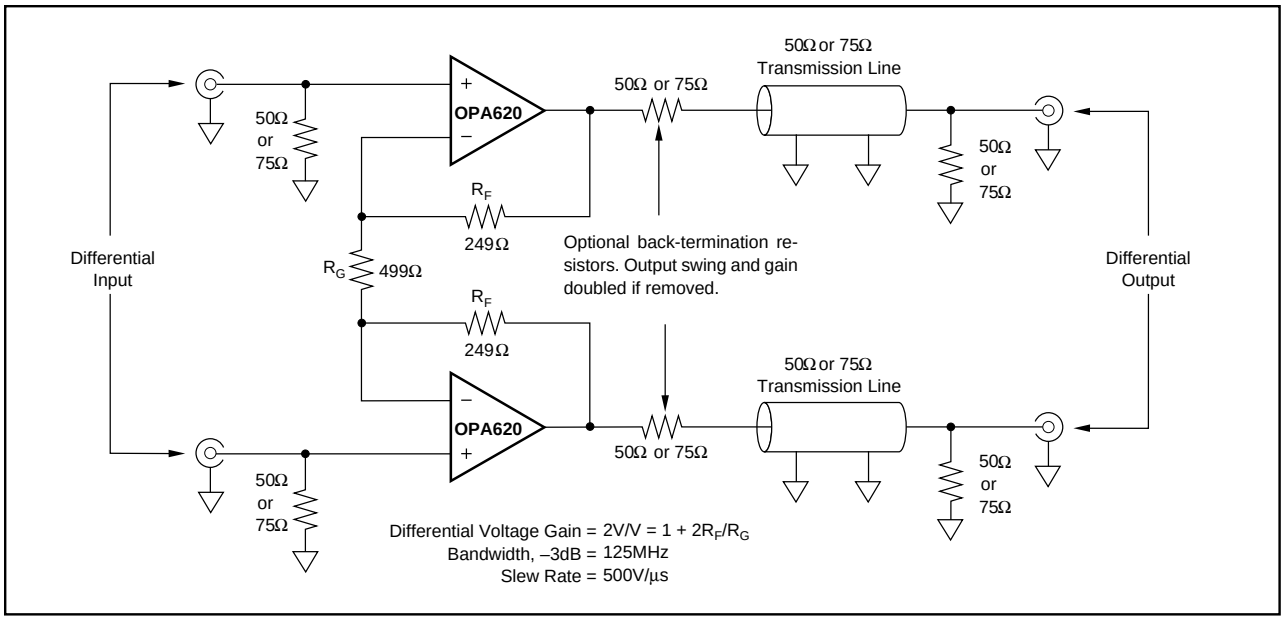



FIGURE 14. Differential Line Driver for 50Ω or 75Ω Systems.

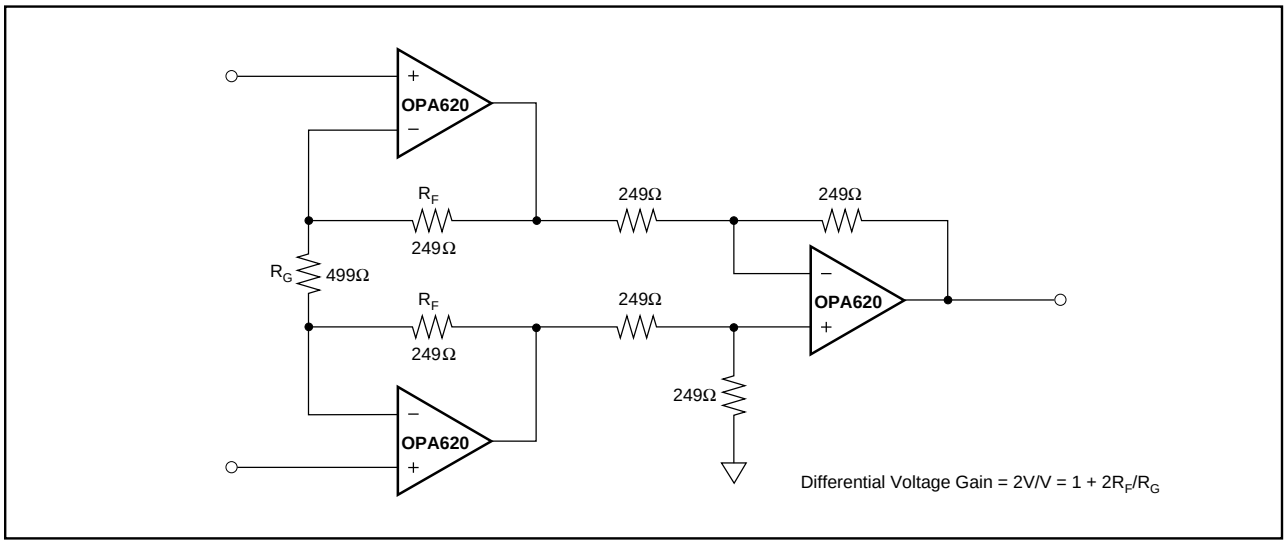



FIGURE 15. Wideband, Fast-Settling Instrumentation Amplifier.

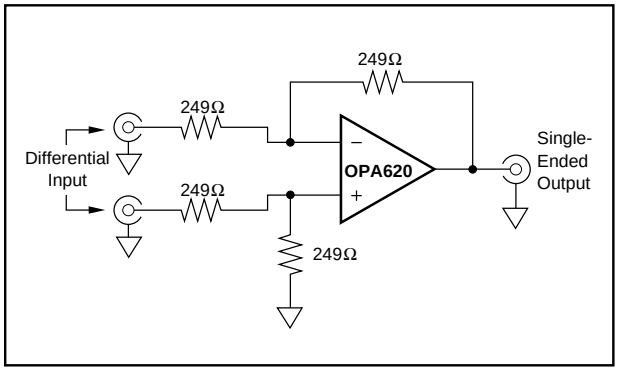



FIGURE 16. Unity Gain Difference Amplifier.

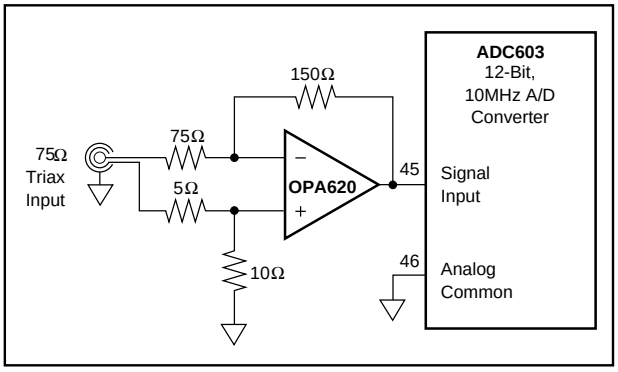
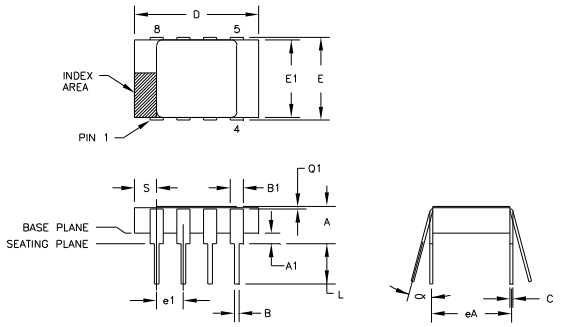



FIGURE 17. Differential Input Buffer Amplifier (G = –2V/V).

## PACKAGE DRAWINGS

**Package Number 157 - 8-Pin Ceramic, Side-Braze DIP**

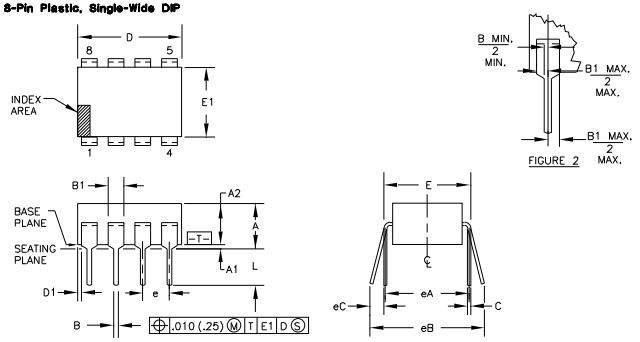



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .105 | .175 | 2.67 | 4.45 | |
| A1 | .025 | .055 | 0.64 | 1.40 | |
| B | .015 | .021 | 0.38 | 0.53 | |
| B1 | .038 | .060 | 0.97 | 1.52 | |
| C | .008 | .012 | 0.20 | 0.30 | |
| D | .380 | .550 | 9.65 | 13.97 | |
| E | .290 | .325 | 7.37 | 8.26 | |
| E1 | .280 | .310 | 7.11 | 7.87 | 6 |
| e1 | .100 | TYP. | 2.54 | TYP. | 2 |
| eA | .300 | TYP. | 7.62 | TYP. | 2 |
| L | .125 | .175 | 3.18 | 4.45 | |
| N | 8 | | 8 | | 4 |
| Q1 | .010 | -- | 2.54 | -- | |
| S | .030 | .120 | 0.76 | 3.05 | |
| α | 0° | 15° | 0° | 15° | 3 |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1973.
2. LEADS WITHIN .13mm (.005) RADIUS OF TRUE POSITION (TP) WITH MAXIMUM MATERIAL CONDITION.
3. α APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
4. N IS THE NUMBER OF TERMINAL POSITIONS.
5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE BASE PLANE (A1 = 0), TERMINALS LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING BASE PLANE.
6. E1 DOES NOT INCLUDE PARTICLES OF PACKAGE MATERIALS.
7. CONTROLLING DIMENSION: INCH.

| PACKAGE NUMBER: ZZ157 | REV.: B |
|---|---|
| JEDEC NUMBER: MO-036 | |

**Package Number 006 - 8-Pin Plastic, Single-Wide DIP**

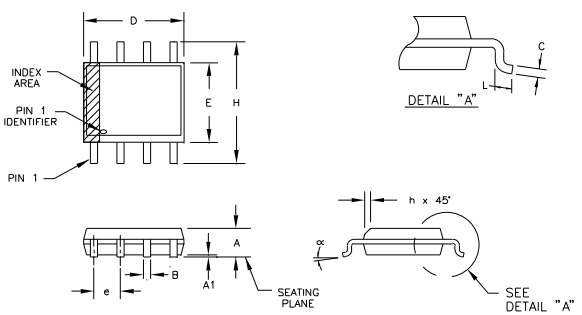



| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | -- | .210 | -- | 5.33 | 3 |
| A1 | .015 | -- | 0.38 | -- | 3 |
| A2 | .115 | .195 | 2.92 | 4.95 | |
| B | .014 | .022 | 0.36 | 0.56 | |
| B1 | .045 | .070 | 1.14 | 1.78 | |
| C | .008 | .015 | 0.20 | 0.38 | |
| D | .348 | .430 | 8.84 | 10.92 | 4 |
| D1 | .005 | -- | 0.13 | -- | |
| E | .300 | .325 | 7.62 | 8.26 | 5 |
| E1 | .240 | .280 | 6.10 | 7.11 | 4 |
| e | .100 | BASIC | 2.54 | BASIC | |
| eA | .300 | BASIC | 7.63 | BASIC | 5 |
| eB | -- | .430 | -- | 10.92 | 6 |
| L | .115 | .160 | 2.92 | 4.06 | 3 |
| N | 8 | | 8 | | 7 |

NOTES:
1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 4, 5, AND 8) MAY BE CONFIGURED AS SHOWN IN FIGURE 2.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

| PACKAGE NUMBER: ZZ006 | REV.: D |
|---|---|
| JEDEC NUMBER: MS-001 | |

**Package Number 182 - 8-Lead SO-8 Surface Mount**




| DIM | INCHES MIN. | INCHES MAX. | MILLIMETERS MIN. | MILLIMETERS MAX. | NOTE |
|---|---|---|---|---|---|
| A | .054 | .068 | 1.37 | 1.73 | |
| A1 | .004 | .009 | 0.10 | 0.23 | |
| B | .014 | .019 | 0.36 | 0.48 | |
| C | .008 | .0098 | 0.20 | 0.25 | |
| D | .189 | .196 | 4.80 | 4.98 | |
| E | .150 | .157 | 3.81 | 3.99 | |
| e | .050 | BASIC | 1.27 | BASIC | |
| H | .229 | .244 | 5.82 | 6.20 | |
| h | .010 | .019 | 0.25 | 0.48 | |
| L | .016 | .050 | 0.41 | 1.27 | |
| N | 8 | | 8 | | |
| α | 0° | 8° | 0° | 8° | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5-1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.086 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

| PACKAGE NUMBER: ZZ182 | REV.: F |
|---|---|
| JEDEC NUMBER: MS-012 | |