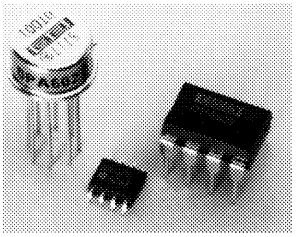
BURR - BROWN®



OPA602

High-Speed Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.5MHz
- HIGH SLEW RATE: 35V/µs
- LOW OFFSET: ±250µV max
- LOW BIAS CURRENT: ±1pA max
- FAST SETTLING TIME: 1µs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DATA CONVERSION

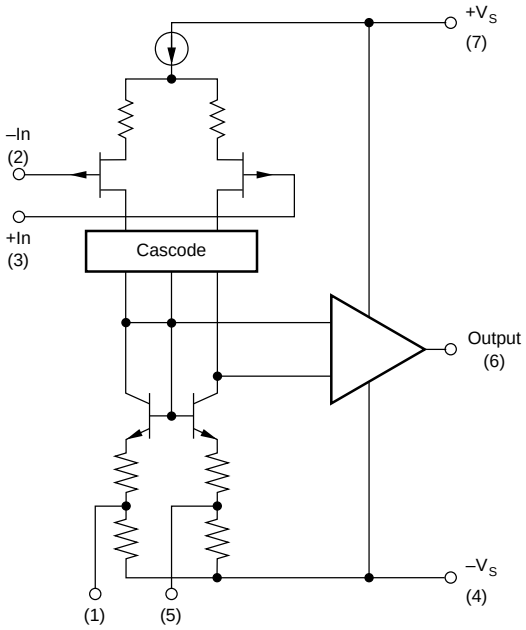
DESCRIPTION

The OPA602 is a precision, wide bandwidth FET operational amplifier. Monolithic ***Difet*** (dielectrically isolated FET) construction provides an unusual combination of high speed and accuracy.

Its wide-bandwidth design minimizes dynamic errors. High slew rate and fast settling time allow accurate signal processing in pulse and data conversion applications. Wide bandwidth and low distortion minimize AC errors. All specifications are rated with a 1kΩ resistor in parallel with 500pF load. The OPA602 is unity-gain stable and easily drives capacitive loads up to 1500pF.

Laser-trimmed input circuitry provides offset voltage and drift performance normally associated with precision bipolar op amps. ***Difet*** construction achieves extremely low input bias currents (1pA max) without compromising input voltage noise.

The OPA602's unique input cascode circuitry maintains low input bias current and precise input characteristics over its full input common-mode voltage range.



Difet® Burr-Brown Corp.

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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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PDS-753E
Printed in U.S.A. August, 1995

SPECIFICATIONS

ELECTRICAL

At V_S = ±15VDC and T_A = +25°C unless otherwise noted.

PARAMETER	CONDITIONS	OPA602AM/AP/AU MIN	OPA602AM/AP/AU TYP	OPA602AM/AP/AU MAX	OPA602BM/SM/BP MIN	OPA602BM/SM/BP TYP	OPA602BM/SM/BP MAX	OPA602CM MIN	OPA602CM TYP	OPA602CM MAX	UNITS
INPUT NOISE											
Voltage: f_O = 10Hz			*			23			*		nV/√Hz
f_O = 100Hz			*			19			*		nV/√Hz
f_O = 1kHz			*			13			*		nV/√Hz
f_O = 10kHz			*			12			*		nV/√Hz
f_B = 10Hz to 10kHz			*			1.4			*		µVrms
f_B = 0.1Hz to 10Hz			*			0.95			*		µVp-p
Current: f_B = 0.1Hz to 10Hz			*			12			*		fAp-p
f_O = 0.1Hz to 20kHz			*			0.6			*		fA/√Hz
OFFSET VOLTAGE											
Input Offset Voltage:											
M Package	V_{CM} = 0VDC		±300	±1000		±150	±500		±100	±250	µV
P Package			1	2		0.5	1				mV
U Package			1	3							mV
Over Specified Temperature											
M Package			±550			±250	±1000		±200	±500	µV
P, U Packages			±1.5			±0.75	±1.5				mV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		*	±15		±3	±5		*	±2	µV/°C
Supply Rejection	$±V_S$ = 12V to 18V	70	*		80	100		86	*		dB
BIAS CURRENT											
Input Bias Current	V_{CM} = 0VDC		±2	±10		±1	±2		±0.5	±1	pA
Over Specified Temperature			±20	±500		±20	±200		±10	±100	pA
SM Grade						±200	±2000				pA
OFFSET CURRENT											
Input Offset Current	V_{CM} = 0VDC		1	10		0.5	2		0.5	1	pA
Over Specified Temperature			20	500		20	200		10	100	pA
SM Grade						200	1000				pA
INPUT IMPEDANCE											
Differential			*			10^{13} || 1			*		Ω || pF
Common-Mode			*			10^{14} || 3			*		Ω || pF
INPUT VOLTAGE RANGE											
Common-Mode Input Range		*	*		±10.2	+13, –11		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	75	*		88	100		92	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	$R_L \geq 1k\Omega$	75	*		88	100		92	*		dB
FREQUENCY RESPONSE											
Gain Bandwidth	Gain = 100	3.5	*		4	6.5		5	*		MHz
Full Power Response	20Vp-p, R_L = 1kΩ		*			570			*		kHz
Slew Rate	V_O = ±10V, R_L = 1kΩ	20	*		24	35		28	*		V/µs
Settling Time: 0.1%	Gain = –1, R_L = 1kΩ		*			0.6			*		µs
0.01%	C_L = 500pF, 10V Step		*			1.0			*		µs
RATED OUTPUT											
Voltage Output	R_L = 1kΩ	±11	*		±11.5	+12.9, –13.8		*	*		V
Current Output	V_O = ±10VDC	*	*		±15	±20		*	*		mA
Output Resistance	1MHz, Open Loop		*			80			*		Ω
Load Capacitance Stability	Gain = +1		*			1500			*		pF
Short Circuit Current		±25	*		±30	±50		*	*		mA
POWER SUPPLY											
Rated Voltage			*			±15			*		VDC
Voltage Range, Derated Performance		*		*	±5		±18	*		*	VDC
Current, Quiescent	I_O = 0mADC		*	*		3	4		*	*	mA
Over Specified Temperature			*	*		3.5	4.5		*	*	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	*		*	–25		+85	*		*	°C
SM Grade					–55		+125				°C
Operating: M Package	Ambient Temperature	*		*	–55		+125	*		*	°C
P, U Packages		–25		+85	–25		+85				°C
Storage: M Package	Ambient Temperature	*		*	–65		+150	*		*	°C
P, U Packages		–40		+125	–40		+125				°C
θ_{JA}			*			200			*		°C/W

* Same specifications as OPA602BM.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18VDC
Internal Power Dissipation ($T_J \leq +175°C$)	1000mW
Differential Input Voltage	Total V_S
Input Voltage Range	$\pm V_S$
Storage Temperature Range	
M Package	–65°C to +150°C
P and U Packages	–40°C to +125°C
Operating Temperature Range	
M Package	–55°C to +125°C
P and U Packages	–25°C to + 85°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C
Output Short Circuit to Ground (+25°C)	Continuous
Junction Temperature	+175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER[1]
OPA602AM	TO-99	001
OPA602BM	TO-99	001
OPA602CM	TO-99	001
OPA602SM	TO-99	001
OPA602AP	Plastic DIP	006
OPA602BP	Plastic DIP	006
OPA602AU	Plastic SOIC	182

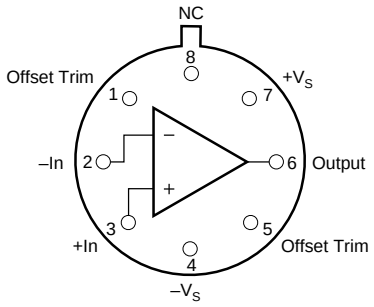
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (µV) AT 25°C
OPA602AM	TO-99	–25 to +85°C	±1000
OPA602BM	TO-99	–25 to +85°C	±500
OPA602CM	TO-99	–25 to +85°C	±250
OPA602SM	TO-99	–55 to +125°C	±500
OPA602AP	Plastic DIP	–25 to +85°C	±2000
OPA602BP	Plastic DIP	–25 to +85°C	±1000
OPA602AU	Plastic SOIC	–25 to +85°C	±3000

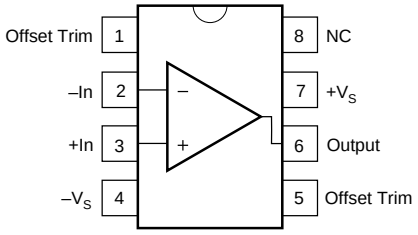
PIN CONFIGURATIONS

Top View — TO-99

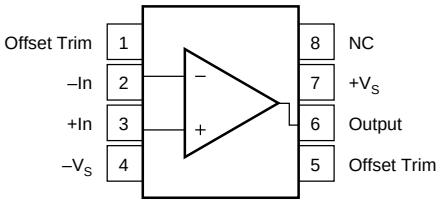


Case Connected to $+V_S$.

Top View — DIP



Top View — SOIC



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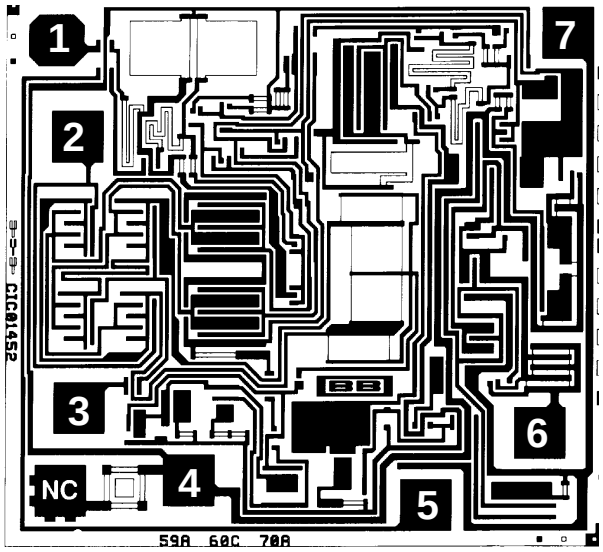
DICE INFORMATION



OPA602 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	–In
3	+In
4	$-V_S$
5	Offset Trim
6	Output
7	$+V_S$

Substrate Bias: $-V_S$
NC: No Connection.

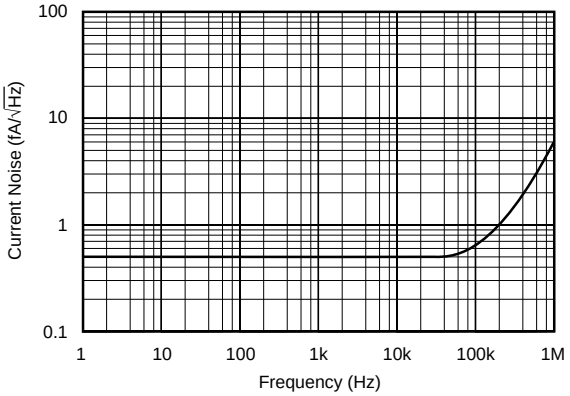
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	63 x 58 ±5	1.60 x 1.47 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None
Transistor Count		36

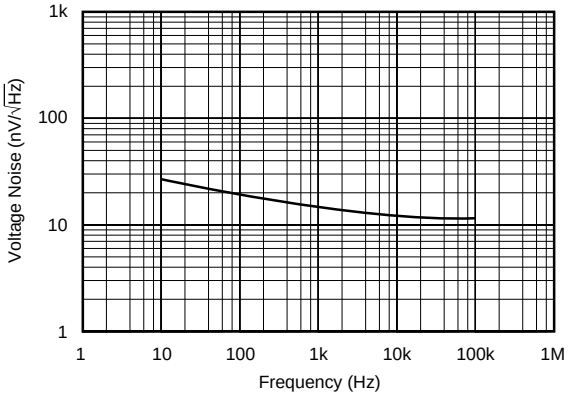
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

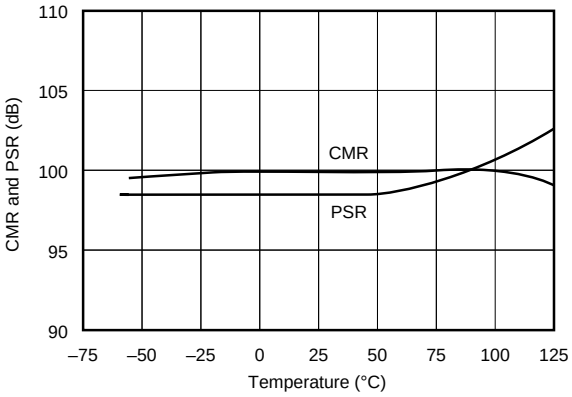
INPUT CURRENT NOISE SPECTRAL DENSITY



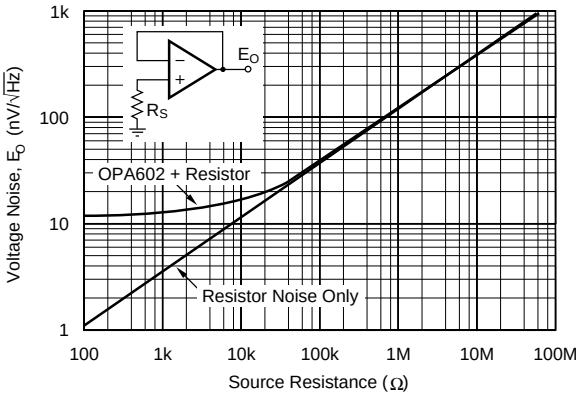
INPUT VOLTAGE NOISE SPECTRAL DENSITY



POWER SUPPLY REJECTION AND COMMON-MODE REJECTION vs TEMPERATURE



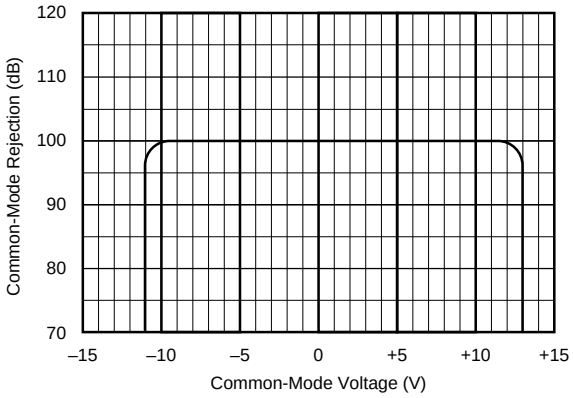
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



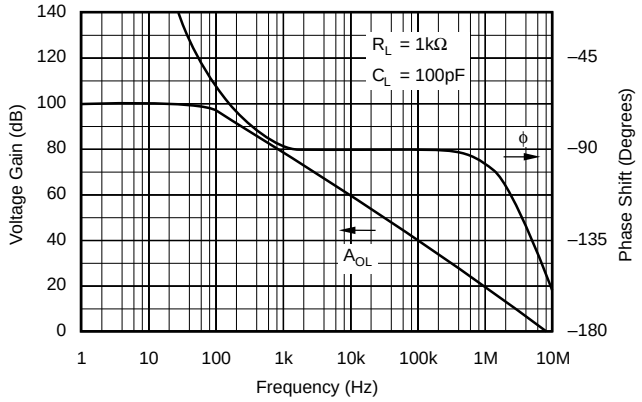
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

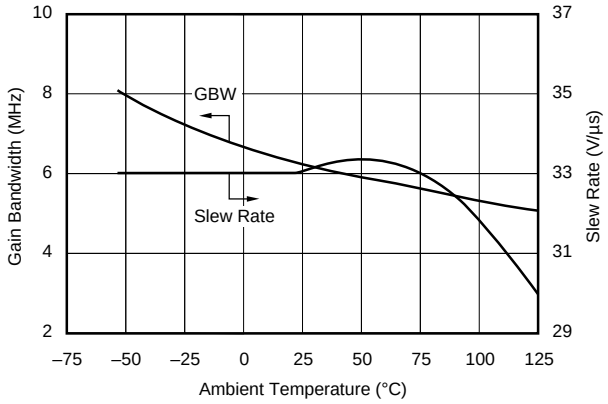
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



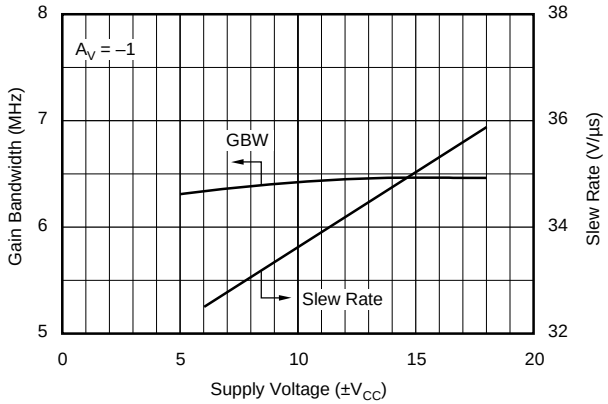
OPEN-LOOP FREQUENCY RESPONSE



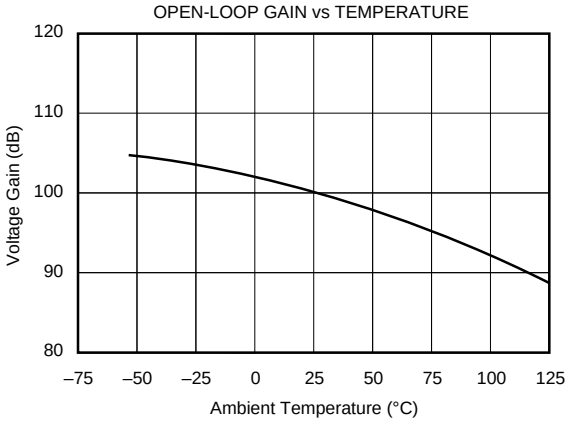
GAIN BANDWIDTH AND SLEW RATE
vs TEMPERATURE



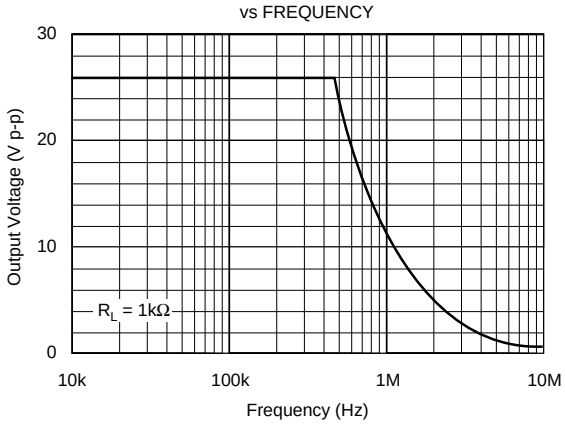
GAIN BANDWIDTH AND SLEW RATE
vs SUPPLY VOLTAGE



OPEN-LOOP GAIN vs TEMPERATURE



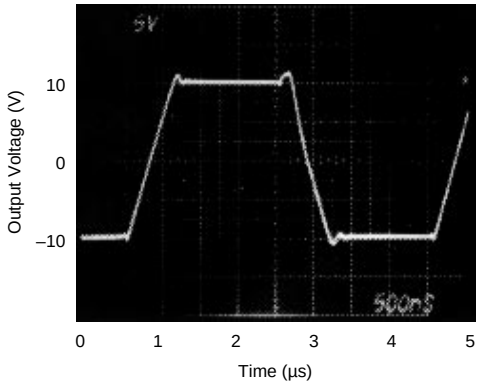
MAXIMUM OUTPUT VOLTAGE SWING
vs FREQUENCY



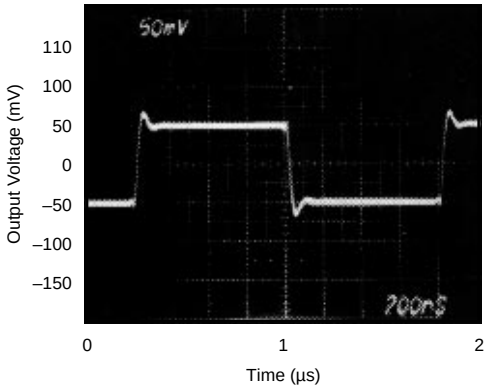
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.

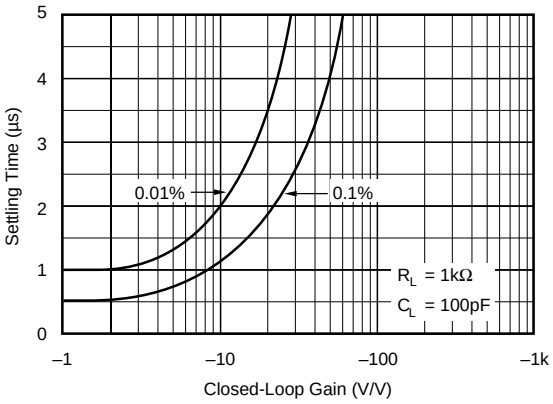
LARGE SIGNAL TRANSIENT RESPONSE



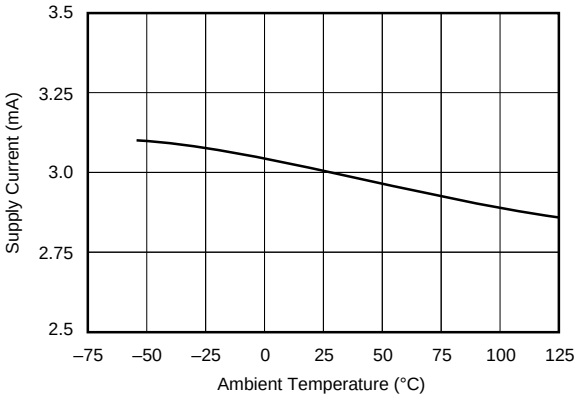
SMALL SIGNAL TRANSIENT RESPONSE



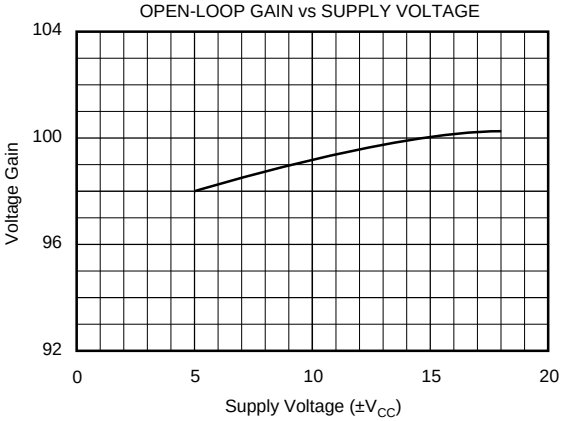
SETTLING TIME vs CLOSED-LOOP GAIN



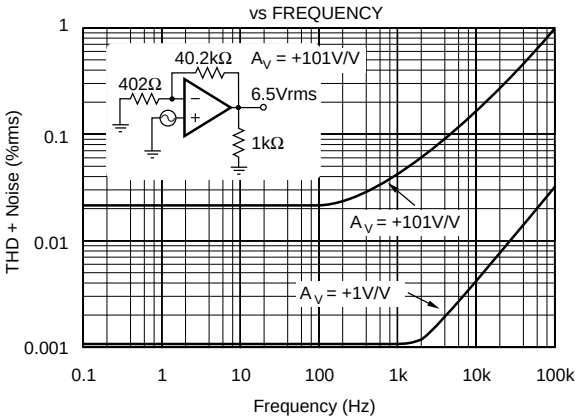
SUPPLY CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

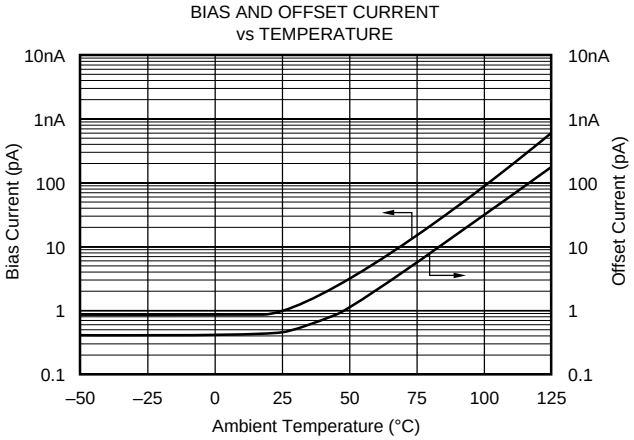


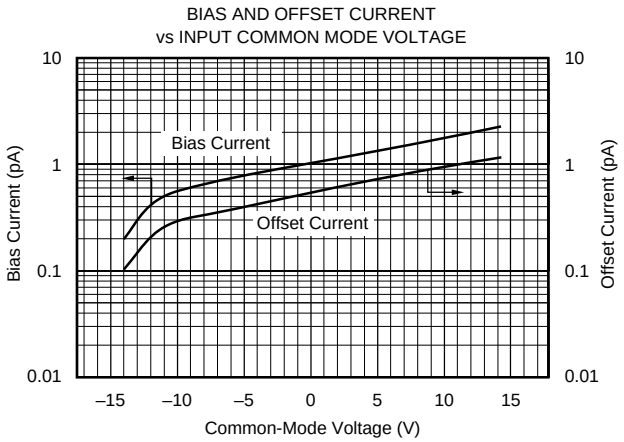
TOTAL HARMONIC DISTORTION vs FREQUENCY

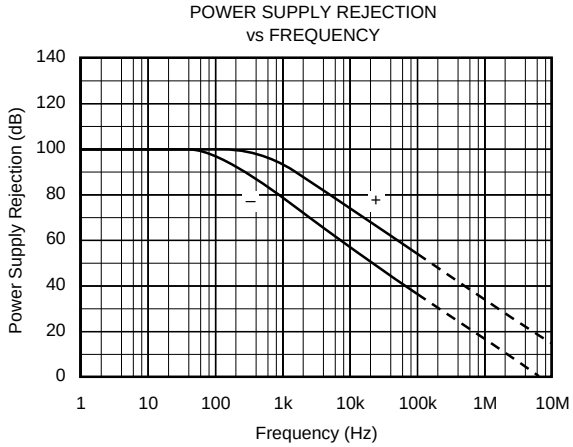


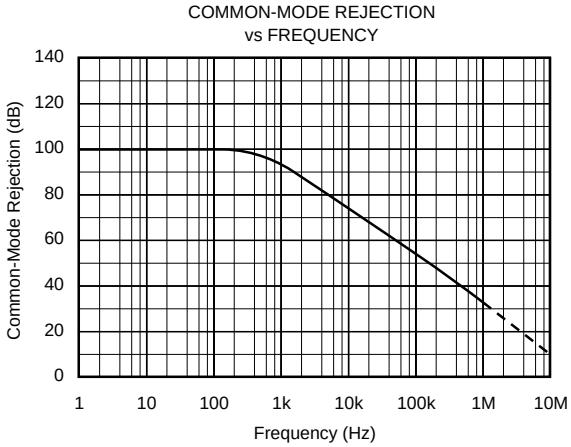
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15VDC unless otherwise noted.









APPLICATIONS INFORMATION

Unity-gain stability with good phase margin and excellent output drive characteristics bring freedom from the subtle problems associated with other high speed amplifiers. But with any high speed, wide bandwidth circuitry, careful circuit layout will ensure best performance. Make short, direct interconnections and avoid stray wiring capacitance—especially at the inverting input pin.

Power supplies should be bypassed with good high frequency capacitors positioned close to the op amp pins. In most cases 0.1µF ceramic capacitors are adequate. Applications with heavier loads and fast transient waveforms may benefit from use of additional 1.0µF tantalum bypass capacitors.

INPUT BIAS CURRENT GUARDING

Leakage currents across printed circuit boards can easily exceed the input bias current of the OPA602. A circuit board "guard" pattern (Figure 1) is an effective solution to difficult leakage problems. This guard pattern must be repeated on all layers of a multilayer board. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage currents will flow harmlessly to the low impedance node.

Input bias current may also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards may be cleaned with appropriate solvents and deionized water. Each rinsing operation should be followed by a 30-minute bake at +85°C.

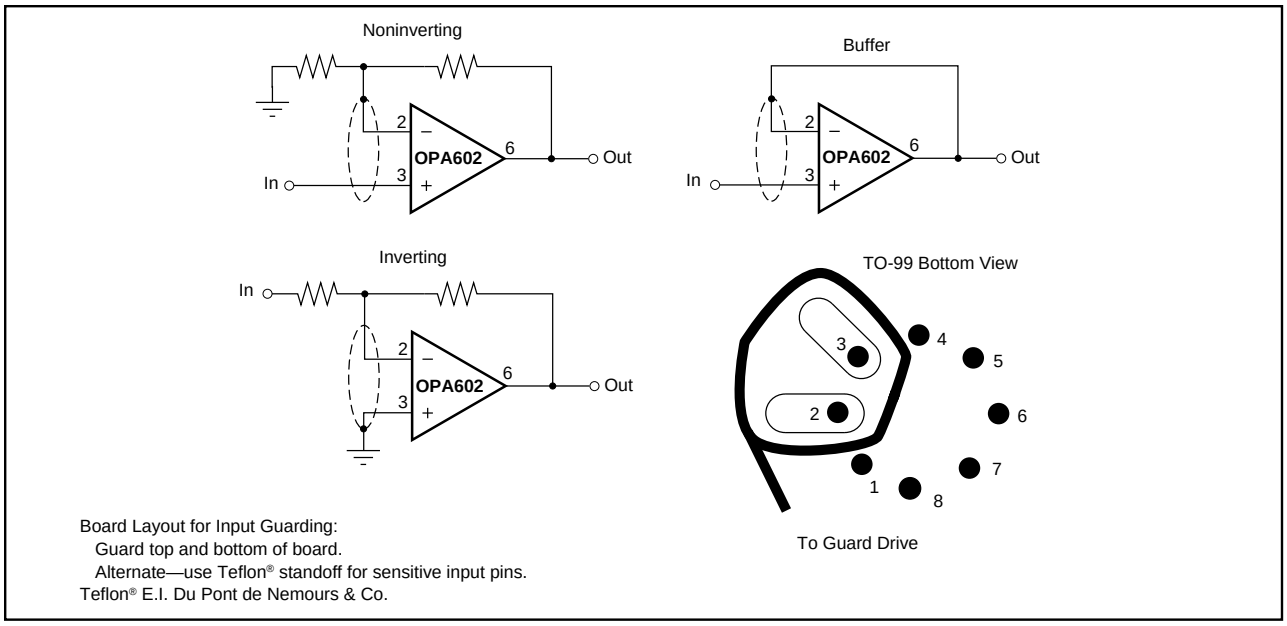


FIGURE 1. Connection of Input Guard.

APPLICATION CIRCUITS

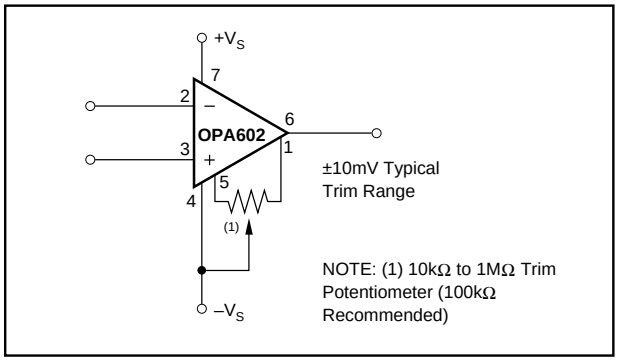


FIGURE 2. Offset Voltage Trim.

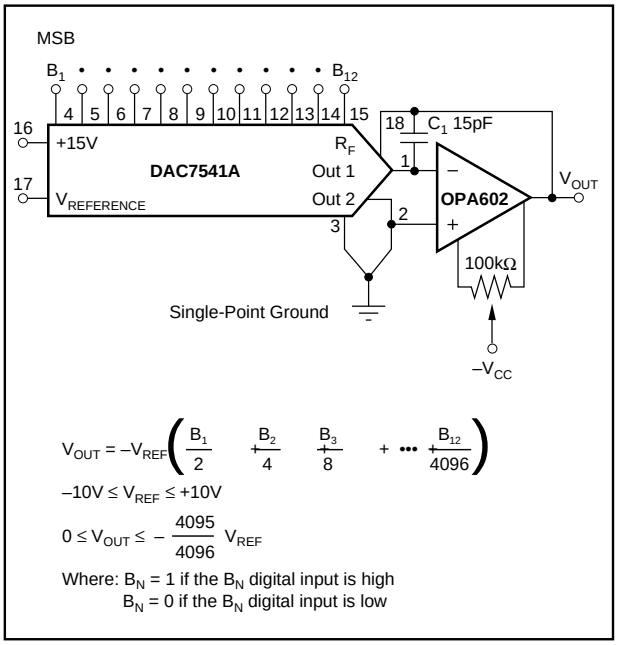


FIGURE 3. Voltage Output D/A Converter.

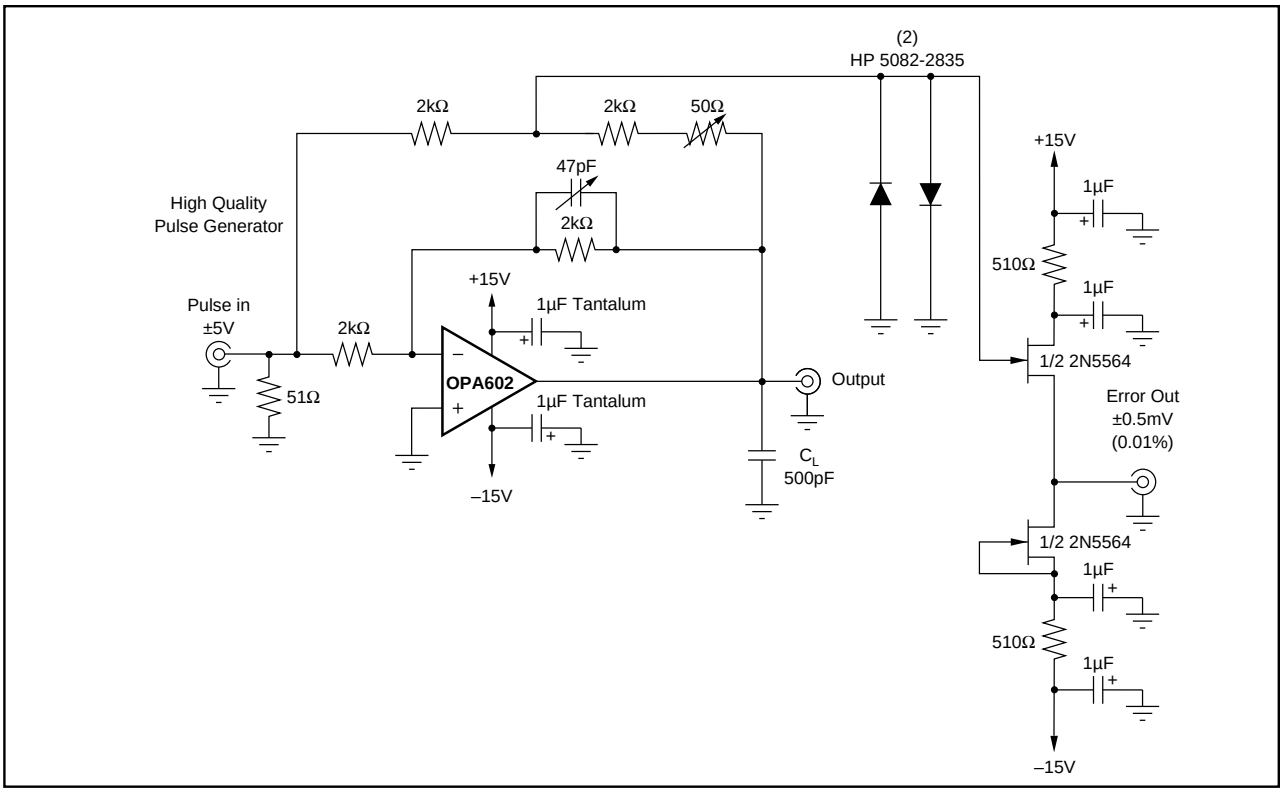
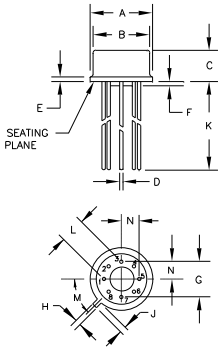


FIGURE 4. Settling Time and Slew Rate Test Circuit.

PACKAGE DRAWINGS

Package Number 001 - Metal TO-99



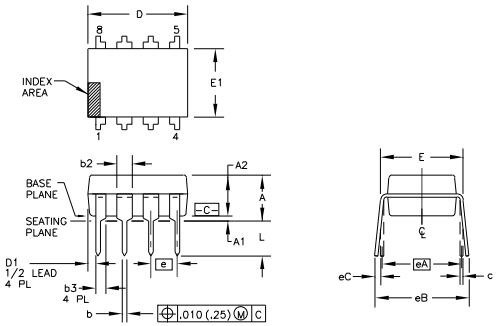
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.335	.380	8.51	9.65	
B	.305	.335	7.75	8.51	
C	.165	.185	4.19	4.70	
D	.016	.021	0.41	0.53	
E	.010	.040	0.25	1.02	
F	.010	.040	0.25	1.02	
G	.200	BASIC	5.08	BASIC	
H	.028	.034	0.71	0.86	
J	.029	.045	0.74	1.14	
K	.500	--	12.7	--	
L	.110	.160	2.79	4.06	
M	45°	BASIC	45°	BASIC	
N	.095	.105	2.41	2.67	

NOTES:

1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ001 REV.: B
JEDEC NUMBER: UNKNOWN

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



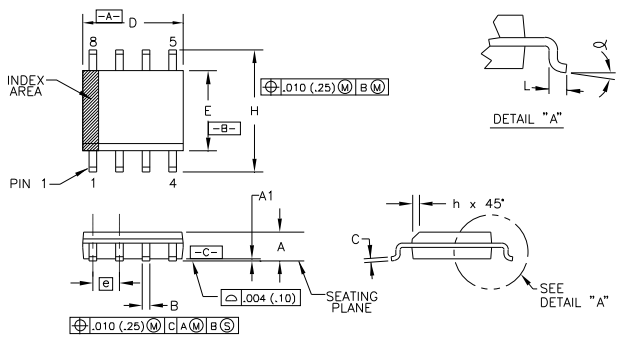
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.63	BASIC	5
eB	--	.430	--	10.92	6
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:

1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 REV.: E
JEDEC NUMBER: MS-001-BA

Package Number 182 - 8-Lead SOIC



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050	BASIC	1.27	BASIC	
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	
L	.016	.050	0.41	1.27	5
N	8		8		6
α	0°	8°	0°	8°	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 REV.: G
JEDEC NUMBER: MS-012-AA