

OPA404

Quad High-Speed Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- WIDE BANDWIDTH: 6.4MHz
- HIGH SLEW RATE: 35V/ μ s
- LOW OFFSET: $\pm 750\mu$ V max
- LOW BIAS CURRENT: ± 4 pA max
- LOW SETTLING: 1.5 μ s to 0.01%
- STANDARD QUAD PINOUT

APPLICATIONS

- PRECISION INSTRUMENTATION
- OPTOELECTRONICS
- SONAR, ULTRASOUND
- PROFESSIONAL AUDIO EQUIPMENT
- MEDICAL EQUIPMENT
- DETECTOR ARRAYS

DESCRIPTION

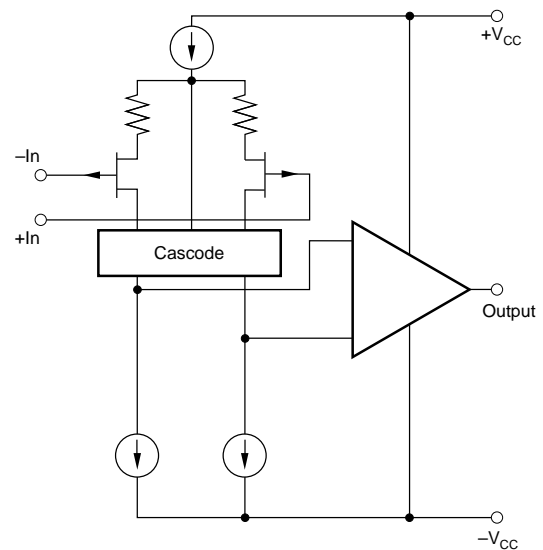
The OPA404 is a high performance monolithic *Difet*[®] (dielectrically-isolated FET) quad operational amplifier. It offers an unusual combination of very-low bias current together with wide bandwidth and fast slew rate.

Noise, bias current, voltage offset, drift, and speed are superior to BIFET[®] amplifiers.

Laser-trimming of thin-film resistors gives very low offset and drift—the best available in a quad FET op amp.

The OPA404's input cascode design allows high precision input specifications and uncompromised high-speed performance.

Standard quad op amp pin configuration allows upgrading of existing designs to higher performance levels. The OPA404 is unity-gain stable.



OPA404 Simplified Circuit
(Each Amplifier)

Difet[®], Burr-Brown Corp.
BIFET[®], National Semiconductor Corp.

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU ⁽¹⁾			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE Voltage: $f_o = 10\text{Hz}$ $f_o = 100\text{Hz}$ $f_o = 1\text{kHz}$ $f_o = 10\text{kHz}$ $f_B = 10\text{Hz to } 10\text{kHz}$ $f_B = 0.1\text{Hz to } 10\text{Hz}$ Current: $f_B = 0.1\text{Hz to } 10\text{Hz}$ $f_o = 0.1\text{Hz thru } 20\text{kHz}$			32			*			*		$\text{nV}/\sqrt{\text{Hz}}$
				19			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				15			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				12			*		*		$\text{nV}/\sqrt{\text{Hz}}$
				1.4			*		*		μVrms
				0.95			*		*		$\mu\text{Vp-p}$
				12			*		*		fA, p-p
			0.6			*		*		$\text{fA}/\sqrt{\text{Hz}}$	
OFFSET VOLTAGE Input Offset Voltage KP, KU Average Drift KP, KU Supply Rejection KP, KU Channel Separation	$V_{CM} = 0\text{VDC}$		± 260 ± 750	$\pm 1\text{mV}$ $\pm 2.5\text{mV}$		*	± 750		*	*	μV μV
	$T_A = T_{MIN}$ to T_{MAX}		± 3 ± 5			*			*		$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
	$\pm V_{CC} = 12\text{V to } 18\text{V}$	80 76	100 100		86	*		*	*		dB dB
	$100\text{Hz, } R_L = 2\text{k}\Omega$		125			*			*		dB
BIAS CURRENT Input Bias Current KP, KU	$V_{CM} = 0\text{VDC}$		± 1 ± 1	± 8 ± 12		*	± 4		*	*	pA pA
OFFSET CURRENT Input Offset Current KP, KU	$V_{CM} = 0\text{VDC}$		0.5 0.5	8 12		*	4		*	*	pA pA
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{14} \parallel 3$			*			*		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
VOTAGE RANGE Common-Mode Input Range Common-Mode Rejection KP, KU	$V_{IN} = \pm 10\text{VDC}$	± 10.5 88 84	$+13, -11$ 100 100		*	*		*	*		V dB dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	88	100		92	*		*	*		dB
FREQUENCY RESPONSE Gain Bandwidth Full Power Response Slew Rate Settling Time: 0.1% 0.01%	Gain = 100 $20\text{Vp-p, } R_L = 2\text{k}\Omega$	4	6.4 570		5	*		*	*		MHz kHz
	$V_O = \pm 10\text{V, } R_L = 2\text{k}\Omega$	24	35		28	*		*	*		$\text{V}/\mu\text{s}$
	Gain = -1, $R_L = 2\text{k}\Omega$		0.6			*		*	*		μs
	$C_L = 100\text{ pF, } 10\text{V Step}$		1.5			*		*	*		μs
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ 1MHz, Open Loop Gain = +1	± 11.5 ± 5	$+13.2, -13.8$ ± 10 80 1000		*	*		*	*		V mA Ω pF mA
				± 40	*	*	*	*	*	*	
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent			± 15		*	*		*	*		VDC
		± 5		± 18 10	*	*	*	*	*	*	VDC mA
	$I_O = 0\text{mADC}$		9								
TEMPERATURE RANGE Specification KP, KU Operating KP, KU Storage KP, KU θ Junction-Ambient KP, KU	Ambient Temperature	-25 0		+85 +70	*	*		-55		+125	$^\circ\text{C}$ $^\circ\text{C}$
	Ambient Temperature	-55 -25		+125 +85	*	*	*	*	*	*	$^\circ\text{C}$ $^\circ\text{C}$
	Ambient Temperature	-65 -40		+150 +125	*	*	*	*	*	*	$^\circ\text{C}$ $^\circ\text{C}$
			100			*	*	*	*	*	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$
			120/100								

*Specifications same as OPA404AG.

NOTE: (1) OPA404KU may be marked OPA404U.

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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA404AG, KP, KU			OPA404BG			OPA404SG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification Range KP, KU	Ambient Temperature	-25 0		+85 +70	*		*	-55		+125	°C °C
INPUT OFFSET VOLTAGE Input Offset Voltage KP KU Average Drift KP, KU Supply Rejection	$V_{CM} = 0\text{VDC}$		± 450 ± 1 ± 3 ± 5 96	2mV ± 3.5		*	$\pm 1.5\text{mV}$		± 550 *	$\pm 2.5\text{mV}$	μV mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$ dB
BIAS CURRENT Input Bias Current	$V_{CM} = 0\text{VDC}$		± 32	± 200		*	± 100		± 500	$\pm 5\text{nA}$	pA
OFFSET CURRENT Input Offset Current	$V_{CM} = 0\text{VDC}$		17	100		*	50		260	2.5nA	pA
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection KP, KU	$V_{IN} = \pm 10\text{VDC}$	± 10 82 80	$\pm 12.7, -10.6$ 99 99		*	*		± 10 80	$+12.6, -10.5$ 88		V dB dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	82	94		86	*		80	88		dB
RATED OUTPUT Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	± 11.5 ± 5 ± 8	$\pm 12.9, -13.8$ ± 9 ± 20	± 50	*	*	*	± 11 *	$+12.7, -13.8$ ± 8 *		V mA mA
POWER SUPPLY Current, Quiescent	$I_O = 0\text{mADC}$		9.3	10.5		*	*		9.4	11	mA

* Specification same as OPA404AG.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA404KP	14-Pin Plastic DIP	0°C to +70°C
OPA404KU ⁽¹⁾	16-Pin Plastic SOIC	0°C to +70°C
OPA404AG	14-Pin Ceramic DIP	-25°C to +85°C
OPA404BG	14-Pin Ceramic DIP	-25°C to +85°C
OPA404SG	14-Pin Ceramic DIP	-55°C to +125°C

NOTE: (1) OPA404KU may be marked OPA404U.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA404KP	14-Pin Plastic DIP	010
OPA404KU ⁽²⁾	16-Pin Plastic SOIC	211
OPA404AG	14-Pin Ceramic DIP	169
OPA404BG	14-Pin Ceramic DIP	169
OPA404SG	14-Pin Ceramic DIP	169

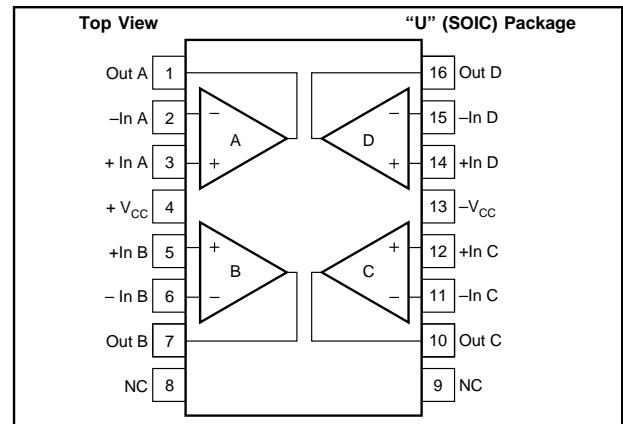
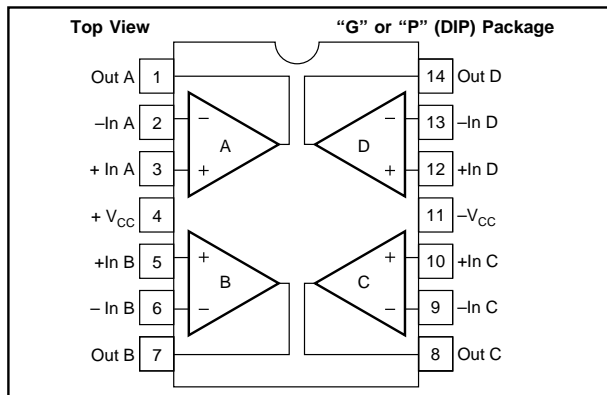
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book. (2) OPA404KU may be marked OPA404U.

ABSOLUTE MAXIMUM RATINGS

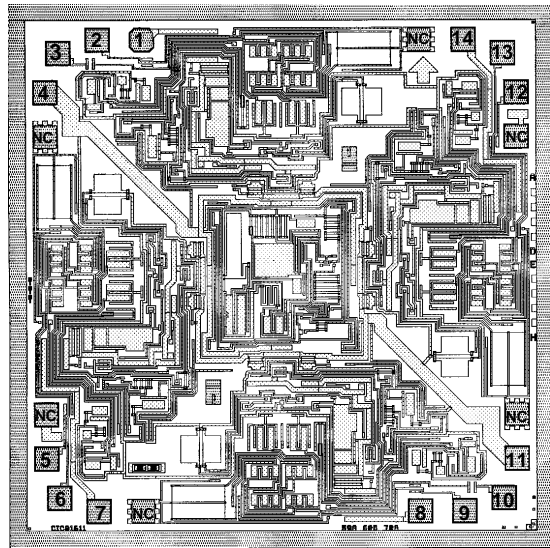
Supply	$\pm 18\text{VDC}$	Operating Temperature Range .. P, U = -25°C/+85°C, G = -55°C/+125°C	
Internal Power Dissipation ⁽¹⁾	1000mW	Lead Temperature (soldering, 10s)	300°C
Differential Input Voltage ⁽²⁾	$\pm 36\text{VDC}$	SOIC (soldering, 3s)	+260°C
Input Voltage Range ⁽²⁾	$\pm 18\text{VDC}$	Output Short-Circuit Duration ⁽³⁾	Continuous
Storage Temperature Range ... P, U = -40°C/+125°C, G = -65°C/+150°C		Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on $\theta_{JC} = 30^\circ\text{C/W}$ or $\theta_{JA} = 120^\circ\text{C/W}$. (2) For supply voltages less than $\pm 18\text{VDC}$ the absolute maximum input voltage is equal to: $18\text{V} > V_{IN} > -V_{CC} - 8\text{V}$. See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J .

PIN CONFIGURATION



DICE INFORMATION



OPA404 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Output A	8	Output C
2	-Input A	9	-Input C
3	+Input A	10	+Input C
4	+V _{CC}	11	-V _{CC}
5	+Input B	12	+Input D
6	-Input B	13	-Input D
7	Output B	14	Output D

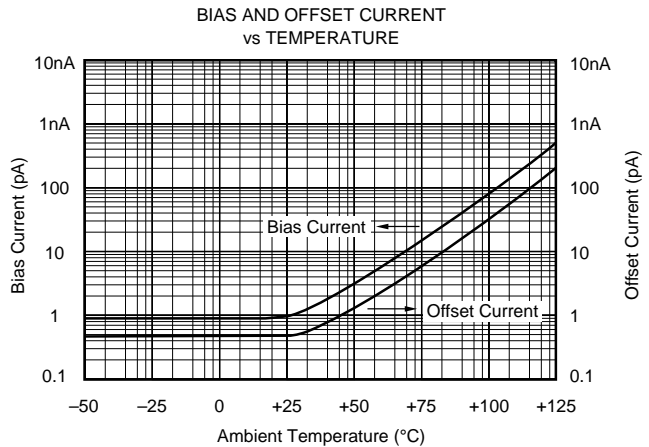
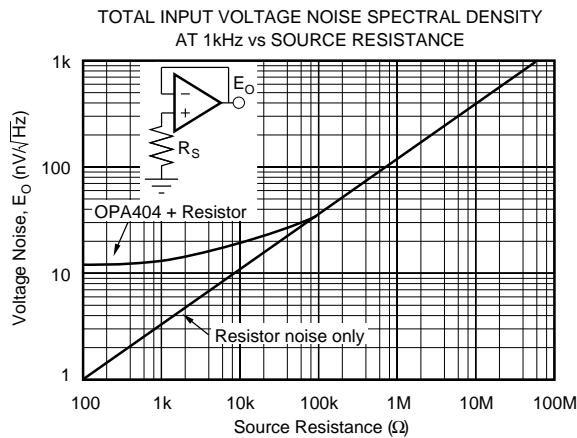
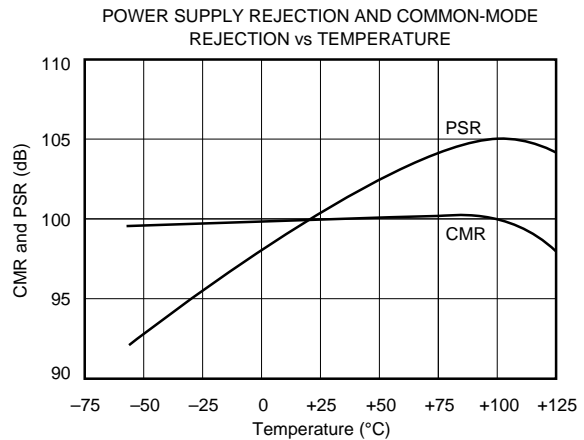
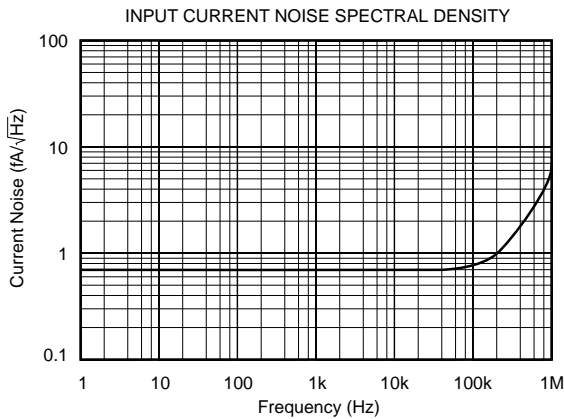
Substrate Bias: -V_{CC}
 NC: No connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	108 x 108 ±5	2.74 x 2.74 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	None	

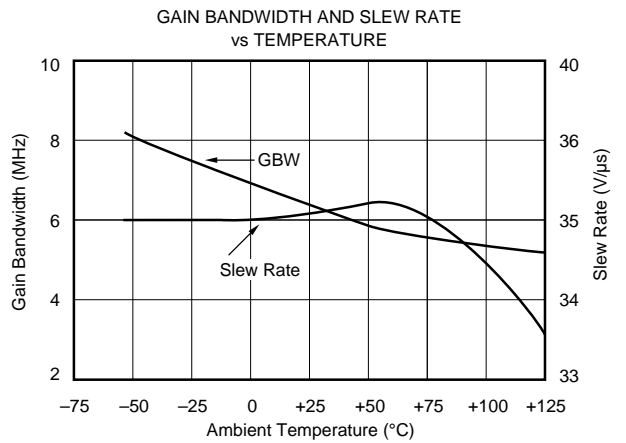
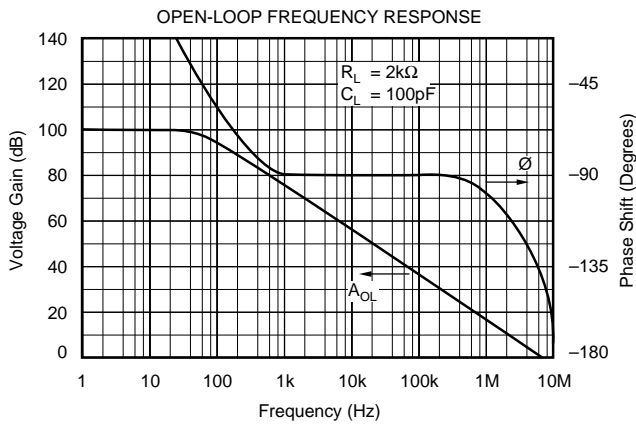
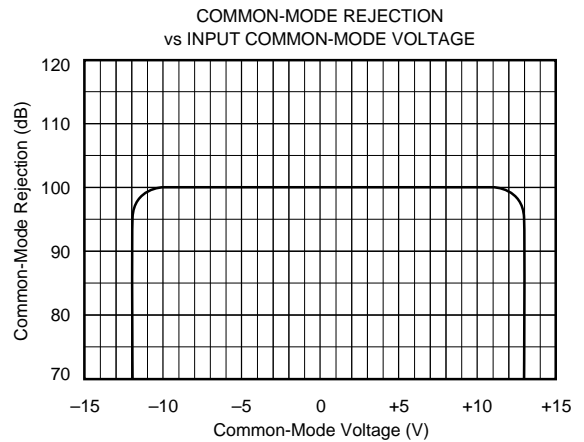
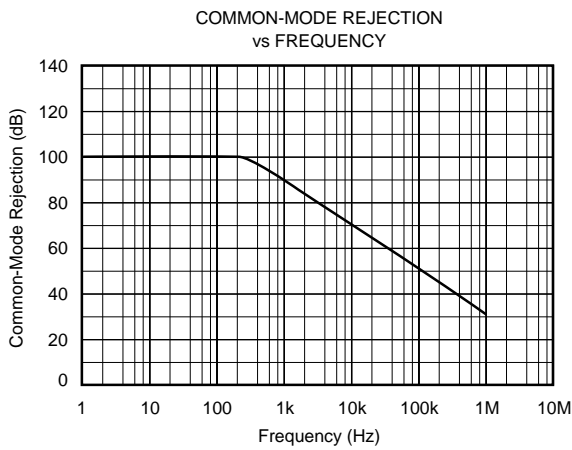
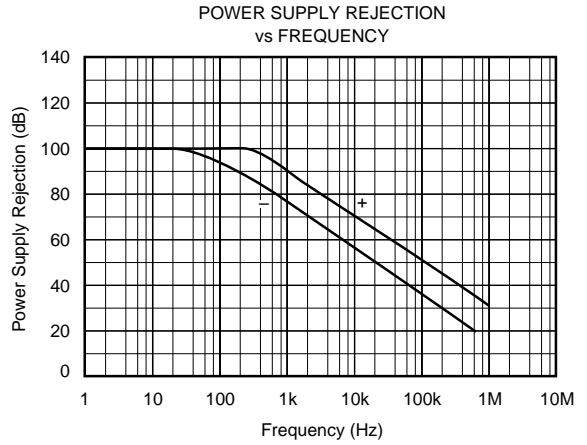
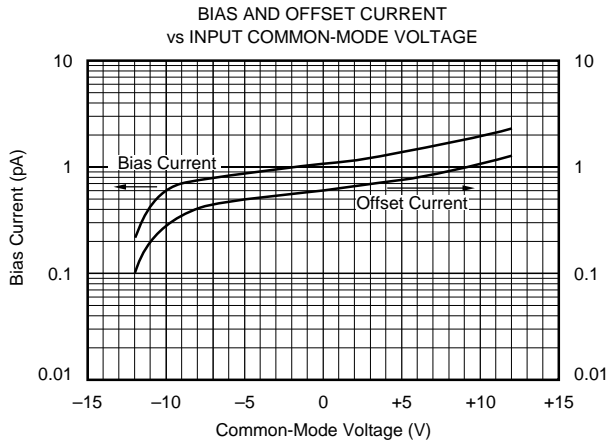
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = ±15VDC unless otherwise noted.



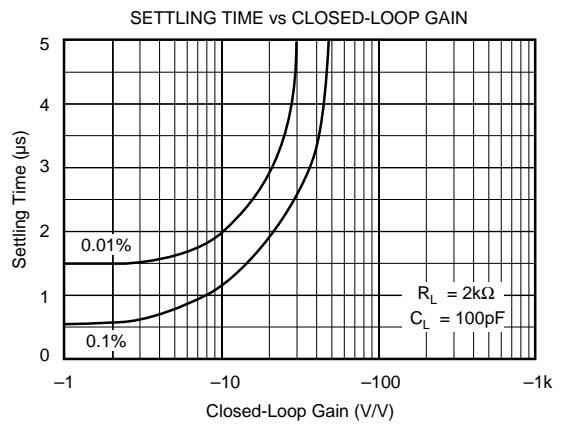
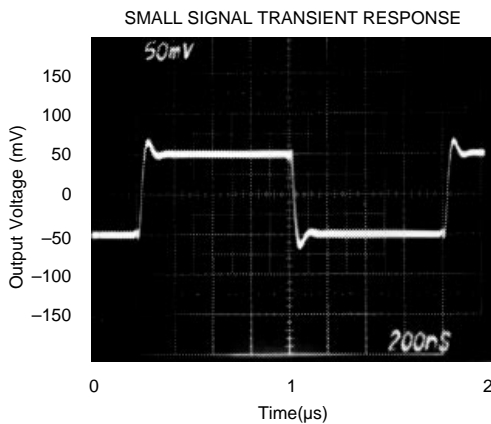
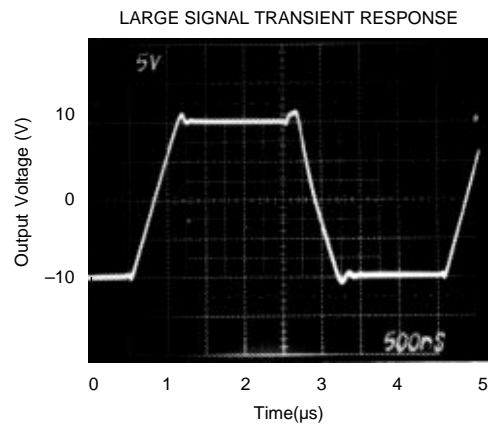
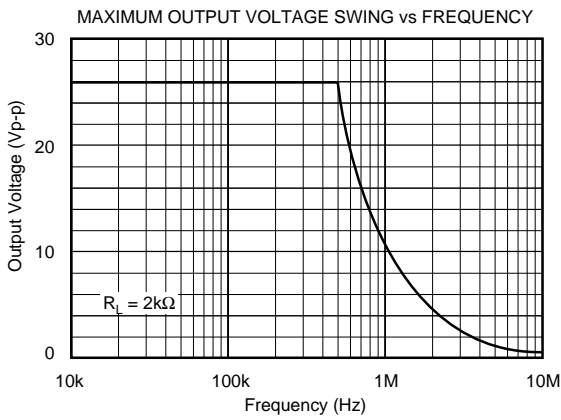
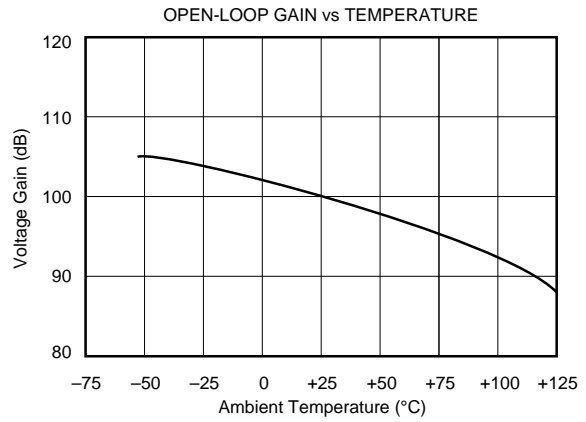
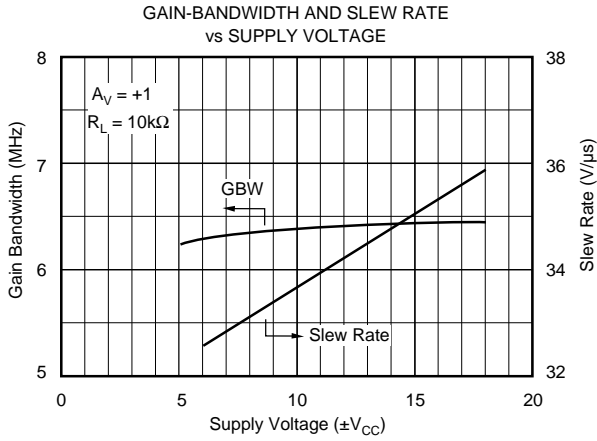
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



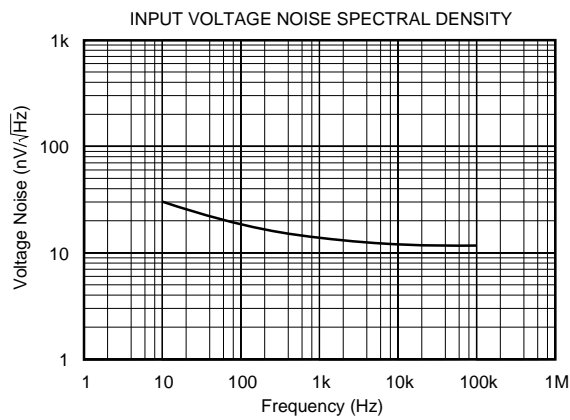
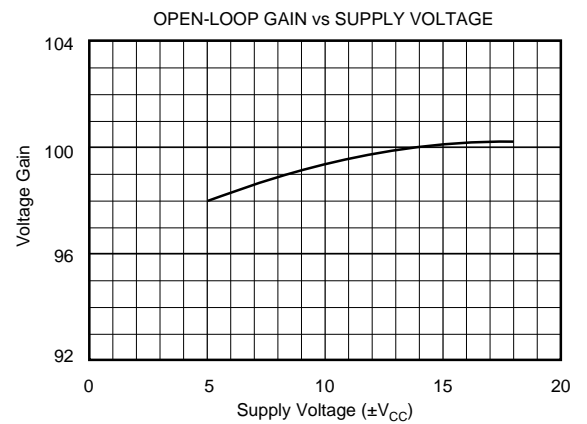
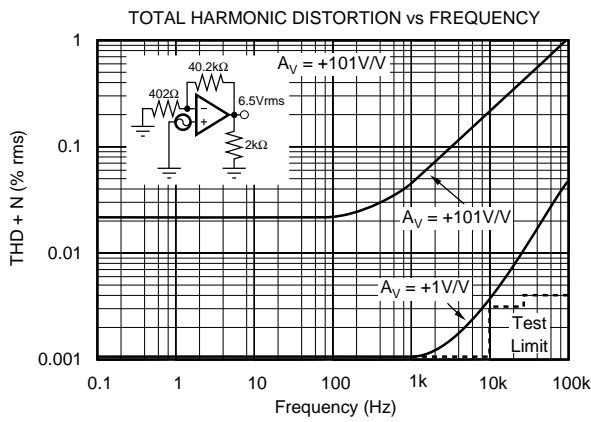
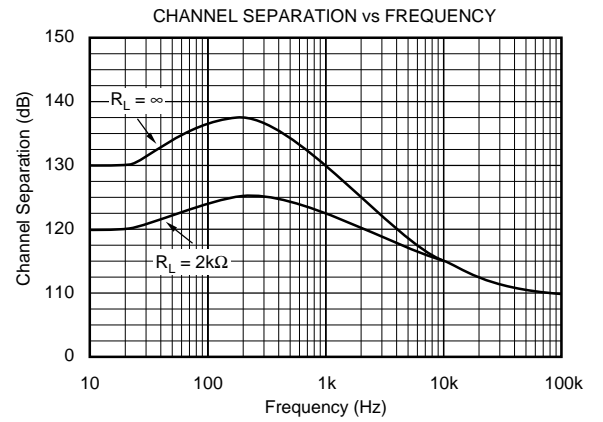
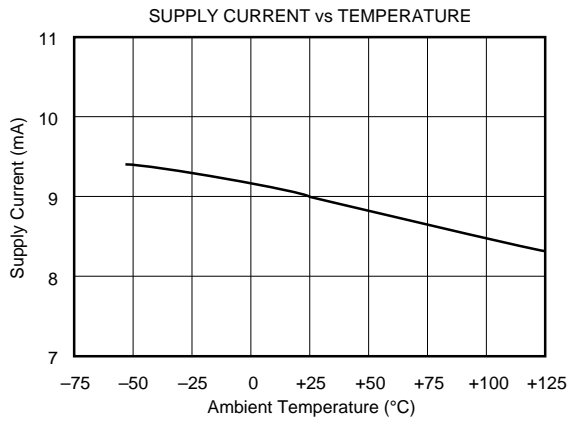
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA404 offset voltage is laser-trimmed and will require no further trim for most applications. If desired, offset voltage can be trimmed by summing (see Figure 1). With this trim method there will be no degradation of input offset drift.

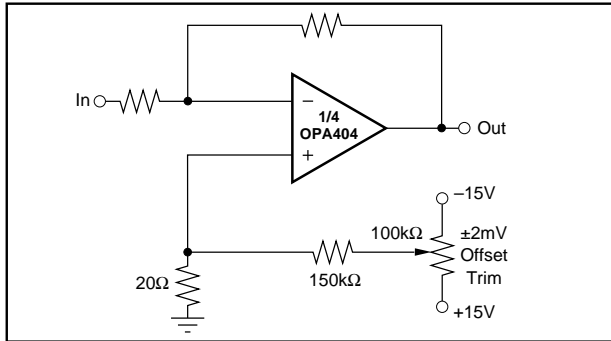


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the *Difet* OPA404 requires input current limiting resistors only if its input voltage is greater than 8 volts more negative than $-V_{CC}$. A $10k\Omega$ series resistor will limit the input current to a safe value with up to $\pm 15V$ input levels even if both supply voltages are lost. (See Figure 2 and Absolute Maximum Ratings).

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

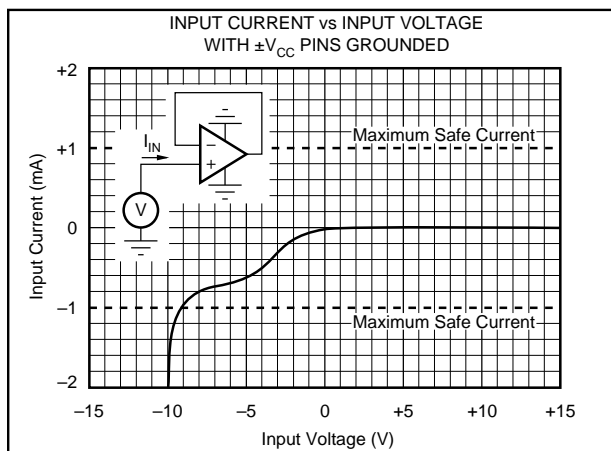


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA404. To avoid leakage, utmost care must be used in planning the board layout. A “guard” pattern should completely surround the high impedance input leads and should be connected to a low-impedance point which is at the signal input potential. (See Figure 3).

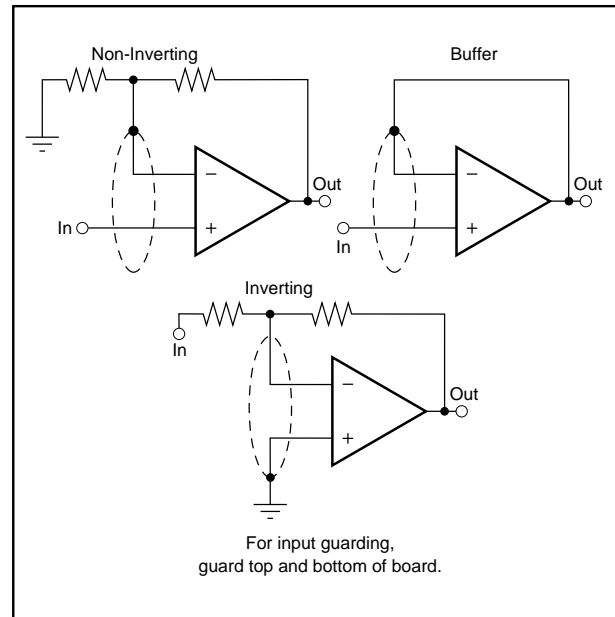


FIGURE 3. Connection of Input Guard.

HANDLING AND TESTING

Measuring the unusually low bias current of the OPA404 is difficult without specialized test equipment; most commercial benchtop testers cannot accurately measure the OPA404 bias current. Low-leakage test sockets and special test fixtures are recommended if incoming inspection of bias current is to be performed.

To prevent surface leakage between pins, the DIP package should not be handled by bare fingers. Oils and salts from fingerprints or careless handling can create leakage currents that exceed the specified OPA404 bias currents.

If necessary, DIP packages and PC board assemblies can be cleaned with Freon TF®, baked for 30 minutes at 85°C, rinsed with de-ionized water, and baked again for 30 minutes at 85°C. Surface contamination can be prevented by the application of a high-quality conformal coating to the cleaned PC board assembly.

BIAS CURRENT CHANGE vs COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 4). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely low bias current of the OPA404 is not compromised by common-mode voltage.

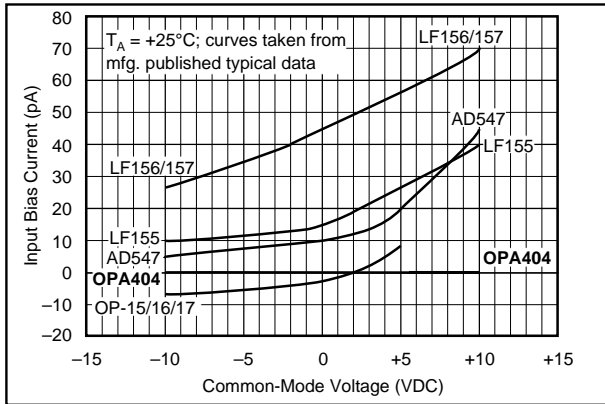


FIGURE 4. Input Bias Current vs Common-Mode Voltage.

APPLICATIONS CIRCUITS

Figures 5 through 11 are circuit diagrams of various applications for the OPA404.

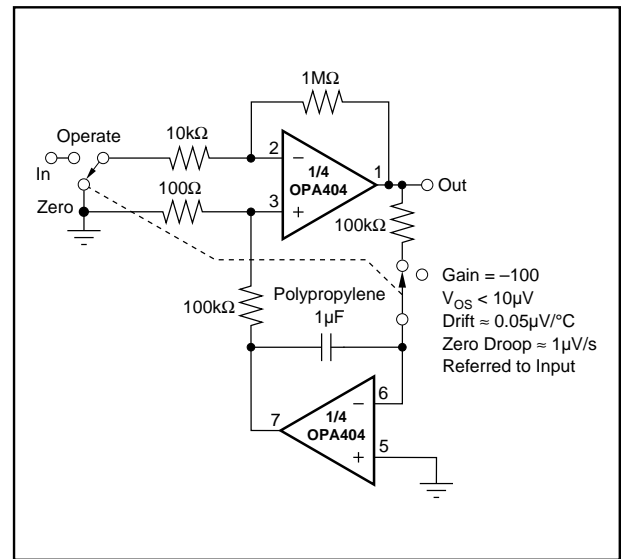


FIGURE 5. Auto-Zero Amplifier.

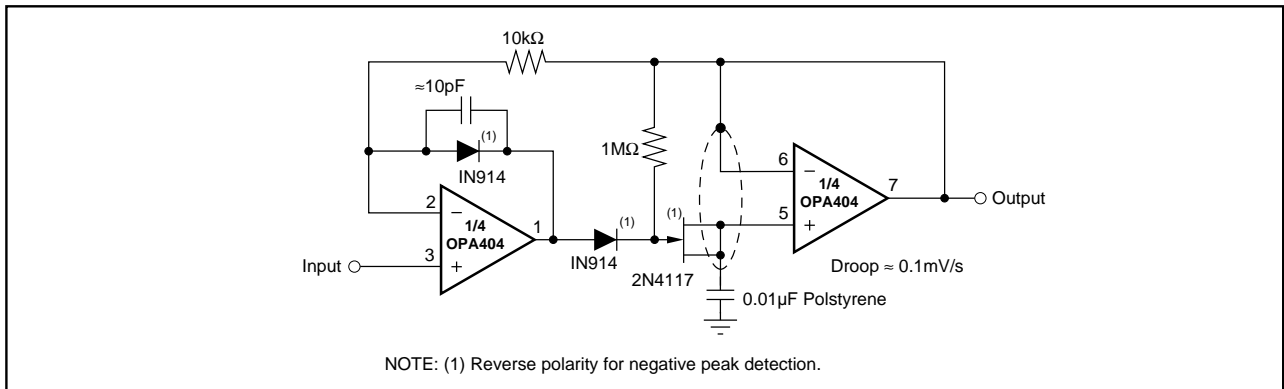


FIGURE 6. Low-Droop Positive Peak Detector.

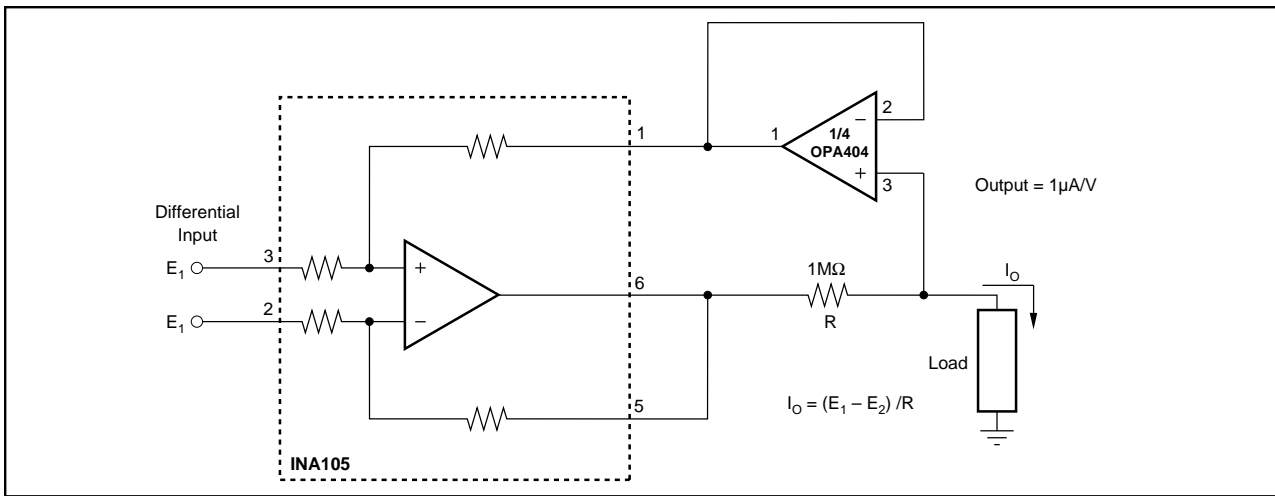


FIGURE 7. Voltage-Controlled Microamp Current Source.

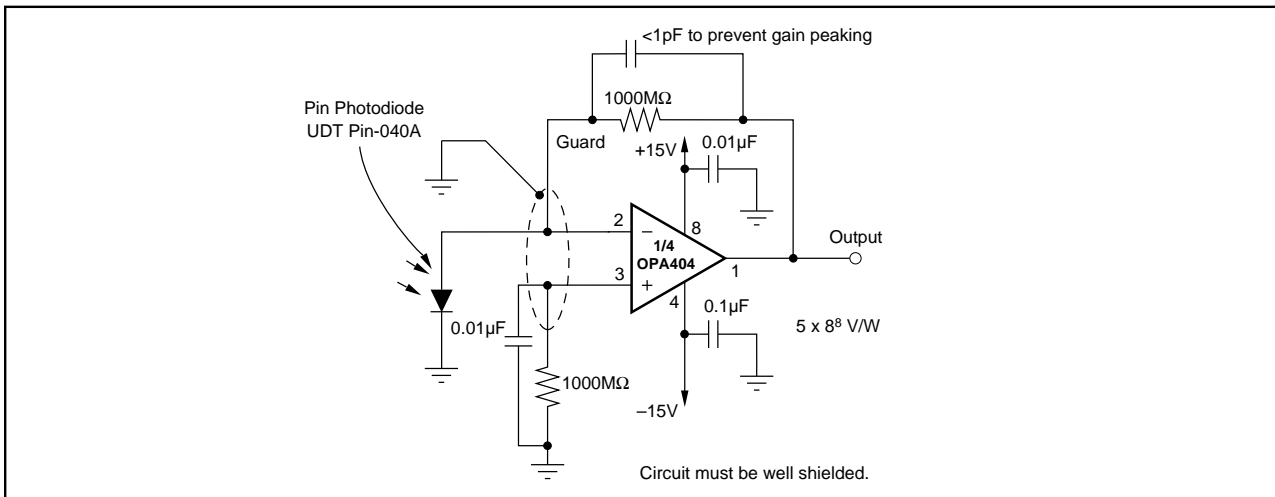


FIGURE 8. Sensitive Photodiode Amplifier.

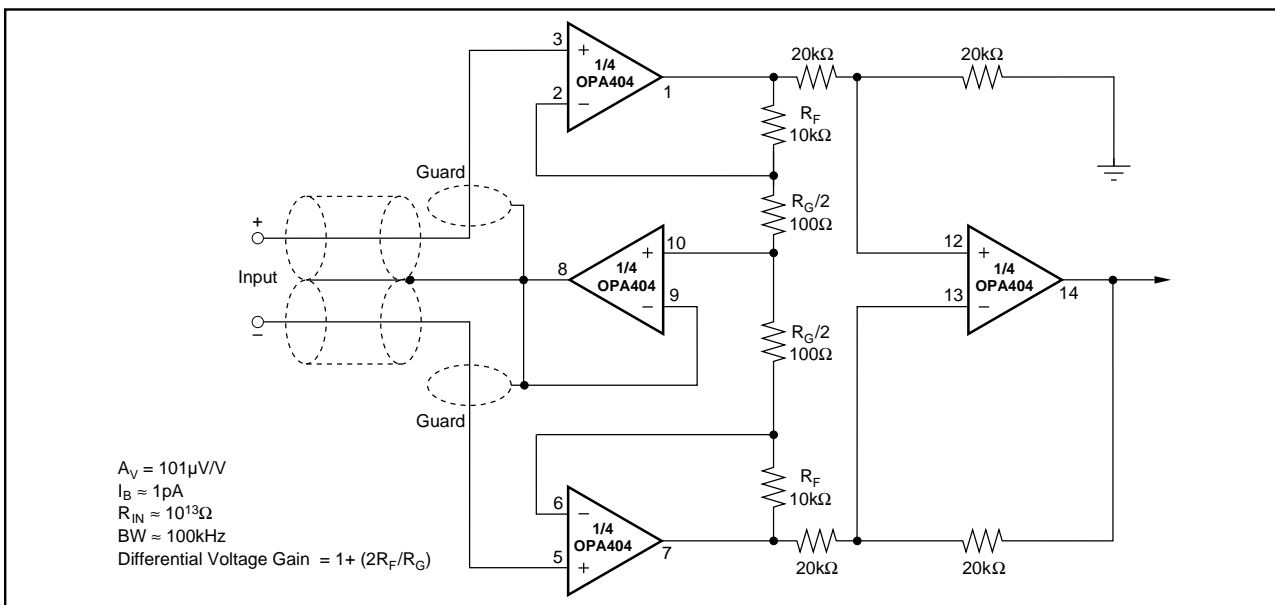


FIGURE 9. FET Instrumentation Amplifier with Shield Driver.

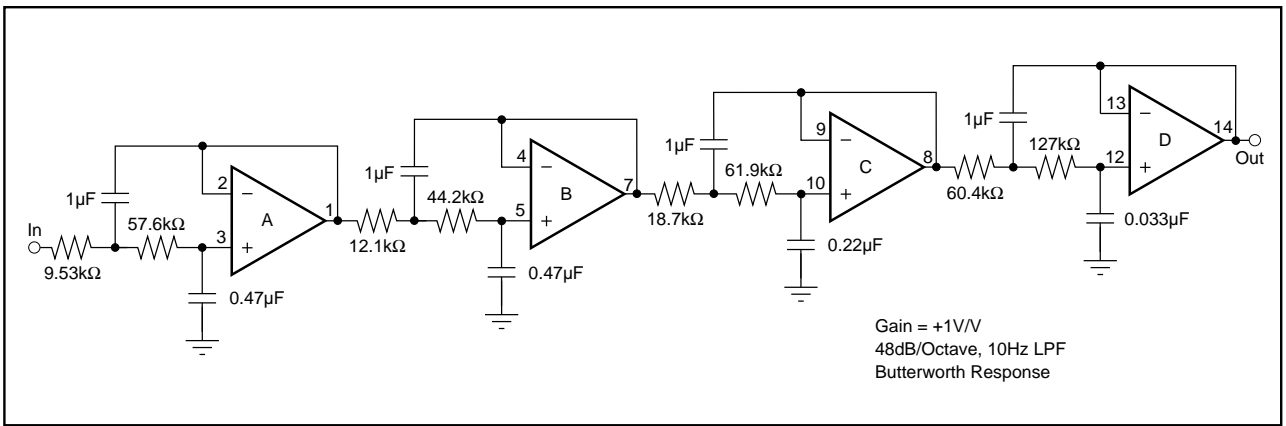


FIGURE 10. 8-Pole 10Hz Low-Pass Filter.

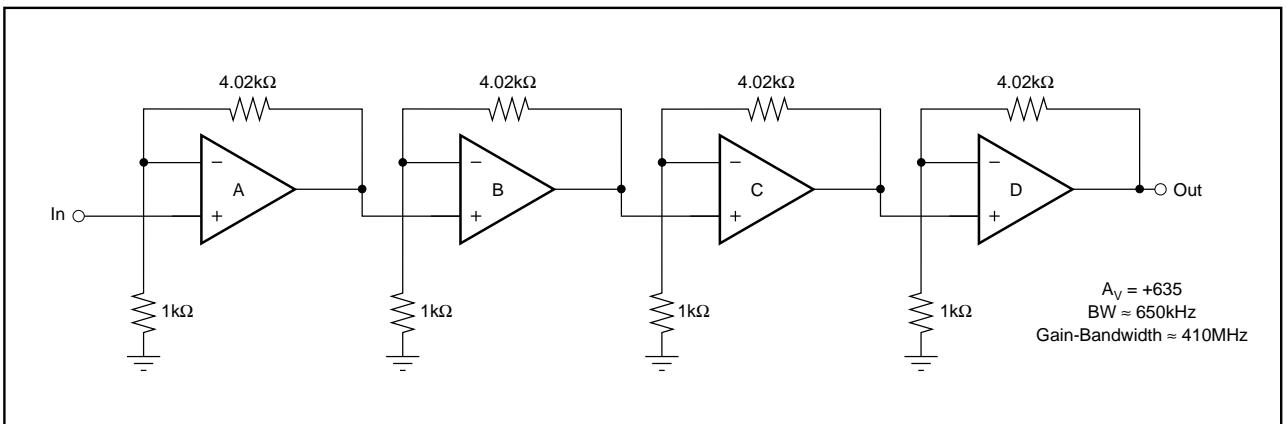
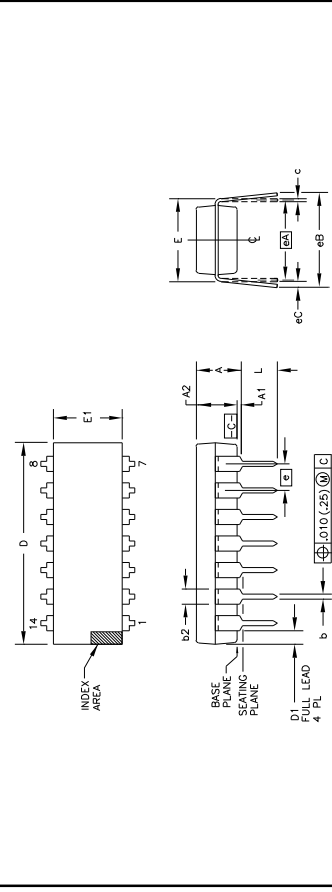


FIGURE 11. Wide-Band Amplifier.

PACKAGE DRAWINGS

Package Number 010 - 14-Pin Plastic, Single-Wide DIP



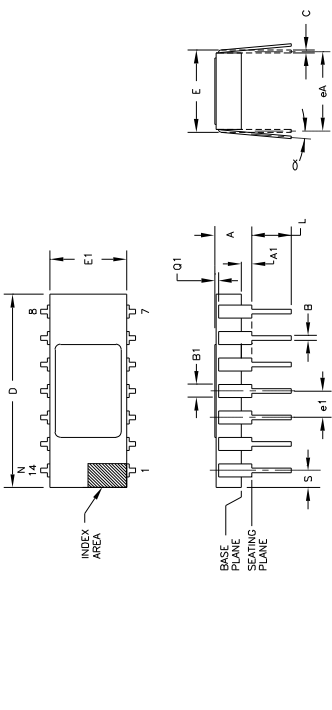
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.115	.195	2.92	4.95
A1	.015	.022	0.38	0.56
B	.045	.070	1.14	1.78
B2	.008	.014	0.20	0.36
C	.039	.075	1.00	1.91
D	.735	.775	18.67	19.69
E1	.005	.013	0.13	0.33
E	.240	.280	6.10	7.14
L	.240	.280	6.10	7.14
N	.050 BASIC	0.050	1.27 BASIC	1.27
eA	.300 BASIC	0.300	7.62 BASIC	7.62
eB	.450	.600	11.43	15.24
eC	.000	.060	0.00	1.52

NOTES:

- ALL DIMENSIONS ARE IN INCHES.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1987, AND L ARE IN JEDEC SEATING PLANE GAUGE GS-3.
- MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
- INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
- CONSTRAINED TO BE PERPENDICULAR TO DATUM [C].
- LEAD TIPS WITH THE LEADS UNCONSTRAINED.
- N IS THE MAXIMUM OF TERMINAL POSITIONS.

PACKAGE NUMBER: Z210 REV: G
JEDEC NUMBER: MS-001-AA

Package Number 100 - 14-Lead, Ceramic Side Braze DIP, .300 Wide



DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.105	.175	2.67	4.45
A1	.025	.055	0.64	1.40
B	.015	.021	0.38	0.53
B1	.038	.060	0.97	1.52
C	.008	.012	0.20	0.30
D	.690	.770	17.53	19.56
E	.290	.325	7.37	8.28
E1	.280	.310	7.11	7.87
L	.300 DIP	.362 DIP	7.62	9.18
N	.125	.175	3.18	4.45
L	.14	---	3.54	---
S	.010	---	0.25	---
S1	.030	.095	0.76	2.41

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1987.
- EDGES WITHIN .008 IN. (0.13mm) AT GAUGE PLANE WITH MAXIMUM MATERIAL CONDITION AND UNIT INSTALLED.
- APPLIES TO SPREAD LEADS PRIOR TO INSTALLATION.
- INDICATES THE NUMBER OF TERMINAL POSITIONS.

5. OUTLINES ON WHICH THE SEATING PLANE IS COINCIDENT WITH THE LEAD STANDOFFS ARE NOT REQUIRED, AND B1 MAY EQUAL B ALONG ANY PART OF THE LEAD ABOVE THE SEATING/BRAZE PLANE.

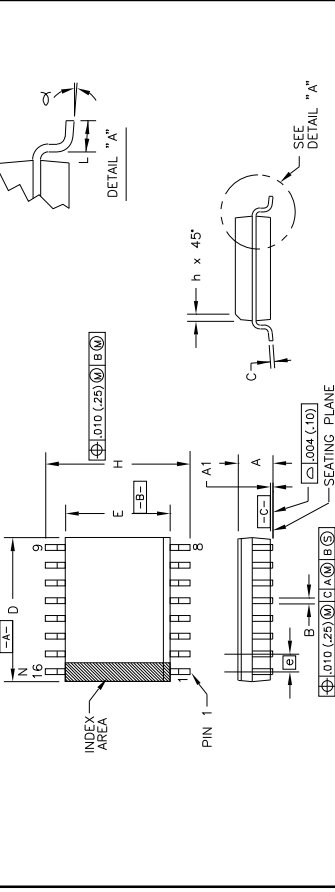
6. E1 DOES NOT INCLUDE PARTICLES OF PACKING MATERIALS.

7. CONTROLLING DIMENSION: INCH.

8. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

PACKAGE NUMBER: Z2169 REV: F
JEDEC NUMBER: MO-35-AB

Package Number 211 - 16-Lead SOIC



DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	.0926	.1043	2.35	2.65
A1	.004	.0118	0.10	0.30
B	.013	.020	0.33	0.51
C	.0391	.0725	1.00	1.83
D	.7314	.7592	18.58	19.28
E	.2914	.3292	7.40	8.30
E1	.2914	.3292	7.40	8.30
H	.394	.419	10.00	10.65
L	.010	.029	0.25	0.75
N	.016	.050	0.40	1.27
L	.016	.050	0.40	1.27
N	.16	---	4.13	---
α	0°	8°	0°	8°

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1987.
- DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
- DIMENSION "E" DOES NOT INCLUDE PROTRUSIONS AND GATE BURRS. PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .024 IN. (0.61 mm). LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.
- OPTIONAL: IF IT IS NOT PRESENT.

8. POINTED OR ROUNDED LEAD TIPS ARE REFERRED TO EASE INSERTION.

9. MAXIMUM DIMENSION DOES NOT EXCEED .010 (0.25mm).

10. DISTANCE BETWEEN LEADS INCLUDING .005 (0.127mm) MINIMUM.

11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE OF THE LEAD SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: Z210 REV: G
JEDEC NUMBER: MS-001-AA