BURR - BROWN®

OPA2107

Precision Dual *Difet* ® OPERATIONAL AMPLIFIER

FEATURES

- VERY LOW NOISE: 8nV/√Hz at 10kHz
- LOW V_{os}: 500μV max
- LOW DRIFT: 5μV/°C max
- LOW I_B: 5pA max
- FAST SETTLING TIME: 2μs to 0.01%
- UNITY-GAIN STABLE

APPLICATIONS

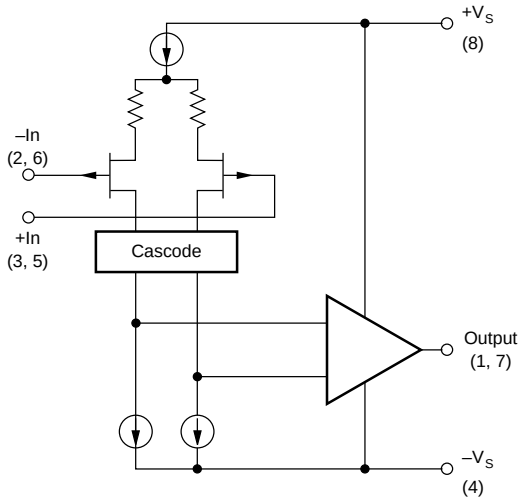
- DATA ACQUISITION
- DAC OUTPUT AMPLIFIER
- OPTOELECTRONICS
- HIGH-IMPEDANCE SENSOR AMPS
- HIGH-PERFORMANCE AUDIO CIRCUITRY
- MEDICAL EQUIPMENT, CT SCANNERS

DESCRIPTION

The OPA2107 dual operational amplifier provides precision ***Difet*** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (***Difet***) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent DC performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in plastic DIP, metal TO-99, and SOIC packages. Industrial and Military temperature range versions are available.



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BIFET® National Semiconductor

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SPECIFICATIONS

T_A = +25°C, V_S = ±15V unless otherwise noted.

PARAMETER	CONDITION	OPA2107AM, SM, AP, AU			OPA2107BM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE[1]								
Input Offset Voltage	V_{CM} = 0V		100	1mV		50	500	µV
Over Specified Temperature			0.5	2		0.2	1	mV
SM Grade			0.8	2.5				mV
Average Drift Over Specified Temperature			3	10		2	5	µV/°C
Power Supply Rejection	V_S = ±10 to ±18V	80	96		84	100		dB
INPUT BIAS CURRENT[1]								
Input Bias Current	V_{CM} = 0V		4	10		2	5	pA
Over Specified Temperature			0.25	1.5		0.15	1	nA
SM Grade			4	35				nA
Input Offset Current	V_{CM} = 0V		1	8		0.5	3	pA
Over Specified Temperature				1			0.5	nA
SM Grade			1	28				nA
INPUT NOISE								
Voltage: f = 10Hz	R_S = 0		30			*		nV/√Hz
f = 100Hz			12			*		nV/√Hz
f = 1kHz			9			*		nV/√Hz
f = 10kHz			8			*		nV/√Hz
BW = 0.1 to 10Hz			1.2			*		µVp-p
BW = 10 to 10kHz			0.85			*		µVrms
Current: f = 0.1Hz thru 20kHz			1.2			0.9		fA/√Hz
BW = 0.1Hz to 10Hz			23			17		fAp-p
INPUT IMPEDANCE								
Differential			10^{13} || 2			*		Ω || pF
Common-Mode			10^{14} || 4			*		Ω || pF
INPUT VOLTAGE RANGE								
Common-Mode Input Range		±10.5	±11		*	*		V
Over Specified Temperature		±10.2	±10.5		*	*		V
SM Grade		±10	±10.3					V
Common-Mode Rejection	V_{CM} = ±10V	80	94		84	100		dB
OPEN-LOOP GAIN								
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	82	96		84	100		dB
Over Specified Temperature		80	94		82	96		dB
SM Grade		80	92					dB
DYNAMIC RESPONSE								
Slew Rate	G = +1	13	18		*	*		V/µs
Settling Time: 0.1%	G = –1, 10V Step		1.5			*		µs
0.01%			2			*		µs
Gain-Bandwidth Product	G = 100		4.5			*		MHz
THD + Noise	G = +1, f = 1kHz		0.001			*		%
Channel Separation	f = 100Hz, R_L = 2kΩ		120			*		dB
POWER SUPPLY								
Specified Operating Voltage			±15			*		V
Operating Voltage Range		±4.5		±18	*		*	V
Current			±4.5	±5		*	*	mA
OUTPUT								
Voltage Output	R_L = 2kΩ	±11	±12		*	*		V
Over Specified Temperature		±10.5	±11.5		*	*		V
SM Grade		±10.2	±11.3					V
Short Circuit Current		±10	±40		*	*		mA
Output Resistance, Open-Loop	1MHz		70			*		Ω
Capacitive Load Stability	G = +1		1000			*		pF
TEMPERATURE RANGE								
Specification								
AP, AU, AM, BM		–25		+85	*		*	°C
SM		–55		+125				°C
Operating								
AP, AU		–25		+85				°C
AM, BM, SM		–55		+125	*		*	°C
Storage								
AP, AU		–40		+125				°C
AM, BM, SM		–65		+150	*		*	°C
Thermal Resistance (θ_{J-A})								
AP			90					°C/W
AU			175					°C/W
AM, BM, SM			200			*		°C/W

* Specifications same as OPA2107AM. NOTE: (1) Specified with devices fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$ ±2V
Differential Input Voltage	Total V_S ±4V
Operating Temperature	
M Package	–55°C to +125°C
P and U Packages	–25°C to + 85°C
Storage Temperature	
M Package	–65°C to +150°C
P and U Packages	–40°C to +125°C
Output Short Circuit to Ground (T_A = +25°C)	Continuous
Junction Temperature	+175°C
Lead Temperature	
M and P Packages (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C

PACKAGE INFORMATION

MODELS	PACKAGE	PACKAGE DRAWING NUMBER(1)
OPA2107AP	Plastic DIP	006
OPA2107AM	Metal TO-99	001
OPA2107BM	Metal TO-99	001
OPA2107SM	Metal TO-99	001
OPA2107AU	SO-8 SOIC	182

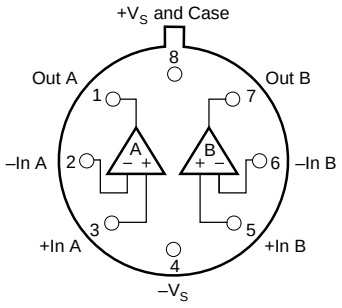
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

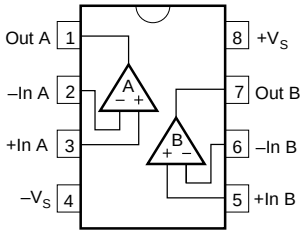
MODELS	PACKAGE	SPECIFICATION TEMPERATURE RANGE
OPA2107AP	Plastic DIP	–25 to +85°C
OPA2107AM	Metal TO-99	–25 to +85°C
OPA2107BM	Metal TO-99	–25 to +85°C
OPA2107SM	Metal TO-99	–55 to +125°C
OPA2107AU	SO-8 SOIC	–25 to +85°C

PIN CONFIGURATIONS

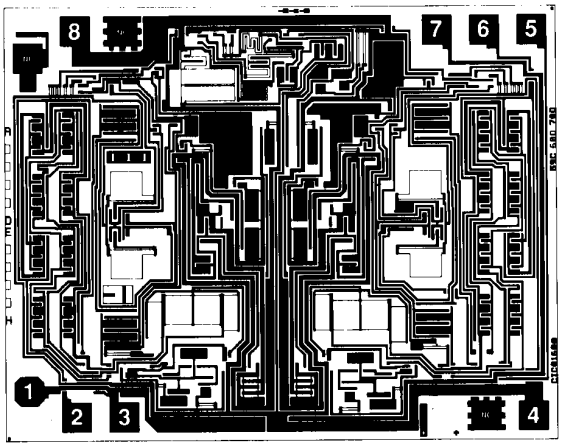
Top View – M Package



Top View – P & U Packages



DICE INFORMATION



OPA2107 DIE TOPOGRAPHY

PAD	FUNCTION
1	Out A
2	–In A
3	+In A
4	–V_S
5	+In B
6	–In B
7	Out B
8	+V_S

Substrate Bias: –V_S

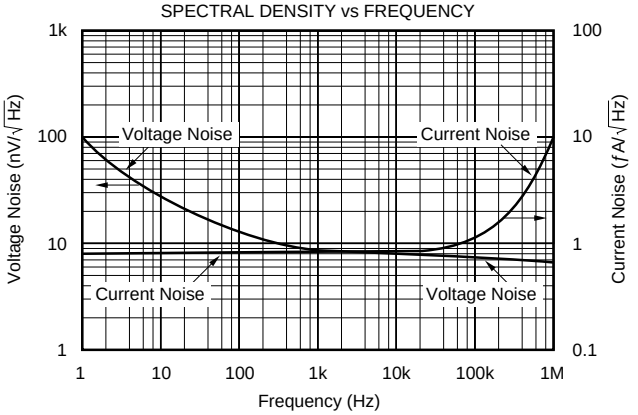
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	97 x 77 ±3	2.46 x 1.96 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Transistor Count		53
Backing		None

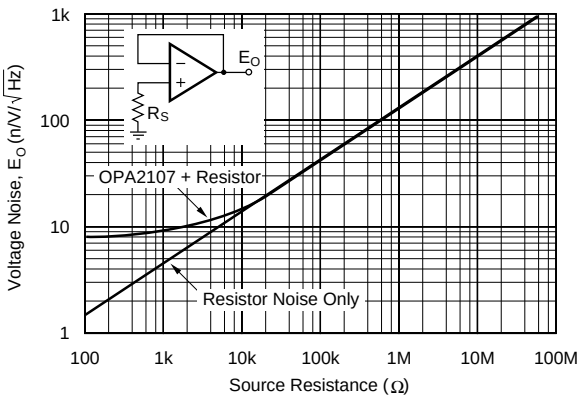
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

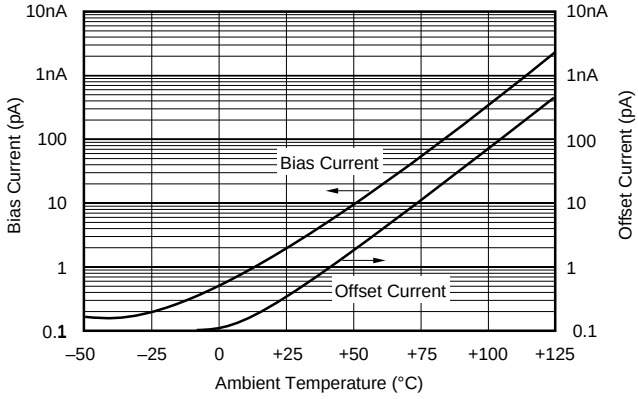
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



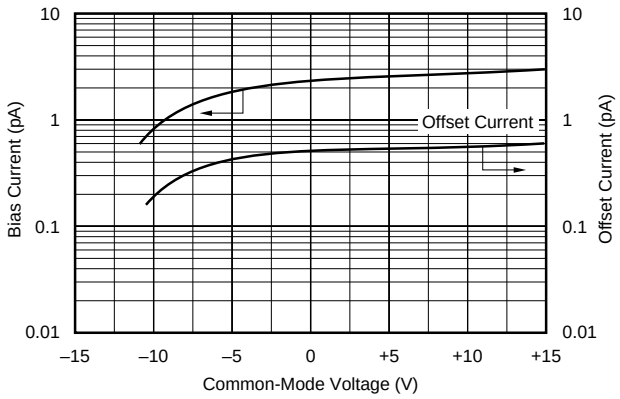
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY at 1kHz vs SOURCE RESISTANCE



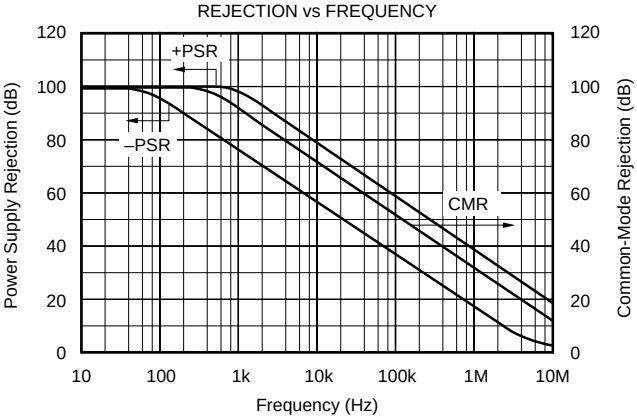
BIAS AND OFFSET CURRENT vs TEMPERATURE



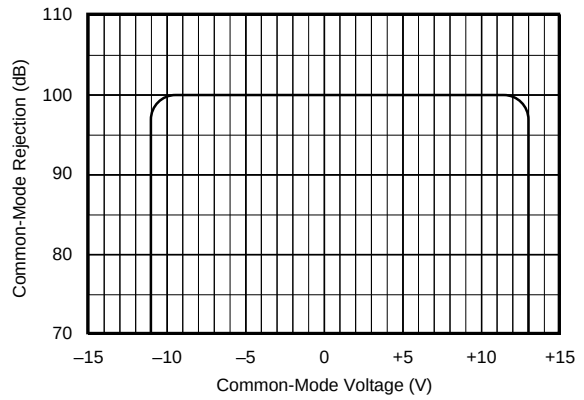
BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



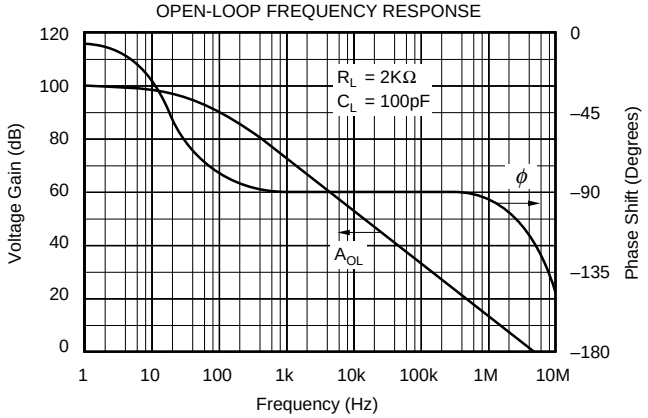
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



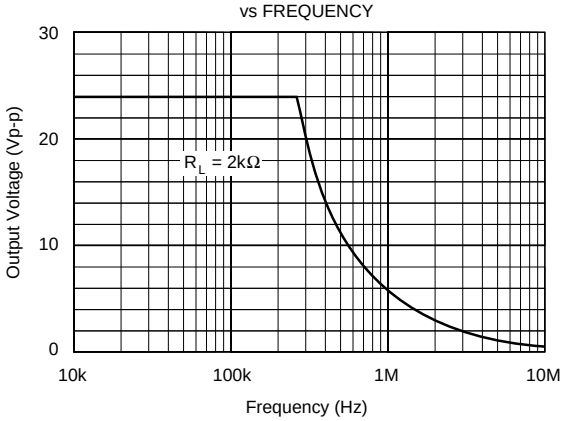
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

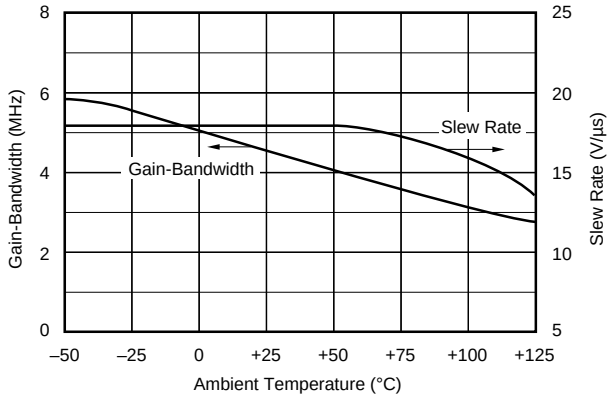
OPEN-LOOP FREQUENCY RESPONSE



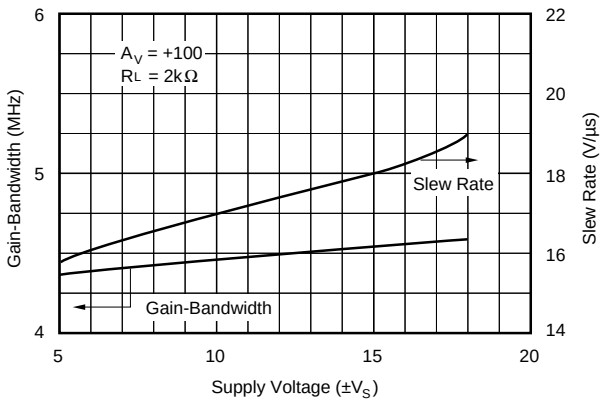
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



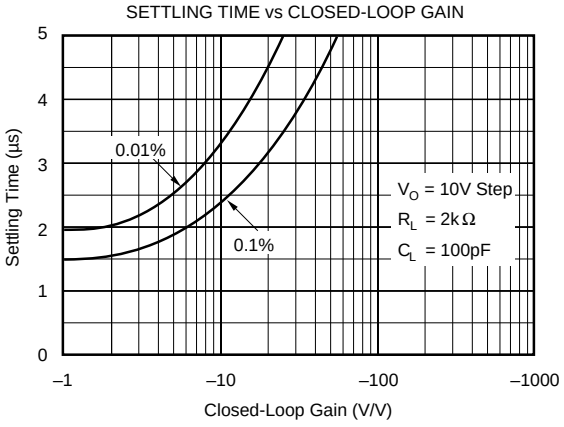
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



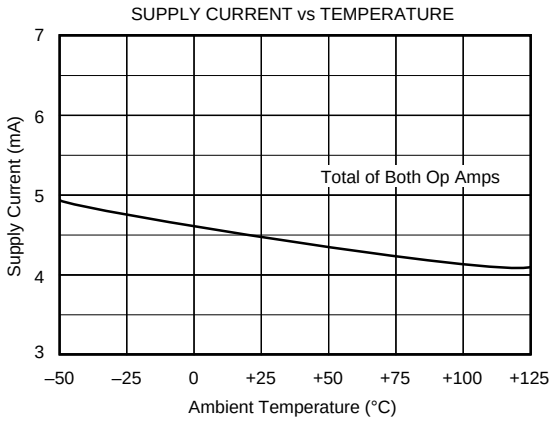
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



SETTLING TIME vs CLOSED-LOOP GAIN



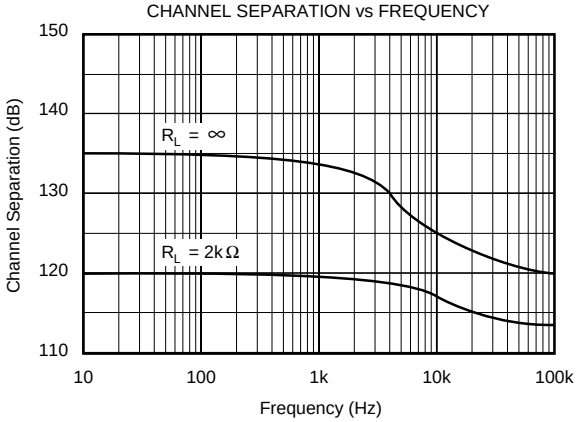
SUPPLY CURRENT vs TEMPERATURE



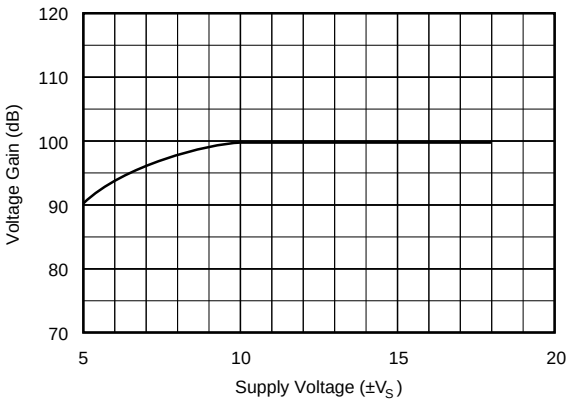
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

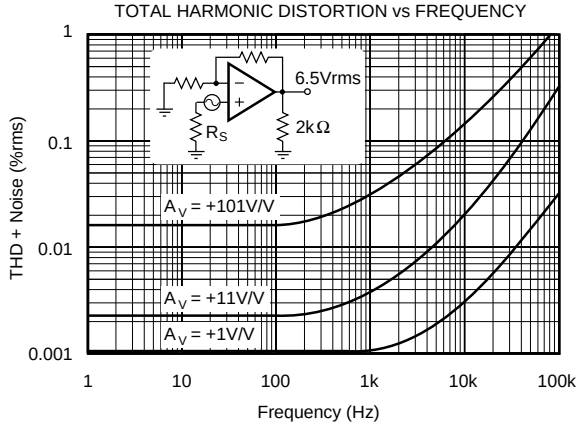
CHANNEL SEPARATION vs FREQUENCY



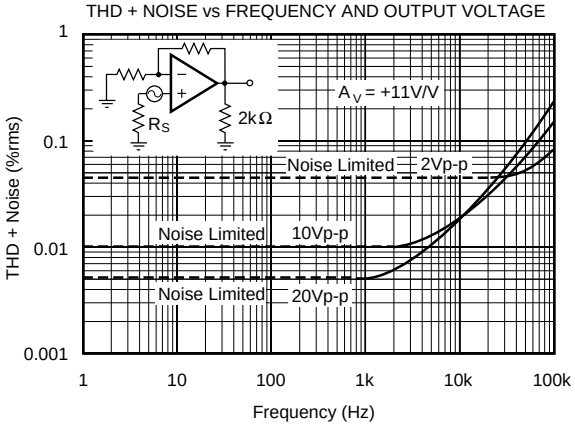
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



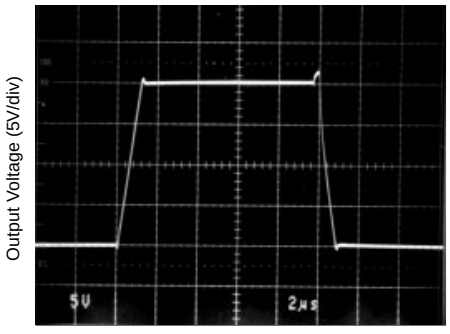
TOTAL HARMONIC DISTORTION vs FREQUENCY



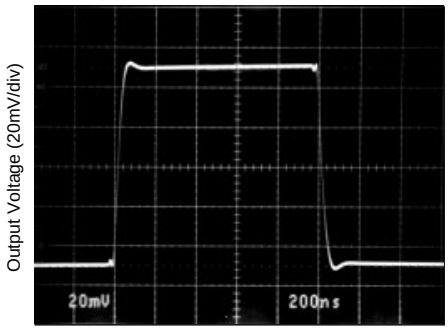
THD + NOISE vs FREQUENCY AND OUTPUT VOLTAGE



OPA2107 LARGE-SIGNAL RESPONSE



OPA2107 SMALL-SIGNAL RESPONSE



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has excellent phase margin. This makes it easy to use in a wide variety of applications.

Power supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1µF ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1µF tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107's ***Difet*** input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances a two-step cleaning process is adequate using a clean organic solvent rinse followed by de-ionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit board guard pattern effectively reduces errors due to circuit board leakage (Figure 1). By encircling critical high impedance nodes with a low impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

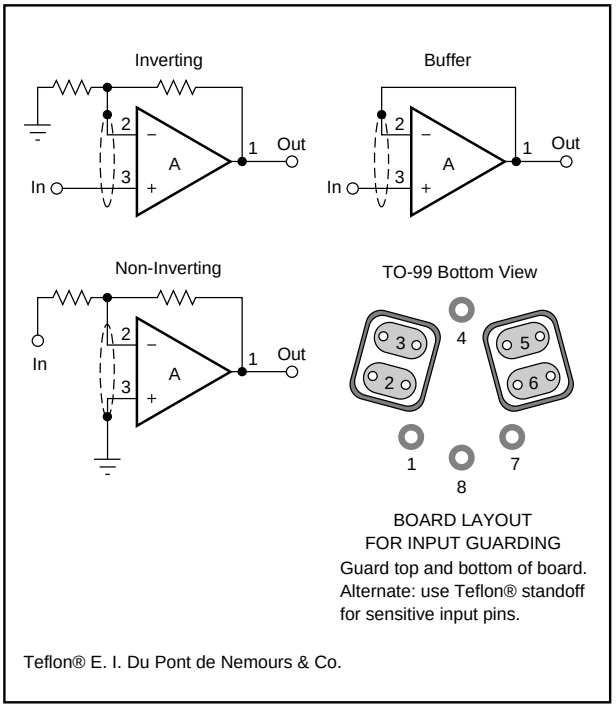


FIGURE 1. Connection of Input Guard.

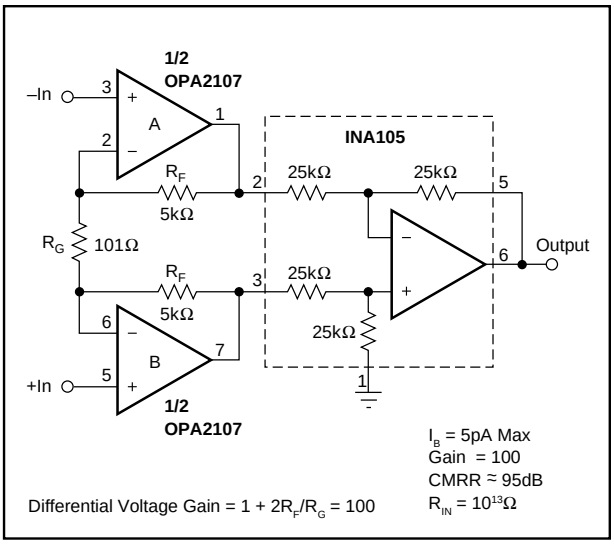


FIGURE 2. FET Input Instrumentation Amplifier.

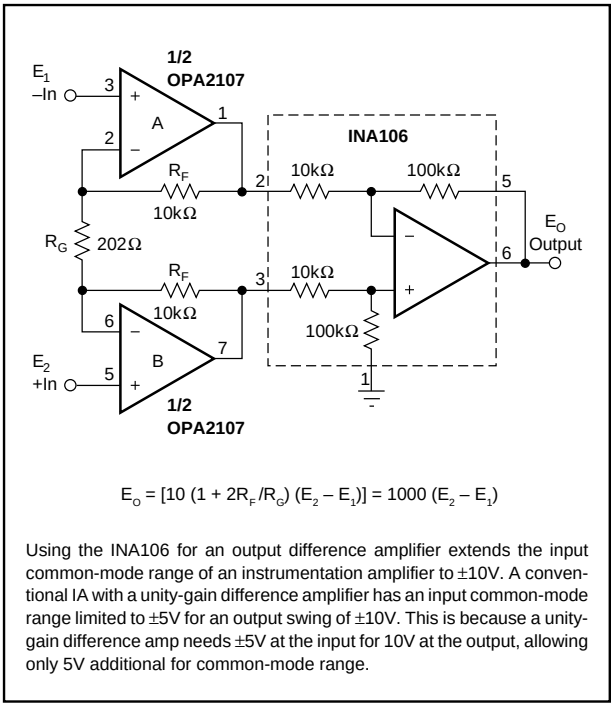
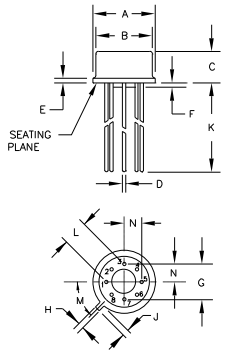


FIGURE 3. Precision Instrumentation Amplifier.

PACKAGE DRAWINGS

Package Number 001 - Metal TO-99

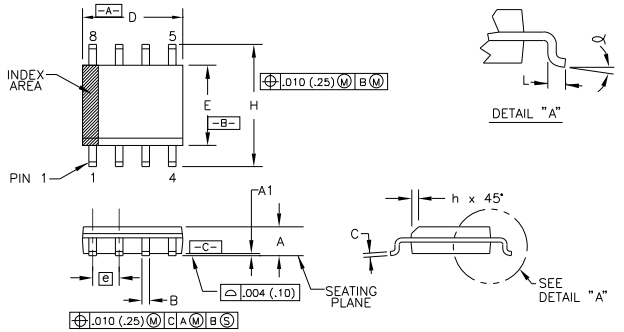


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.335	.380	8.51	9.65	
B	.305	.335	7.75	8.51	
C	.165	.185	4.19	4.70	
D	.016	.021	0.41	0.53	
E	.010	.040	0.25	1.02	
F	.010	.040	0.25	1.02	
G	.200 BASIC		5.08 BASIC		
H	.028	.034	0.71	0.86	
J	.029	.045	0.74	1.14	
K	.500	--	12.7	--	
L	.110	.160	2.79	4.06	
M	45° BASIC		45° BASIC		
N	.095	.105	2.41	2.67	

NOTES:
1. LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
2. PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ001 | REV.: B
JEDEC NUMBER: UNKNOWN

Package Number 182 - 8-Lead SOIC

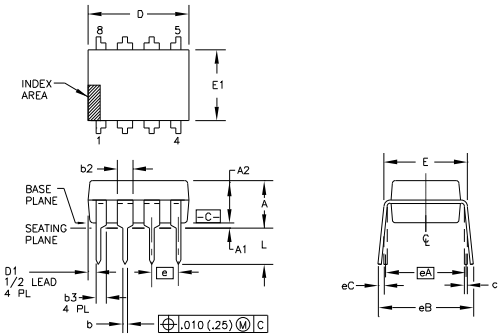


DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050 BASIC		1.27 BASIC		
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	
L	.016	.050	0.41	1.27	5
N	8		8		6
α	0°	8°	0°	8°	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
4. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
8. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182 | REV.: G
JEDEC NUMBER: MS-012-AA

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
eC	.000	.060	0.00	1.52	6
L	.115	.150	2.92	3.81	3
N	8		8		7

NOTES:
1. ALL DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM [-C-].
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. N IS THE MAXIMUM OF TERMINAL POSITIONS.
8. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
9. b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
10. DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
11. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
12. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 | REV.: E
JEDEC NUMBER: MS-001-BA