

OPA128

Difet[®] Electrometer-Grade OPERATIONAL AMPLIFIER

FEATURES

- **ULTRA-LOW BIAS CURRENT:** 75fA max
- **LOW OFFSET:** 500 μ V max
- **LOW DRIFT:** 5 μ V/ $^{\circ}$ C max
- **HIGH OPEN-LOOP GAIN:** 110dB min
- **HIGH COMMON-MODE REJECTION:** 90dB min
- **IMPROVED REPLACEMENT FOR AD515 AND AD549**

APPLICATIONS

- **ELECTROMETER**
- **MASS SPECTROMETER**
- **CHROMATOGRAPH**
- **ION GAUGE**
- **PHOTODETECTOR**
- **RADIATION-HARD EQUIPMENT**

DESCRIPTION

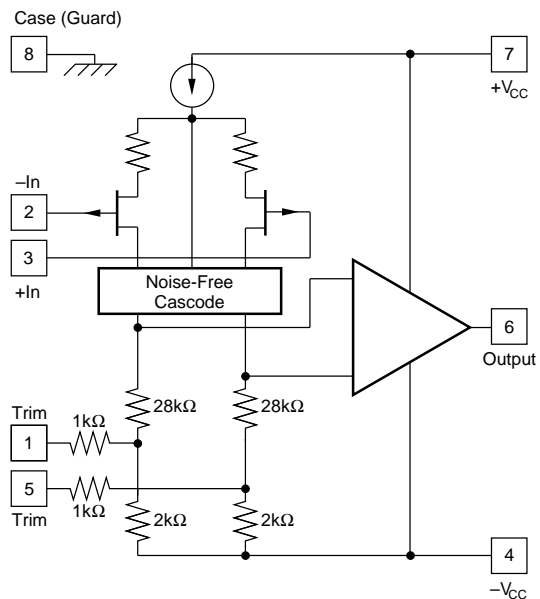
The OPA128 is an ultra-low bias current monolithic operational amplifier. Using advanced geometry dielectrically-isolated FET (*Difet*[®]) inputs, this monolithic amplifier achieves a performance level exceeding even the best hybrid electrometer amplifiers.

Laser-trimmed thin-film resistors give outstanding voltage offset and drift performance.

A noise-free cascode and low-noise processing give the OPA128 excellent low-level signal handling capabilities. Flicker noise is very low.

The OPA128 is an improved pin-for-pin replacement for the AD515.

Difet[®] Burr-Brown Corp.



OPA128 Simplified Circuit

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA128JM			OPA128KM			OPA128LM			OPA128SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0\text{VDC}$, $R_L \geq 10\text{k}\Omega$		± 150	± 300		± 75	± 150		± 40	± 75		± 75	± 150	fA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$, $R_L \geq 10\text{k}\Omega$		65			30			30			30		fA
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX}		± 260	± 1000 ± 20		± 140	± 500 ± 10		± 140	± 500 ± 5		± 140	± 500 ± 10	μV $\mu\text{V}/^\circ\text{C}$ dB $\mu\text{V}/\text{V}$
NOISE Voltage: $f_O = 10\text{Hz}$ $f_O = 100\text{Hz}$ $f_O = 1\text{kHz}$ $f_O = 10\text{kHz}$ $f_B = 10\text{Hz}$ to 10kHz $f_B = 0.1\text{Hz}$ to 10Hz Current: $f_B = 0.1\text{Hz}$ to 10Hz $f_O = 0.1\text{Hz}$ to 20kHz			92 78 27 15 2.4 4 4.2 0.22		92 78 27 15 2.4 4 3 0.16				92 78 27 15 2.4 4 2.3 0.12			92 78 27 15 2.4 4 3 0.16	$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ μVrms $\mu\text{Vp-p}$ fA, p-p fA/ $\sqrt{\text{Hz}}$	
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{15} \parallel 2$		$10^{13} \parallel 1$ $10^{15} \parallel 2$				$10^{13} \parallel 1$ $10^{15} \parallel 2$			$10^{13} \parallel 1$ $10^{15} \parallel 2$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
VOLTAGE RANGE⁽⁴⁾ Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10	± 12		± 10	± 12		± 10	± 12		± 10	± 12		V dB
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	94	128		110	128		110	128		110	128		dB
Unity Gain, Small Signal Full Power Response Slew Rate Settling Time, 0.1% 0.01% Overload Recovery, 50% Overdrive ⁽³⁾	⁽²⁾ 20Vp-p, $R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$ Gain = -1, $R_L = 2\text{k}\Omega$ 10V Step Gain = -1	0.5	1 47 3 5 10 5		0.5	1 47 3 5 10 5		0.5	1 47 3 5 10 5		0.5	1 47 3 5 10 5		MHz kHz V/ μs μs μs μs
Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ DC, Open Loop Gain = +1	± 10 ± 5	± 13 ± 10 100 1000		± 10 ± 5	± 13 ± 10 100 1000		± 10 ± 5	± 13 ± 10 100 1000		± 10 ± 5	± 13 ± 10 100 1000		V mA Ω pF mA
Rated Voltage Voltage Range, Derated Performance Current, Quiescent	$I_O = 0\text{mADC}$	± 5	± 15 ± 18		± 5	± 15 ± 18		± 5	± 15 ± 18		± 5	± 15 ± 18		VDC VDC mA
Specification Operating Storage θ Junction-Ambient	Ambient Temp. Ambient Temp. Ambient Temp.	0 -55 -65		+70 +125 +150	0 -55 -65		+70 +125 +150	0 -55 -65		+70 +125 +150	-55 -55 -65		+125 +125 +150	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. Bias current doubles approximately every 11°C . (2) Sample tested. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

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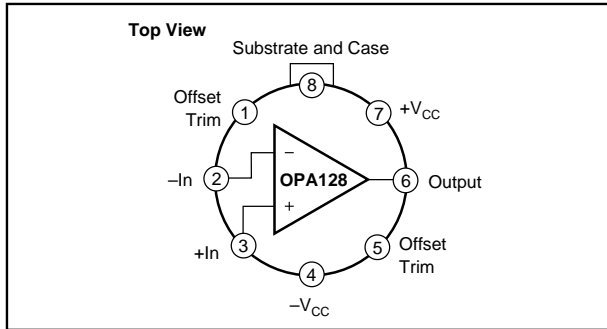
ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{\text{MIN}}$ and T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA128JM			OPA128KM			OPA128LM			OPA128SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE														
Specification Range	Ambient Temp.	0		+70	0		+70	0		+70	-55		+125	°C
INPUT														
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0\text{VDC}$		±2.5	±8		±1.3	±4		±0.7	±2		±43	±170	pA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$		1.1			0.6			0.6			18		pA
OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$			±2.2mV ±20			±1mV ±10			±750 ±5			±1.5mV ±10	μV μV/°C dB μV/V
VOLTAGE RANGE⁽²⁾ Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	±10 74	±11 112		±10 80	±11 112		±10 80	±11 112		±10 74	±11 104		V dB
OPEN-LOOP GAIN, DC														
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	90	125		104	125		104	125		90	122		dB
RATED OUTPUT														
Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	±10 ±5 10			±10 ±5 10		22		±10 ±5 10		22		18	V mA mA
POWER SUPPLY														
Current, Quiescent	$I = 0\text{mADC}$		0.9	1.8		0.9	1.8		0.9	1.8		0.9	2	mA

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (2) If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can withstand overload currents of 0.3mA indefinitely without damage.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal Power Dissipation ⁽¹⁾	500mW
Differential Input Voltage	±36VDC
Input Voltage Range	±18VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration ⁽²⁾	Continuous
Junction Temperature	+175°C

NOTES: (1) Packages must be derated based on $\theta_{CA} = 150^\circ\text{C/W}$ or $\theta_{JA} = 200^\circ\text{C/W}$. (2) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J .

ORDERING INFORMATION

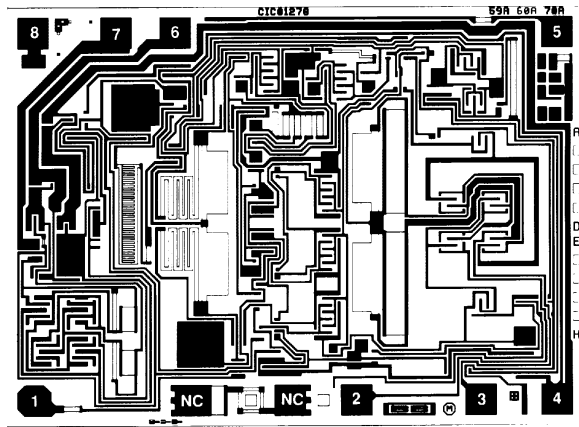
MODEL	PACKAGE	TEMPERATURE RANGE	BIAS CURRENT, max (fA)
OPA128JM	TO-99	0°C to +70°C	±300
OPA128KM	TO-99	0°C to +70°C	±150
OPA128LM	TO-99	0°C to +70°C	±75
OPA128SM	TO-99	-55°C to +125°C	±150

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA128JM	TO-99	001
OPA128KM	TO-99	001
OPA128LM	TO-99	001
OPA128SM	TO-99	001

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

DICE INFORMATION



OPA128 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	-V _{CC}
5	Offset Trim
6	Output
7	+V _{CC}
8	Substrate
NC	No Connection

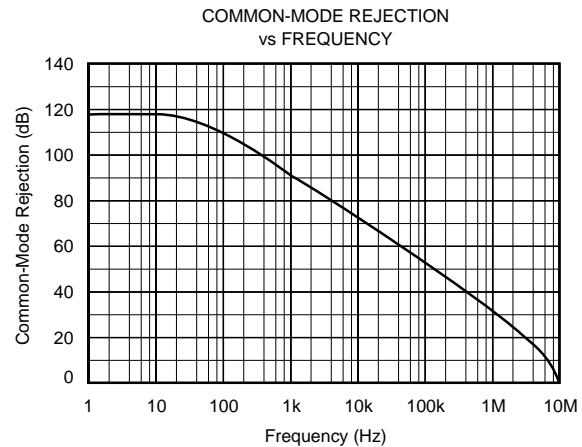
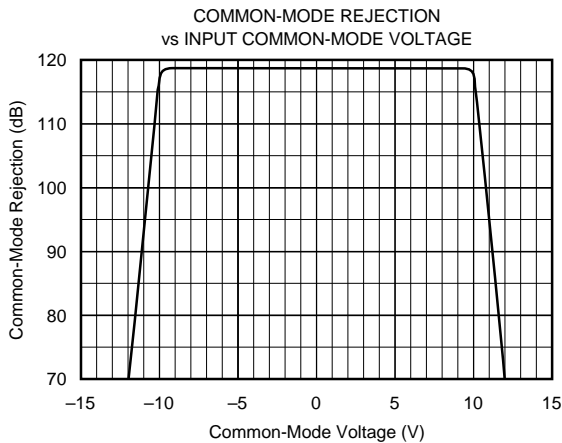
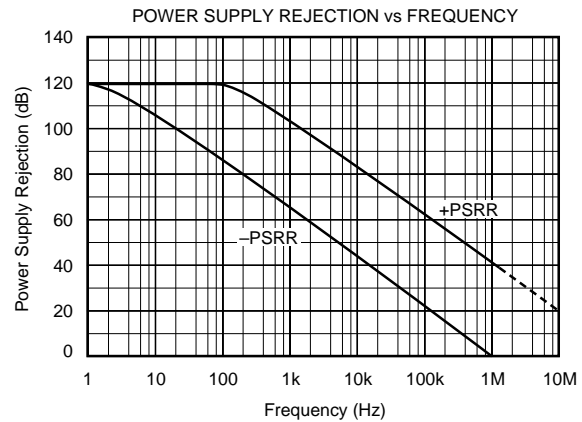
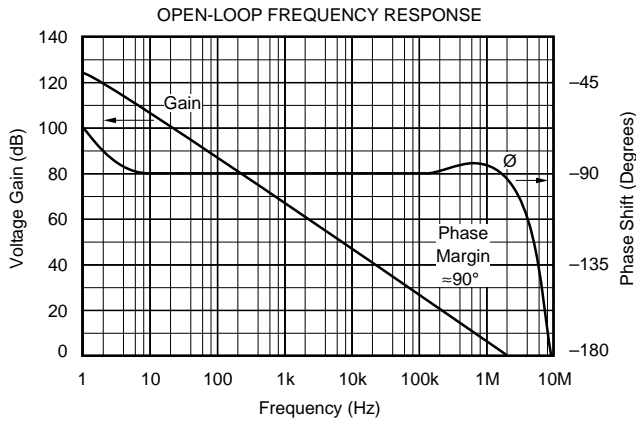
Substrate Bias: Isolated, normally connected to common.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	96 x 71 ±5	2.44 x 1.80 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	None	

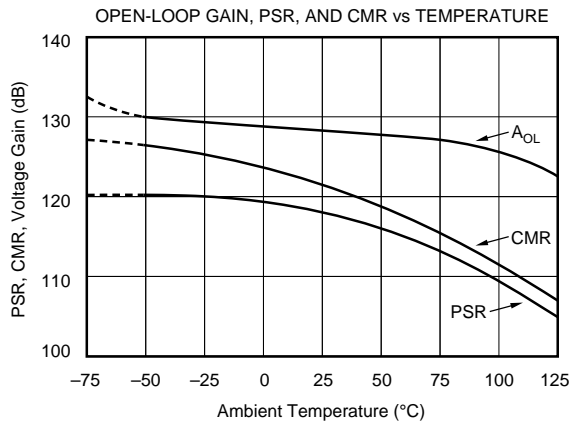
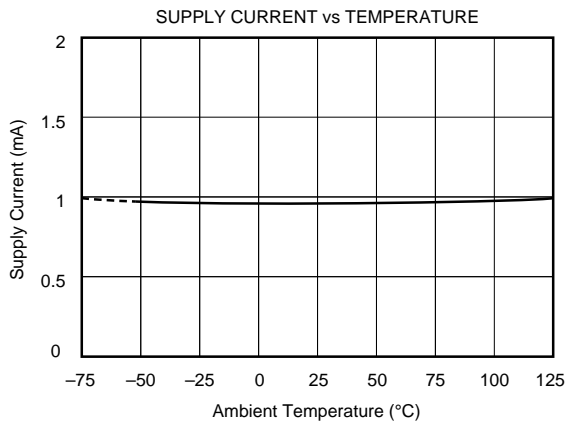
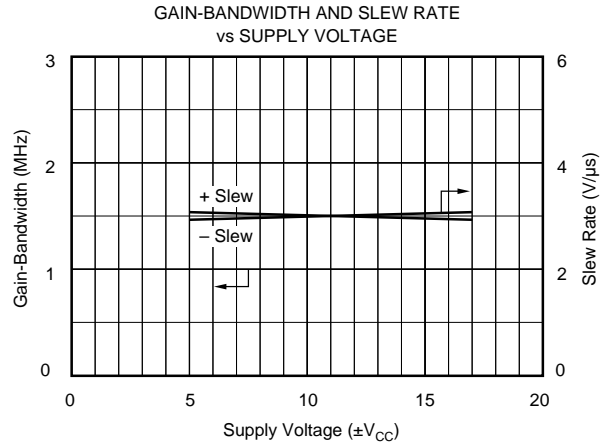
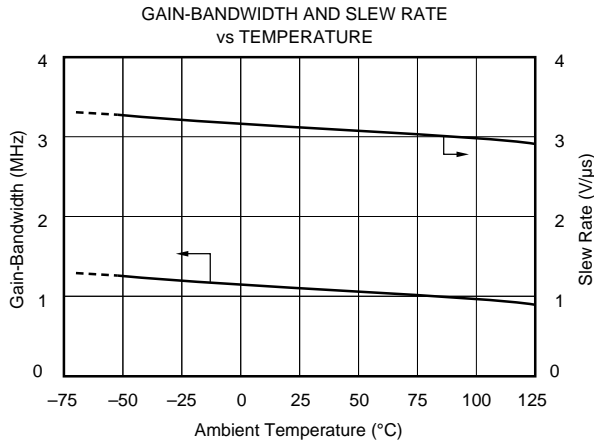
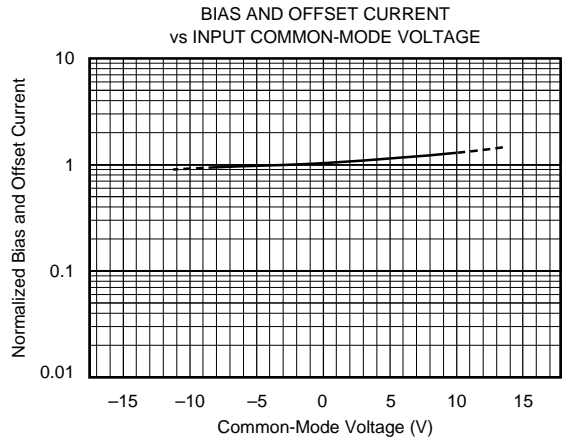
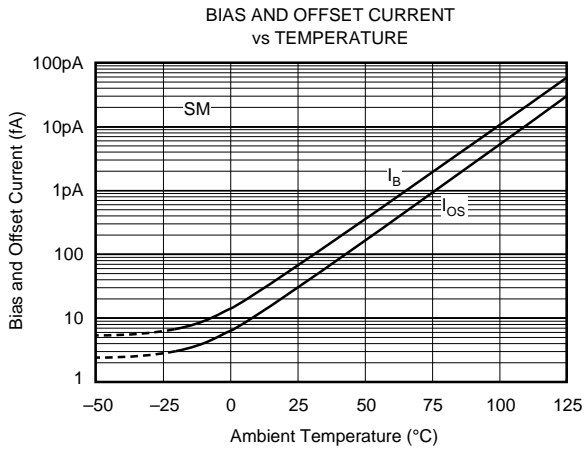
TYPICAL PERFORMANCE CURVES

T_A = +25°C, ±15VDC, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

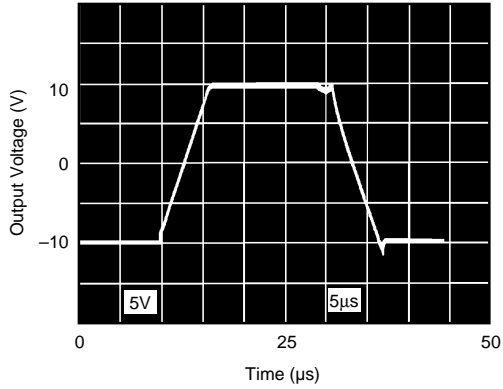
At $T_A = +25^\circ\text{C}$, +15VDC unless otherwise noted.



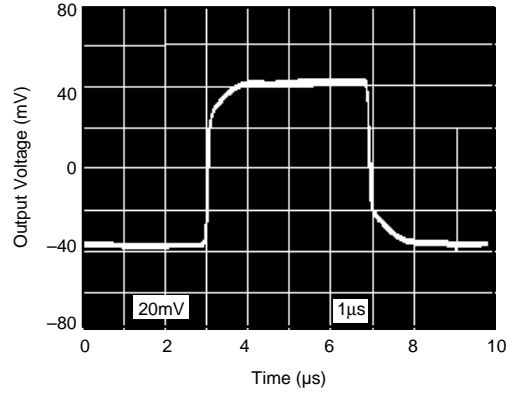
TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25^\circ\text{C}$, +15VDC unless otherwise noted.

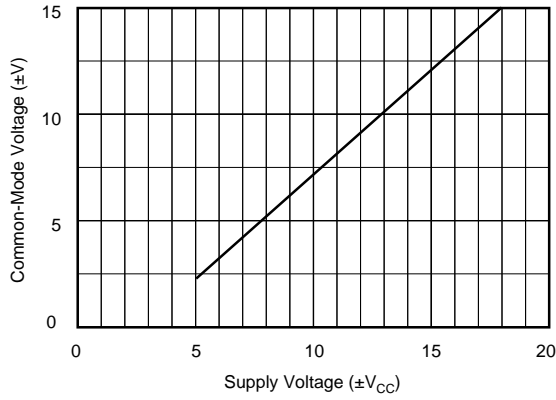
LARGE SIGNAL TRANSIENT RESPONSE



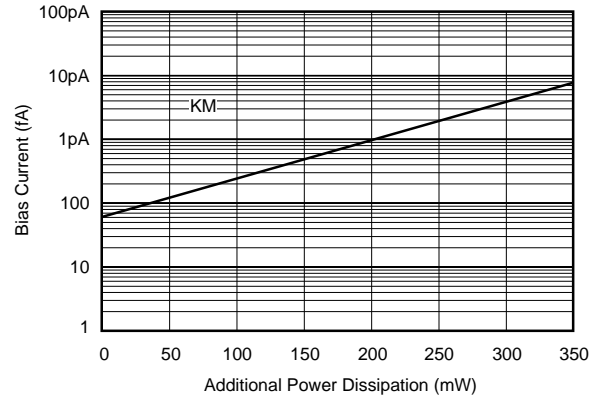
SMALL SIGNAL TRANSIENT RESPONSE



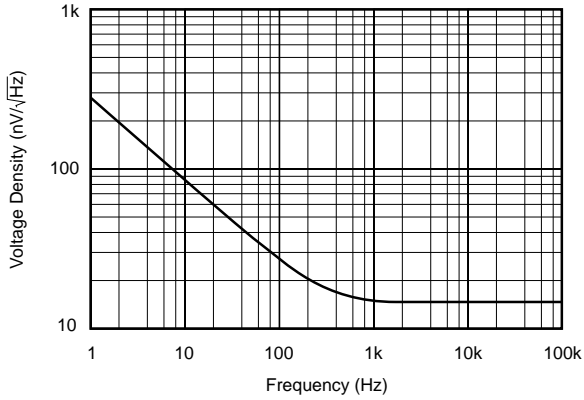
COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE



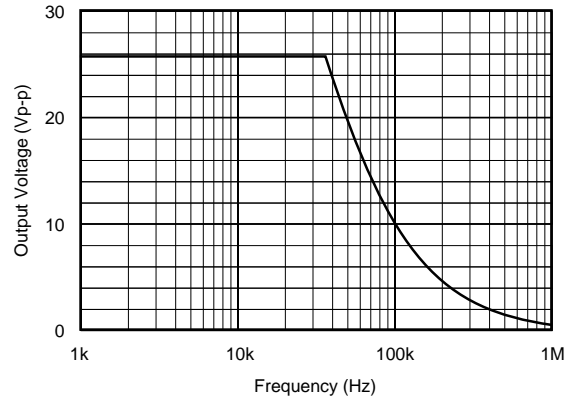
BIAS CURRENT vs ADDITIONAL POWER DISSIPATION



INPUT VOLTAGE NOISE SPECTRAL DENSITY



FULL-POWER OUTPUT vs FREQUENCY



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA128 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted effort. Note that the trim (Figure 1) is similar to operational amplifiers such as HA-5180 and AD515. The OPA128 can replace many other amplifiers by leaving the external null circuit unconnected.

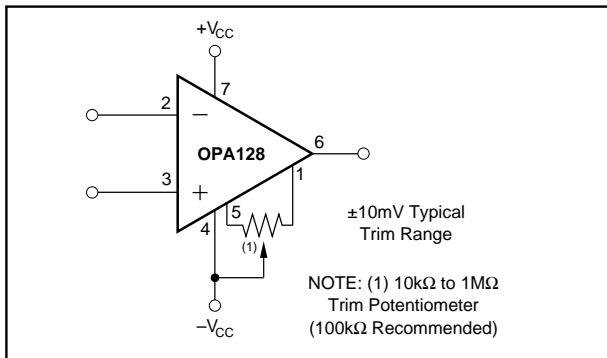


FIGURE 1. Offset Voltage Trim.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers' inputs must be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET® amplifiers can be destroyed by the loss of $-V_{CC}$.

Because of its dielectric isolation, no special protection is needed on the OPA128. Of course, the differential and common-mode voltage limits should be observed.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry. Leakage currents across printed circuit boards can easily exceed the bias current of the OPA128. To avoid leakage problems, it is recommended that the signal input lead of the OPA128 be wired to a Teflon standoff. If the input is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 2).

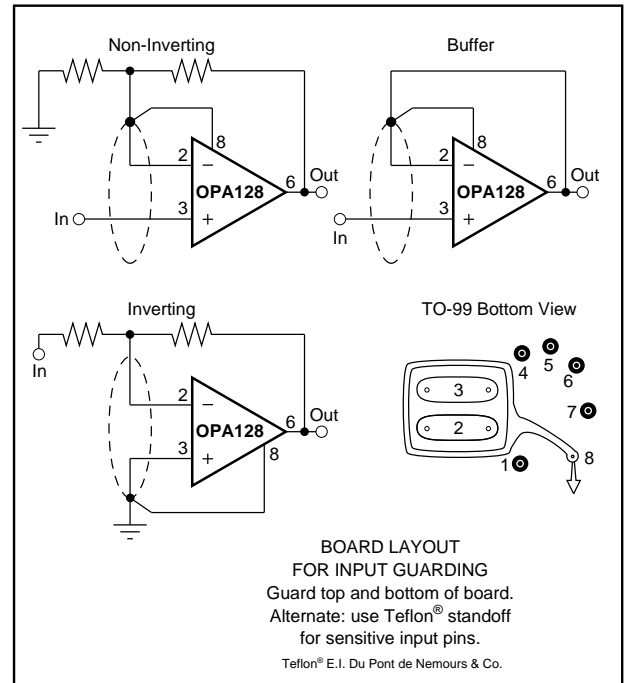


FIGURE 2. Connection of Input Guard.

Triboelectric charge (static electricity generated by friction) can be a troublesome noise source from cables connected to the input of an electrometer amplifier. Special low-noise cable will minimize this effect but the optimum solution is to mount the signal source directly at the electrometer input with short, rigid, wiring to preclude microphonic noise generation.

TESTING

Accurately testing the OPA128 is extremely difficult due to its high level of performance. Ordinary test equipment may not be able to resolve the amplifier's extremely low bias current.

Inaccurate bias current measurements can be due to:

1. Test socket leakage
2. Unclean package
3. Humidity or dew point condensation
4. Circuit contamination from fingerprints or anti-static treatment chemicals
5. Test ambient temperature
6. Load power dissipation

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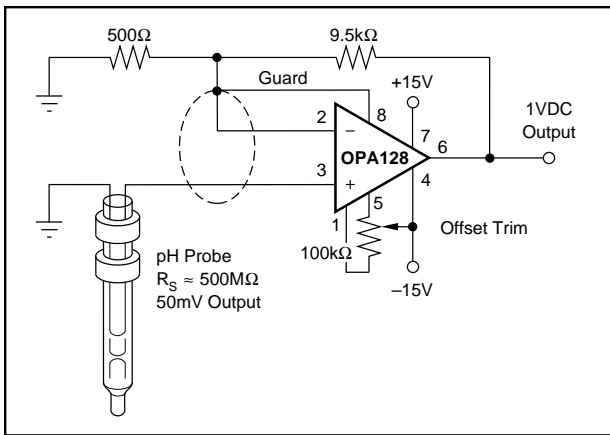


FIGURE 3. High Impedance ($10^{15}\Omega$) Amplifier.

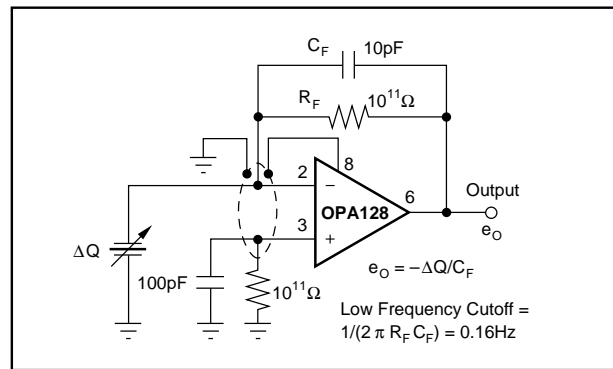


FIGURE 4. Piezoelectric Transducer Charge Amplifier.

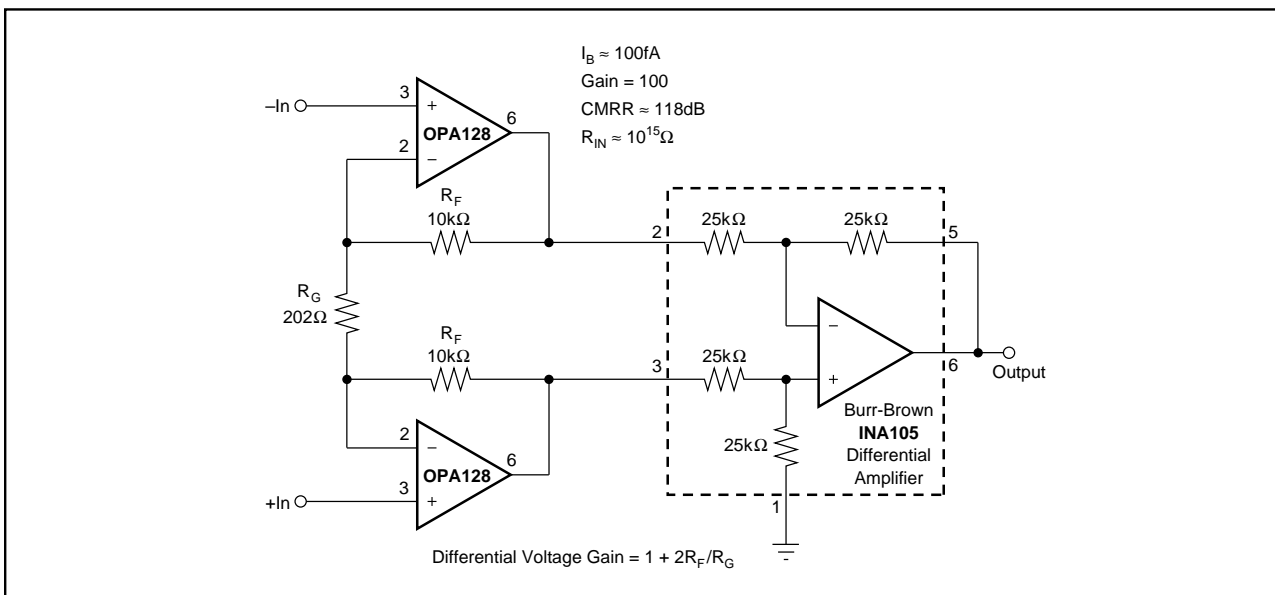


FIGURE 5. FET Input Instrumentation Amplifier for Biomedical Applications.

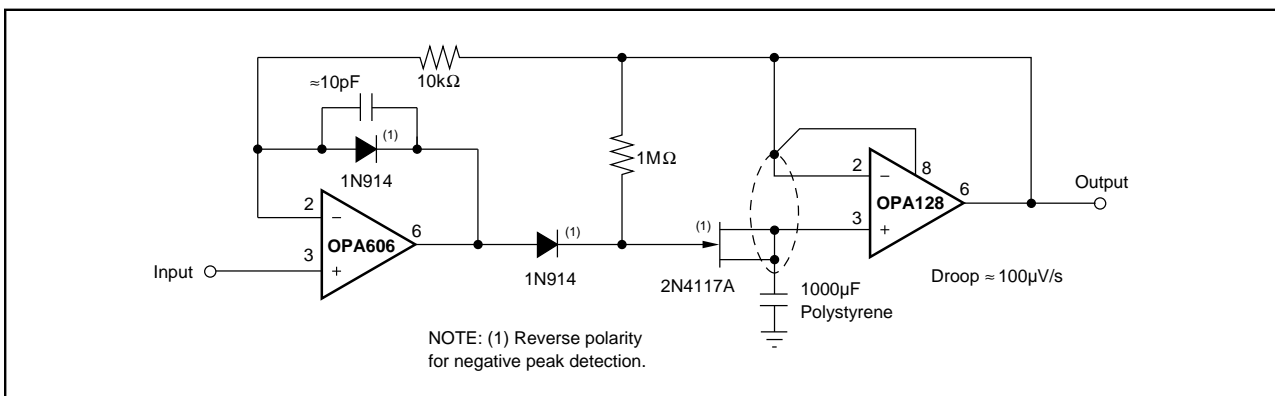


FIGURE 6. Low-Droop Positive Peak Detector.

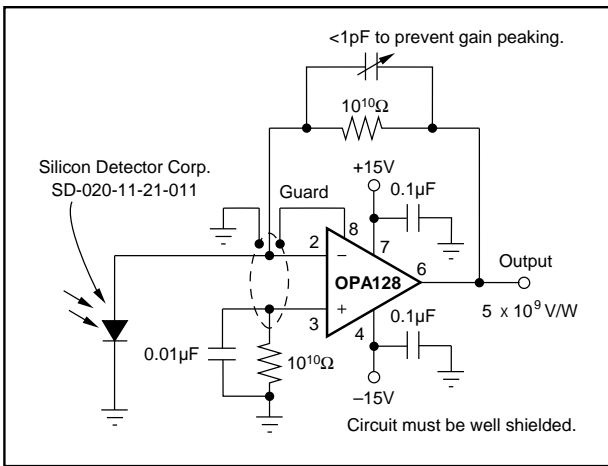


FIGURE 7. Sensitive Photodiode Amplifier.

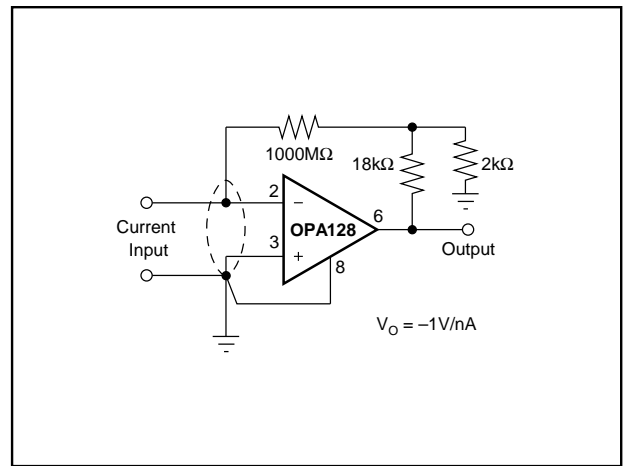


FIGURE 8. Current-to-Voltage Converter.

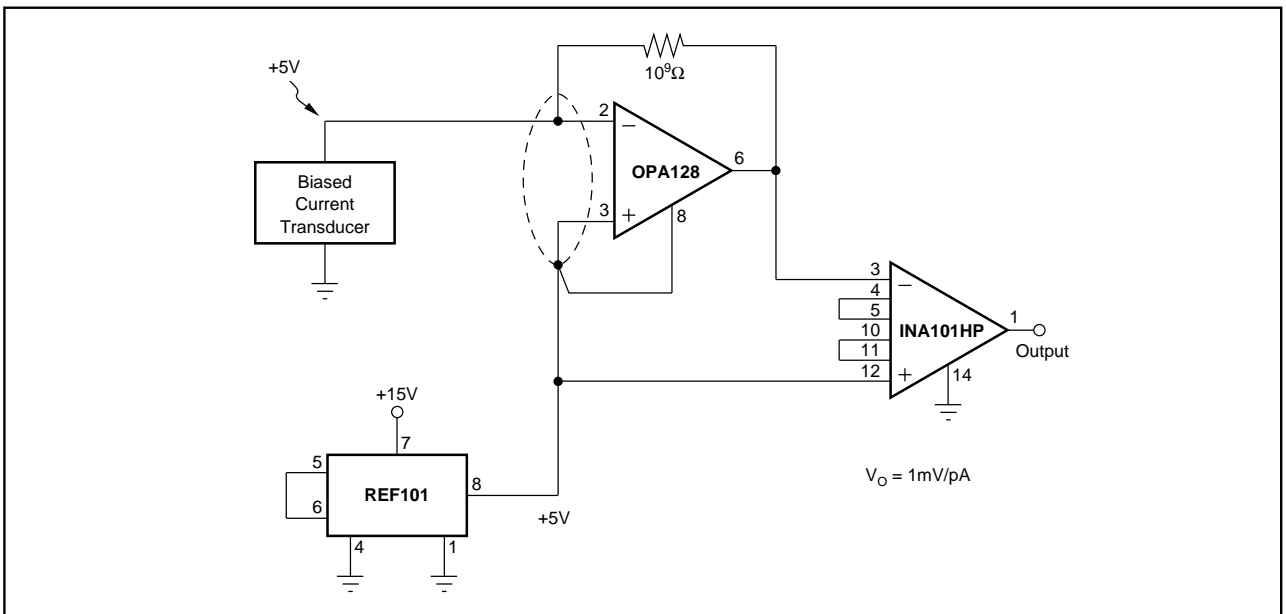
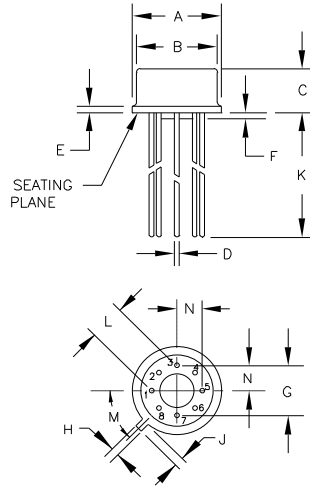


FIGURE 9. Biased Current-to-Voltage Converter.

PACKAGE DRAWINGS

Package Number 001 - Metal TO-99



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.335	.380	8.51	9.65	
B	.305	.335	7.75	8.51	
C	.165	.185	4.19	4.70	
D	.016	.021	0.41	0.53	
E	.010	.040	0.25	1.02	
F	.010	.040	0.25	1.02	
G	.200	BASIC	5.08	BASIC	
H	.028	.034	0.71	0.86	
J	.029	.045	0.74	1.14	
K	.500	--	12.7	--	
L	.110	.160	2.79	4.06	
M	45°	BASIC	45°	BASIC	
N	.095	.105	2.41	2.67	

NOTES:

- LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.
- PIN NUMBERS SHOWN FOR REFERENCE ONLY. NUMBERS MAY NOT BE MARKED ON PACKAGE.

PACKAGE NUMBER: ZZ001 REV.: B
 JEDEC NUMBER: UNKNOWN