



# OPA124

## Low Noise Precision *Difet*<sup>®</sup> OPERATIONAL AMPLIFIER

### FEATURES

- **LOW NOISE:**  $6\text{nV}/\sqrt{\text{Hz}}$  (10kHz)
- **LOW BIAS CURRENT:** 1pA max
- **LOW OFFSET:** 250 $\mu\text{V}$  max
- **LOW DRIFT:** 2 $\mu\text{V}/^\circ\text{C}$  max
- **HIGH OPEN-LOOP GAIN:** 120dB min
- **HIGH COMMON-MODE REJECTION:** 100dB min
- **AVAILABLE IN 8-PIN PLASTIC DIP AND 8-PIN SOIC PACKAGES**

### DESCRIPTION

The OPA124 is a precision monolithic FET operational amplifier using a *Difet* (dielectrical isolation) manufacturing process. Outstanding DC and AC performance characteristics allow its use in the most critical instrumentation applications.

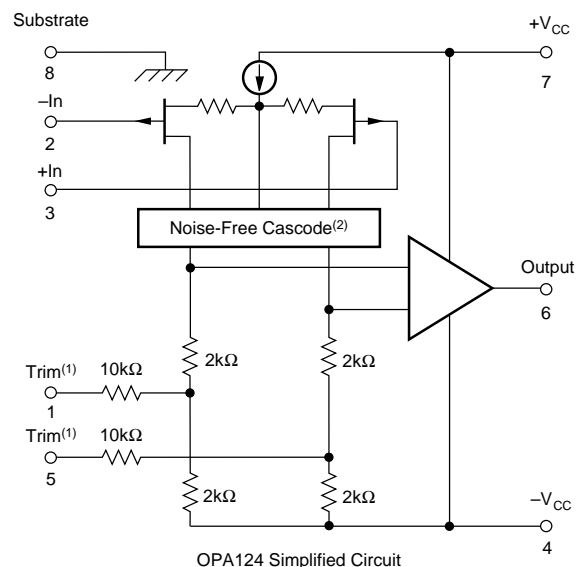
Bias current, noise, voltage offset, drift, open-loop gain, common-mode rejection and power supply rejection are superior to BIFET and CMOS amplifiers. *Difet* fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry. This cascode design also allows high precision input specifications and reduced susceptibility to flicker noise. Laser trimming of thin-film resistors gives very low offset and drift.

Compared to the popular OPA111, the OPA124 gives comparable performance and is available in an 8-pin PDIP and 8-pin SOIC package.

BIFET<sup>®</sup> National Semiconductor Corp.,  
*Difet*<sup>®</sup> Burr-Brown Corp.

### APPLICATIONS

- **PRECISION PHOTODIODE PREAMP**
- **MEDICAL EQUIPMENT**
- **OPTOELECTRONICS**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**



NOTES: (1) Omitted on SOIC. (2) Patented.

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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

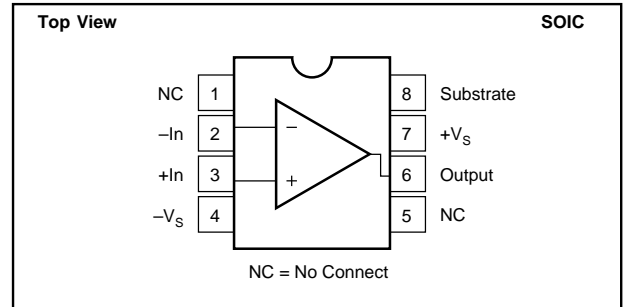
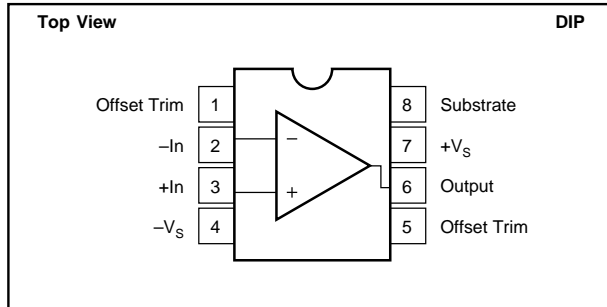
## ELECTRICAL

At  $V_{CC} = \pm 15\text{VDC}$  and  $T_A = +25^\circ\text{C}$  unless otherwise noted.

PARAMETER	CONDITION	OPA124U/P			OPA124UA/PA			OPA124UB/PB			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
<b>INPUT NOISE</b> Voltage, $f_O = 10\text{Hz}^{(4)}$ $f_O = 100\text{Hz}^{(4)}$ $f_O = 1\text{kHz}^{(4)}$ $f_O = 10\text{kHz}^{(5)}$ $f_B = 10\text{Hz}$ to $10\text{kHz}^{(5)}$ $f_B = 0.1\text{Hz}$ to $10\text{Hz}$ Current, $f_B = 0.1\text{Hz}$ to $10\text{Hz}$ $f_O = 0.1\text{Hz}$ thru $20\text{kHz}$			40	80		40	80		40	80	$\text{nV}/\sqrt{\text{Hz}}$	
			15	40		15	40		15	40	$\text{nV}/\sqrt{\text{Hz}}$	
				8	15		8	15		8	15	$\text{nV}/\sqrt{\text{Hz}}$
				6	8		6	8		6	8	$\text{nV}/\sqrt{\text{Hz}}$
				0.7	1.2		0.7	1.2		0.7	1.2	$\mu\text{Vrms}$
				1.6	3.3		1.6	3.3		1.6	3.3	$\mu\text{Vp-p}$
			9.5	15		9.5	15		9.5	15	$\text{fAp-p}$	
			0.5	0.8		0.5	0.8		0.5	0.8	$\text{fA}/\sqrt{\text{Hz}}$	
<b>OFFSET VOLTAGE<sup>(1)</sup></b> Input Offset Voltage vs Temperature Supply Rejection vs Temperature	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to $T_{MAX}$ $V_{CC} = \pm 10\text{V}$ to $\pm 18\text{V}$ $T_A = T_{MIN}$ to $T_{MAX}$		$\pm 200$	$\pm 800$		$\pm 150$	$\pm 500$		$\pm 100$	$\pm 250$	$\mu\text{V}$	
				$\pm 4$	$\pm 7.5$		$\pm 2$	$\pm 4$		$\pm 1$	$\pm 2$	$\mu\text{V}/^\circ\text{C}$
			88	110		90	110		100	110		dB
		84	100		86	100		90	100		dB	
<b>BIAS CURRENT<sup>(1)</sup></b> Input Bias Current	$V_{CM} = 0\text{VDC}$		$\pm 1$	$\pm 5$		$\pm 0.5$	$\pm 2$		$\pm 0.35$	$\pm 1$	$\mu\text{A}$	
<b>OFFSET CURRENT<sup>(1)</sup></b> Input Offset Current	$V_{CM} = 0\text{VDC}$		$\pm 1$	$\pm 5$		$\pm 0.5$	$\pm 1$		$\pm 0.25$	$\pm 0.5$	$\mu\text{A}$	
<b>IMPEDANCE</b> Differential Common-Mode			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		$\Omega \parallel \text{pF}$	
			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		$\Omega \parallel \text{pF}$	
<b>VOLTAGE RANGE</b> Common-Mode Input Range Common-Mode Rejection vs Temperature	$V_{IN} = \pm 10\text{VDC}$ $T_A = T_{MIN}$ to $T_{MAX}$	$\pm 10$	$\pm 11$		$\pm 10$	$\pm 11$		$\pm 10$	$\pm 11$		V	
		92	110		94	110		100	110		dB	
		86	100		86	100		90	100		dB	
<b>OPEN-LOOP GAIN, DC</b> Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	106	125		106	125		120	125		dB	
<b>FREQUENCY RESPONSE</b> Unity Gain, Small Signal Full Power Response Slew Rate THD Settling Time, 0.1% 0.01% Overload Recovery, 50% Overdrive <sup>(2)</sup>	$20\text{Vp-p}$ , $R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{V}$ , $R_L = 2\text{k}\Omega$ Gain = $-1$ , $R_L = 2\text{k}\Omega$ 10V Step Gain = $-1$		1.5			1.5			1.5		MHz	
			16	32		16	32		16	32		kHz
			1	1.6		1	1.6		1	1.6		$\text{V}/\mu\text{s}$
				0.0003			0.0003			0.0003		%
				6			6			6		$\mu\text{s}$
				10			10			10		$\mu\text{s}$
				5			5			5		$\mu\text{s}$
<b>RATED OUTPUT</b> Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ DC, Open Loop Gain = $+1$	$\pm 11$	$\pm 12$		$\pm 11$	$\pm 12$		$\pm 11$	$\pm 12$		V	
		$\pm 5.5$	$\pm 10$		$\pm 5.5$	$\pm 10$		$\pm 5.5$	$\pm 10$		mA	
			100			100			100		$\Omega$	
			1000			1000			1000		pF	
		10	40		10	40		10	40		mA	
<b>POWER SUPPLY</b> Rated Voltage Voltage Range, Derated Current, Quiescent	$I_O = 0\text{mADC}$	$\pm 5$	$\pm 15$		$\pm 5$	$\pm 15$		$\pm 5$	$\pm 15$		VDC	
			2.5	$\pm 18$	$\pm 5$	2.5	$\pm 18$	$\pm 5$	2.5	$\pm 18$	VDC	
				3.5			3.5			3.5	mA	
<b>TEMPERATURE RANGE</b> Specification Storage $\theta$ Junction-Ambient: PDIP SOIC	$T_{MIN}$ and $T_{MAX}$	-25		+85	-25		+85	-25		+85	$^\circ\text{C}$	
		-65		+125	-65		+125	-65		+125	$^\circ\text{C}$	
			90			90			90		$^\circ\text{C}/\text{W}$	
			100			100			100		$^\circ\text{C}/\text{W}$	

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. For performance at other temperatures see Typical Performance Curves. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (3) For performance at other temperatures see Typical Performance Curves. (4) Sample tested, 98% confidence. (5) Guaranteed by design.

## CONNECTION DIAGRAMS



## ABSOLUTE MAXIMUM RATINGS

Supply .....	±18VDC
Internal Power Dissipation <sup>(1)</sup> .....	750mW
Differential Input Voltage <sup>(2)</sup> .....	±36VDC
Input Voltage Range <sup>(2)</sup> .....	±18VDC
Storage Temperature Range .....	-65°C to +150°C
Operating Temperature Range .....	-40°C to +125°C
Lead Temperature (soldering, 10s) .....	+300°C
Output Short Circuit Duration <sup>(3)</sup> .....	Continuous
Junction Temperature .....	+175°C

NOTES: (1) Packages must be derated based on  $\theta_{JA} = 90^{\circ}\text{C/W}$  for PDIP and  $100^{\circ}\text{C/W}$  for SOIC. (2) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to  $+18\text{V} > V_{IN} > -V_{CC} - 6\text{V}$ . See Figure 2. (3) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and  $T_J$ .

## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
OPA124U	8-Pin SOIC	182
OPA124P	8-Pin Plastic DIP	006
OPA124UA	8-Pin SOIC	182
OPA124PA	8-Pin Plastic DIP	006
OPA124UB	8-Pin SOIC	182
OPA124PB	8-Pin Plastic DIP	006

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

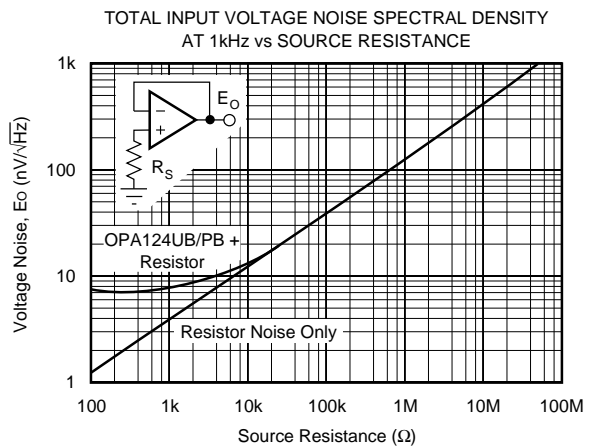
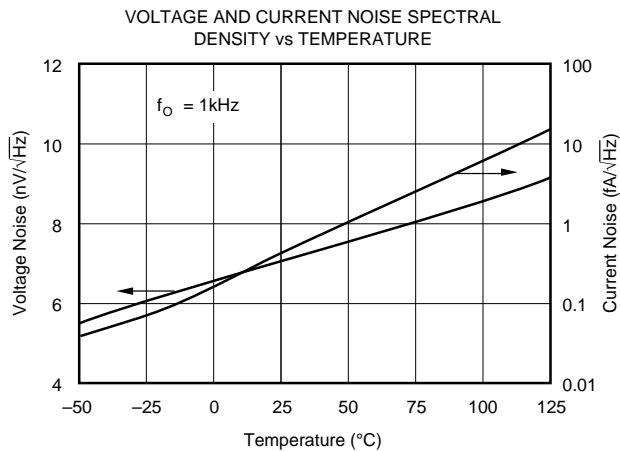
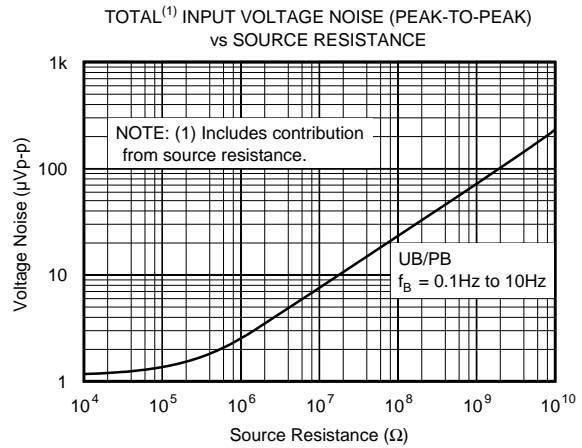
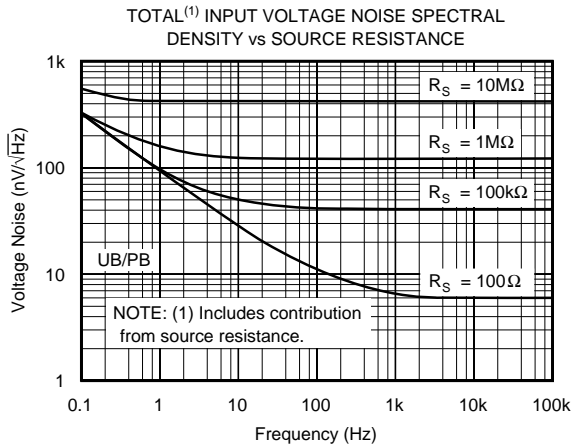
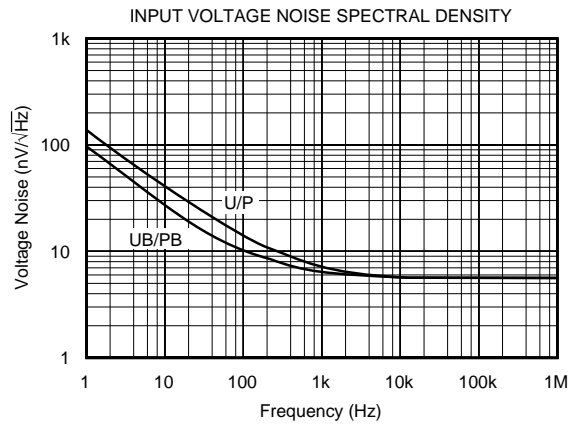
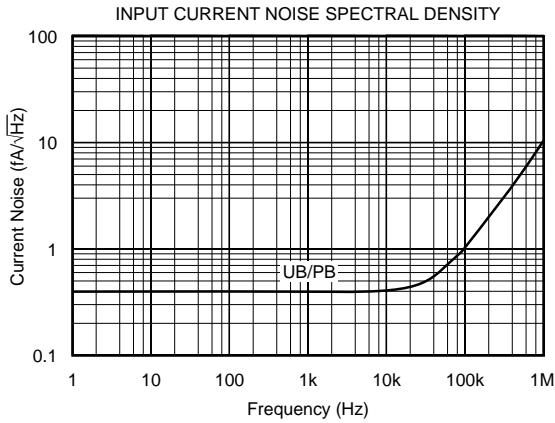
## ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE	BIAS CURRENT pA, max	OFFSET DRIFT $\mu\text{V}/^{\circ}\text{C}$ , max
OPA124U	8-PIN SOIC	-25°C TO +85°C	5	7.5
OPA124P	8-Pin Plastic DIP	-25°C to +85°C	5	7.5
OPA124UA	8-Pin SOIC	-25°C to +85°C	2	4
OPA124PA	8-Pin Plastic DIP	-25°C to +85°C	2	4
OPA124UB	8-Pin SOIC	-25°C to +85°C	1	2
OPA124PB	8-Pin Plastic DIP	-25°C to +85°C	1	2

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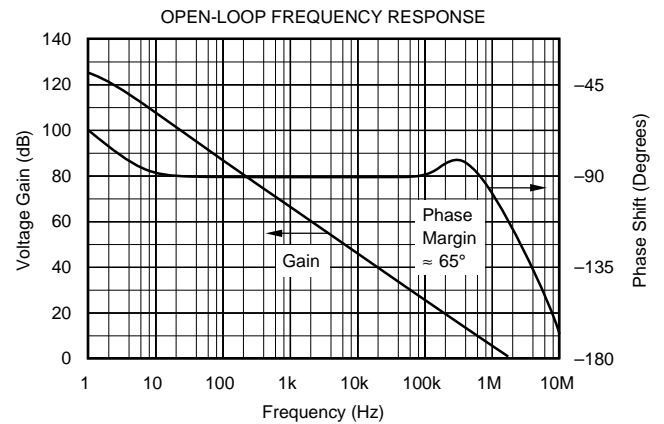
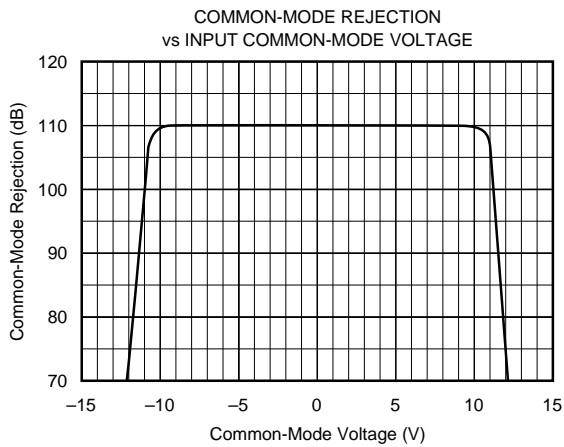
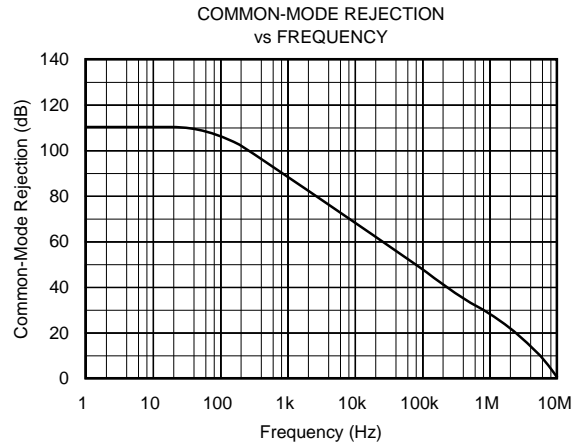
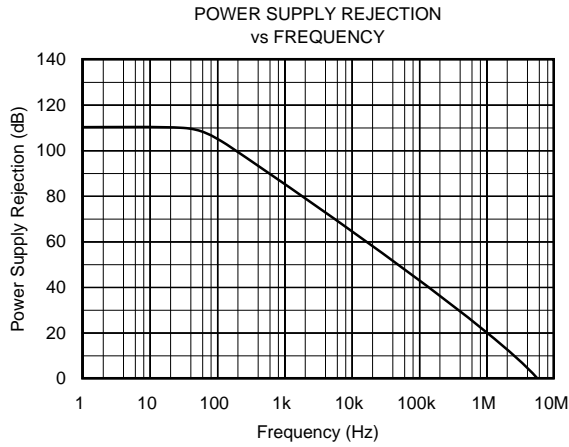
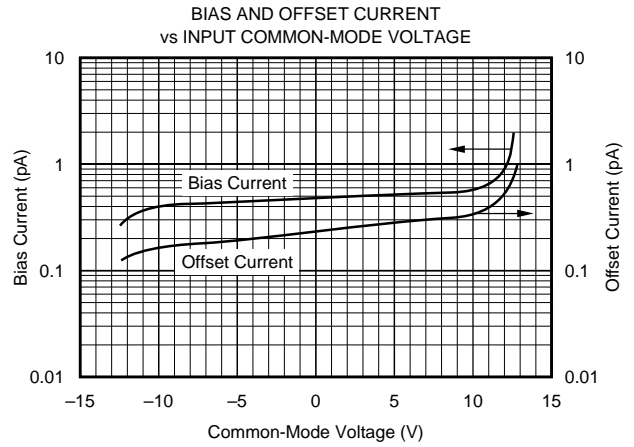
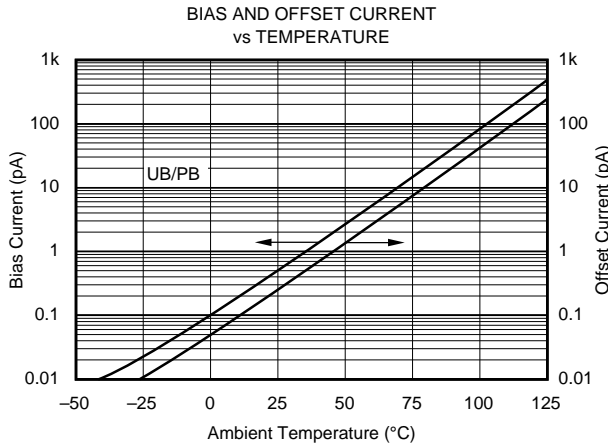
# TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{VDC}$  unless otherwise noted.



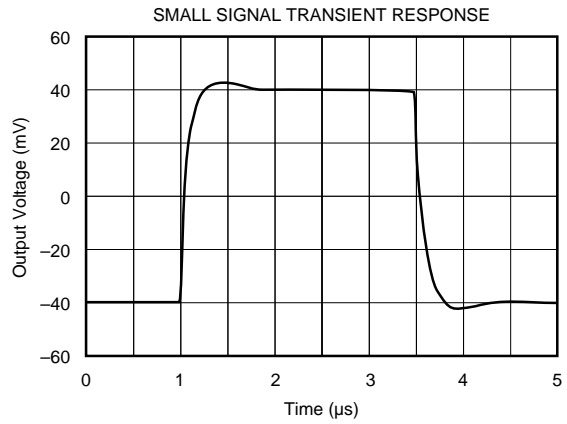
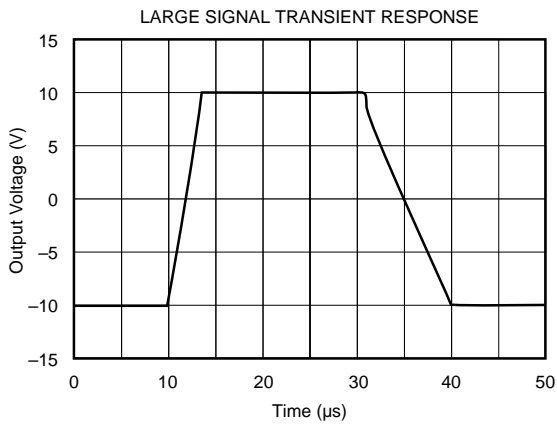
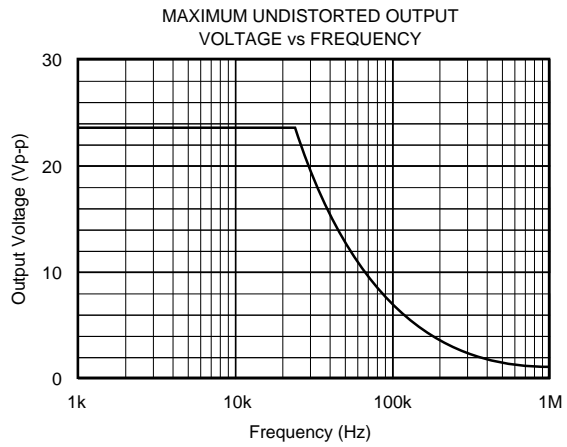
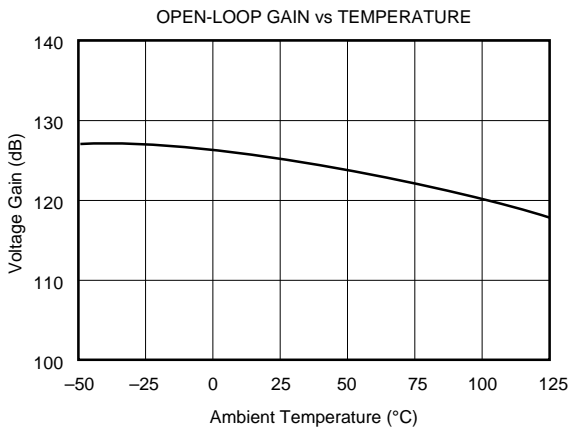
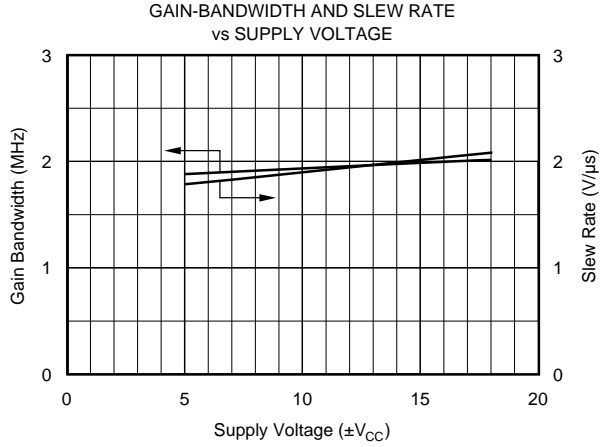
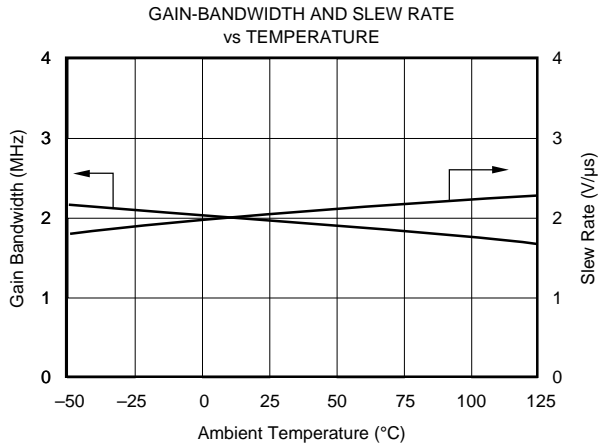
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$T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{VDC}$  unless otherwise noted.



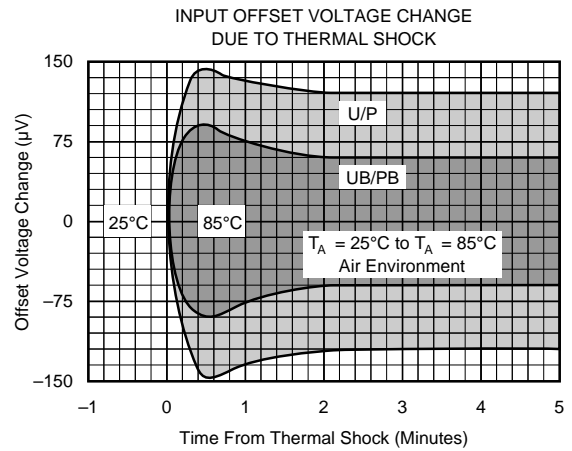
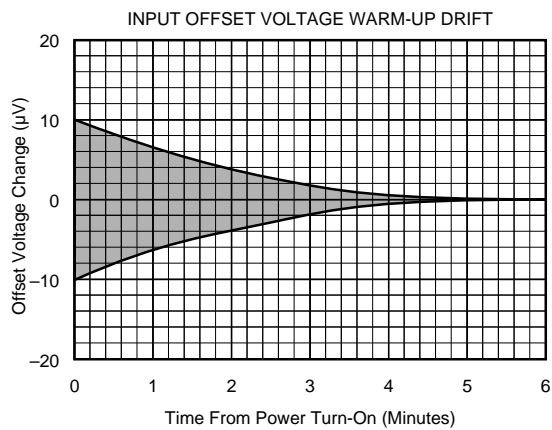
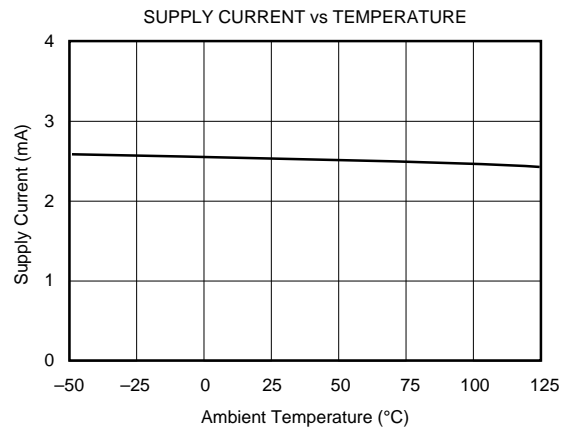
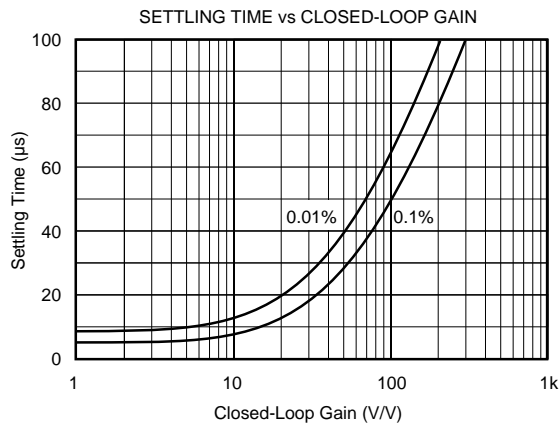
# TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{VDC}$  unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{VDC}$  unless otherwise noted.



# APPLICATIONS INFORMATION

## OFFSET VOLTAGE ADJUSTMENT

The OPA124 offset voltage is laser-trimmed and will require no further trim for most applications. In order to reduce layout leakage errors, the offset adjust capability has been removed from the SOIC versions (OPA124UB, OPA124UA, and OPA124U). The PDIP versions (OPA124PB, OPA124PA, and OPA124P) do have pins available for offset adjustment. As with most amplifiers, externally trimming the remaining offset can change drift performance by about  $0.3\mu\text{V}/^\circ\text{C}$  for each  $100\mu\text{V}$  of adjusted offset. The correct circuit configuration for offset adjust for the PDIP packages is shown in Figure 1.

## INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of  $-V_{CC}$ .

Unlike BIFET amplifiers, the *Difet* OPA124 requires input current limiting resistors only if its input voltage is greater than 6V more negative than  $-V_{CC}$ . A  $10\text{k}\Omega$  series resistor will limit input current to a safe level with up to  $\pm 15\text{V}$  input levels, even if both supply voltages are lost (Figure 2).

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

## GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA124. To avoid leakage problems, the OPA124 should be soldered directly into a printed circuit board. Utmost care must be used in planning the board layout. A “guard” pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier substrate should be connected to any input shield or guard via pin 8 minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 should be connected to ground.

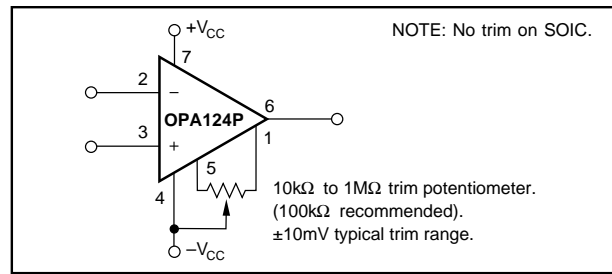


FIGURE 1. Offset Voltage Trim for PDIP packages.

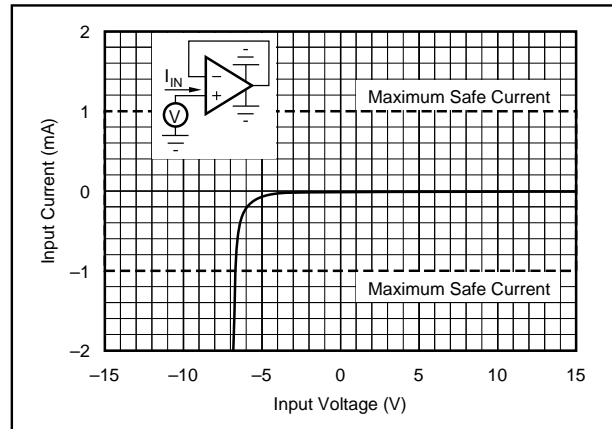


FIGURE 2. Input Current vs Input Voltage with  $\pm V_{CC}$  Pins Grounded.

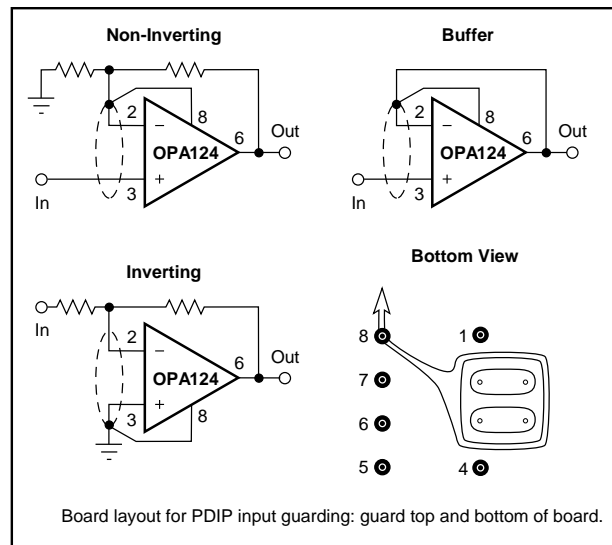
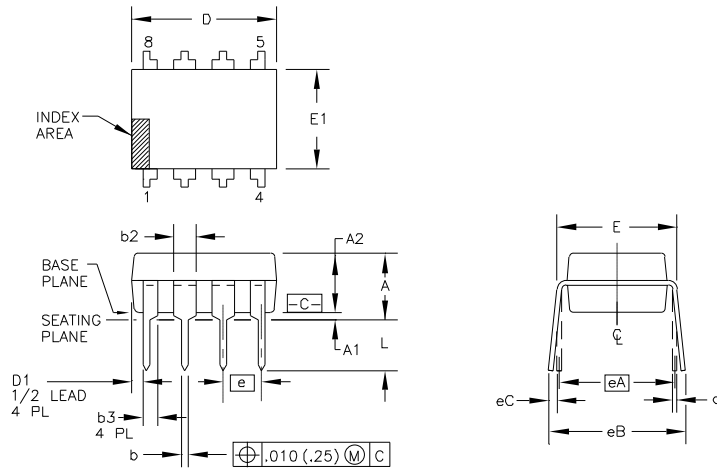


FIGURE 3. Connection of Input Guard.



# PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	9
b	.014	.022	0.36	0.56	
b2	.045	.070	1.14	1.78	9
b3	.030	.045	0.76	1.14	9
c	.008	.014	0.20	0.36	
D	.355	.400	9.02	10.16	4
D1	.005	--	0.13	--	4
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100	BASIC	2.54	BASIC	
eA	.300	BASIC	7.63	BASIC	5
eB	--	.430	--	10.92	6

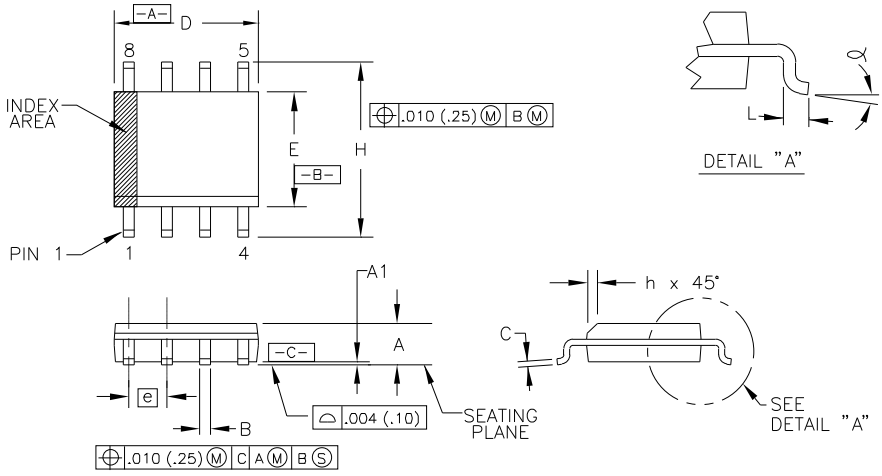
NOTES:

- ALL DIMENSIONS ARE IN INCHES.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
- D, D1, AND E1 DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
- E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM  $\overline{C-C}$ .
- eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
- N IS THE MAXIMUM OF TERMINAL POSITIONS.

- POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
- b2 AND b3 MAXIMUM DIMENSIONS DO NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED .010 (0.25mm).
- DISTANCE BETWEEN LEADS INCLUDING DAMBAR PROTRUSIONS TO BE .005 (0.13mm) MINIMUM.
- A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
- FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006      REV.: E  
JEDEC NUMBER: MS-001-BA

Package Number 182 - 8-Lead SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.0532	.0688	1.35	1.75	
A1	.004	.0098	0.10	0.23	
B	.013	.020	0.33	0.51	7
C	.0075	.0098	0.20	0.25	
D	.189	.1968	4.80	4.98	2
E	.1497	.1574	3.80	4.00	3
e	.050	BASIC	1.27	BASIC	
H	.2284	.244	5.80	6.20	
h	.0099	.0196	0.25	0.50	
L	.016	.050	0.41	1.27	5
N	8		8		6
$\alpha$	0°	8°	0°	8°	

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
- DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 IN. (0.15 mm) PER SIDE.
- DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .010 IN. (0.25 mm) PER SIDE.
- THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT,

A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.

- "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
- "N" IS THE NUMBER OF TERMINAL POSITIONS.
- THE LEAD WIDTH "B", AS MEASURED .014 IN. (0.36 mm) OR GREATER ABOVE THE SEATING PLANE, SHALL NOT EXCEED A MAXIMUM VALUE OF .024 IN. (0.61 mm).
- LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 IN. (0.10 mm) FROM SEATING PLANE.

PACKAGE NUMBER: ZZ182      REV.: G  
JEDEC NUMBER: MS-012-AA