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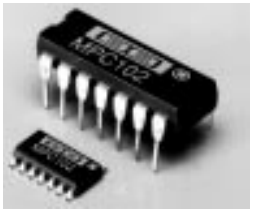


MPC102

Wide-Bandwidth DUAL 2 x 1 VIDEO MULTIPLEXER

FEATURES

- **BANDWIDTH: 210MHz (1.4Vp-p)**
- **LOW INTERCHANNEL CROSSTALK: –68dB (30MHz, SO); –58dB (30MHz, DIP)**
- **LOW SWITCHING TRANSIENTS: +6mV/–8mV**
- **LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.02%, 0.02°**
- **LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±250μA**

APPLICATIONS

- **VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)**
- **RADAR SYSTEMS**
- **DATA ACQUISITION**
- **INFORMATION TERMINALS**
- **SATELLITE OR RADIO LINK IF ROUTING**

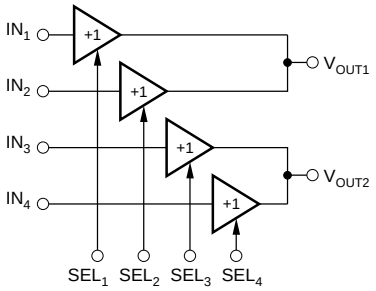
DESCRIPTION

The MPC102 is dual, wide-bandwidth, 2-to-1 channel video signal multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC102 also make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC102 consists of four identical monolithic, integrated, open-loop buffer amplifiers. Two buffer outputs are each connected internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC102 multiplexer enables the user to connect one of two input signals to the corresponding output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 210MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $4nV/\sqrt{Hz}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in a space-saving 14-pin SO and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)



TRUTH TABLE

SEL_1	SEL_2	SEL_3	SEL_4	V_{OUT1}	V_{OUT2}
0	0	0	0	HI-Z	HI-Z
1	0	0	0	IN_1	HI-Z
0	1	0	0	IN_2	HI-Z
0	0	1	0	HI-Z	IN_3
0	0	0	1	HI-Z	IN_4

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SPECIFICATIONS

ELECTRICAL

At V_{CC} = ±5V, R_L = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC102AP, AU			UNITS
		MIN	TYP	MAX	
DC CHARACTERISTICS					
INPUT OFFSET VOLTAGE	R_{IN} = 0, R_{SOURCE} = 0				
Initial			14	±30	mV
vs Temperature			60		µV/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V	–40	–74		dB
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		–50		dB
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–50		dB
Initial Matching	All Four Buffers		±3		mV
INPUT BIAS CURRENT					
Initial			4	±10	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V		±710		nA/V
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		0.26		µA/V
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		1.7		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	f_{OUT} = 20kHz to 10MHz		4.0		nV/√Hz
Signal-to-Noise Ratio	S/N = 0.7/(V_{IN} • √5MHz)		–98		dB
INPUT VOLTAGE RANGE	Gain Error = 10%		±3.6		V
TRANSFER CHARACTERISTICS					
Voltage Gain	R_L = 1kΩ, V_{IN} = ±2V		0.982		V/V
Voltage Gain	R_L = 10kΩ, V_{IN} = ±2.8V	0.98	0.992		V/V
RATED OUTPUT					
Voltage	V_{IN} = ±3V, R_L = 10kΩ	±2.8	±2.98		V
Resistance	One Channel Selected		11		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.5		pF
CHANNEL SELECTION INPUTS					
Logic 1 Voltage		+2		V_{CC}	V
Logic 0 Voltage				+0.8	V
Logic 1 Current	V_{SEL} = 5.0V		100	150	µA
Logic 0 Current	V_{SEL} = 0.8V			5	µA
SWITCHING CHARACTERISTICS	V_{IN} = –0.3V to +0.7V, f = 5MHz				
SEL to Channel ON Time	90% Point of V_{OUT} = 1Vp-p		0.25		µs
SEL to Channel OFF Time	10% Point of V_{OUT} = 1Vp-p		0.25		µs
Switching Transient, Positive	Measured While Switching		6		mV
Switching Transient, Negative	Between Two Grounded Channels		–8		mV
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected		±4.6	±5	mA
	No Channel Selected		±250	±350	µA
Rejection Ratio			–80		dB
TEMPERATURE RANGE					
Operating		–40		+85	°C
Storage		–40		+125	°C
Thermal Resistance, θ_{JA}			90		°C/W

SPECIFICATIONS—AC CHARACTERISTICS (CONT)

At V_{CC} = ±5V, R_L = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC102AP, AU			UNITS
		MIN	TYP	MAX	
LARGE SIGNAL BANDWIDTH (–3dB)	V_{OUT} = 5.0Vp-p, C_{OUT} = 1pF V_{OUT} = 2.8Vp-p, C_{OUT} = 1pF V_{OUT} = 1.4Vp-p, C_{OUT} = 1pF		55 100 210		MHz MHz MHz
SMALL SIGNAL BANDWIDTH	V_{OUT} = 0.2Vp-p, C_{OUT} = 1pF		370		MHz
GROUP DELAY TIME			450		ps
DIFFERENTIAL GAIN	f = 4.43MHz, V_{IN} = 0.3Vp-p VDC = 0 to 0.7V		0.02		%
DIFFERENTIAL PHASE	f = 4.43MHz, V_{IN} = 0.3Vp-p VDC = 0 to 0.7V		0.02		Degrees
GAIN FLATNESS PEAKING	V_{OUT} = 0.2Vp-p, DC to 30MHz V_{OUT} = 0.2Vp-p, DC to 100MHz		0.04 0.05		dB dB
HARMONIC DISTORTION Second Harmonic Third Harmonic	f = 30MHz, V_{OUT} = 1.4Vp-p, R_L = 350Ω		 –64 –66		 dBc dBc
CROSSTALK MPC102AP All Hostile Off Isolation MPC102AU All Hostile Off Isolation 	V_{IN} = 1.4Vp-p f = 5MHz, f = 30MHz, f = 5MHz, f = 30MHz, f = 5MHz, f = 30MHz, f = 5MHz, f = 30MHz		 –75 –58 –70 –71 –78 –68 –75 –76		 dB dB dB dB dB dB dB dB
TIME DOMAIN					
RISE/FALL TIME	V_{OUT} = 1.4Vp-p, Step 10% to 90% C_{OUT} = 1pF, R_{OUT} = 22Ω		2.5		ns
SLEW RATE	V_{OUT} = 1.4Vp-p C_{OUT} = 1pF C_{OUT} = 22pF C_{OUT} = 47pF		 500 360 260		 V/µs V/µs V/µs

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	±6V
Analog Input Voltage (IN_1 through IN_4)	$\pm V_{CC}$, ±0.7V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Output Current	±6mA
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (SEL_1 through SEL_4)	–0.5V to $+V_{CC}$ +0.7V
Logic Voltage Input	–0.6V to $+V_{CC}$ +0.6V

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
MPC102AP	14-Pin Plastic DIP	–40°C to +85°C
MPC102AU	14-Pin SOIC	–40°C to +85°C

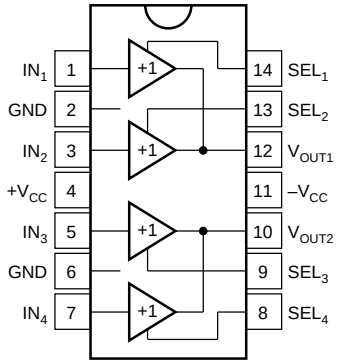
PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
MPC102AP	14-Pin DIP	010
MPC102AU	14-Pin SOIC	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

CONNECTION DIAGRAM

Top View **SO/DIP**

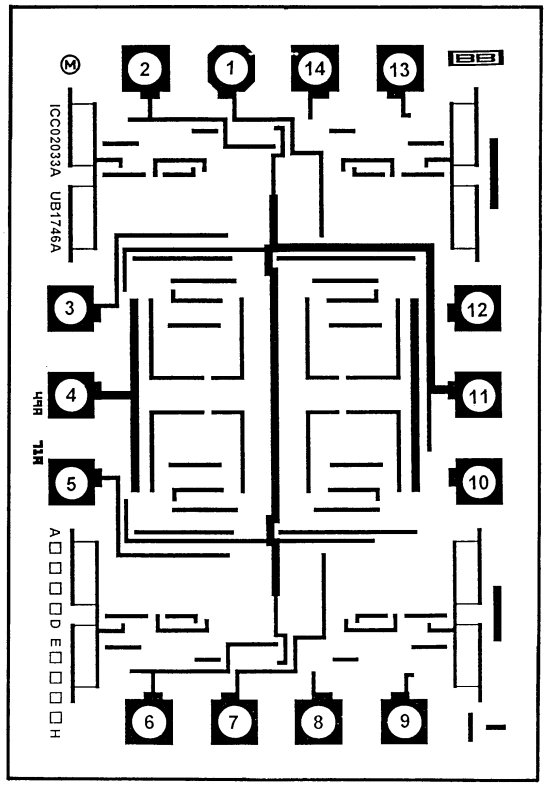


MPC102

PIN DESCRIPTION

PIN	DESCRIPTION
IN_1, IN_2	Analog Inputs Channel 1 and 2
IN_3, IN_4	Analog Inputs Channel 3 and 4
GND	Analog Shielding Grounds, Connect to System Ground
SEL_1, SEL_2	Channel Selection Inputs
V_{OUT1}	Analog Output 1
V_{OUT2}	Analog Output 2
$-V_{CC}$	Negative Supply Voltage; typical –5VDC
$+V_{CC}$	Positive Supply Voltage; typical +5VDC

DICE INFORMATION



MPC102AD DIE TOPOGRAPHY

PAD	FUNCTION
1	Input 1
2	Ground
3	Input 2
4	+5V Supply
5	Input 3
6	Ground
7	Input 4
8	Select 4
9	Select 3
10	Output 2
11	–5V Supply
12	Output 1
13	Select 2
14	Select 1

Substrate Bias: Negative Supply.
NC: No Connection.
Wire Bonding: Gold wire bonding is recommended.

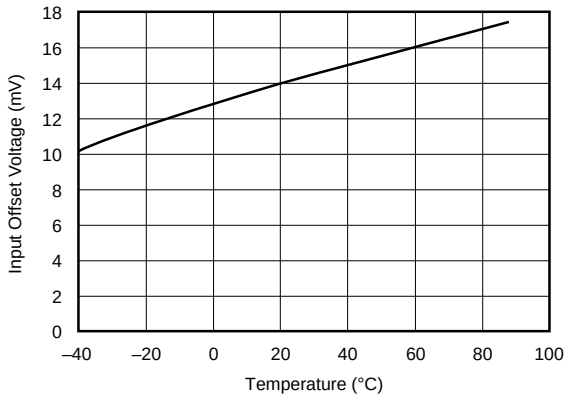
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	51 x 76 ±5	1.295 x 1.93 ±0.13
Die Thickness	14 ±1	0.55 ±0.025
Min. Pad Size	4 x 4	0.10 x 0.10
Backing: Titanium	0.02, +0.05, –0.0	0.0005, +0.0013, –0.0
Gold	0.30, ±0.05	0.0076, ±0.0013

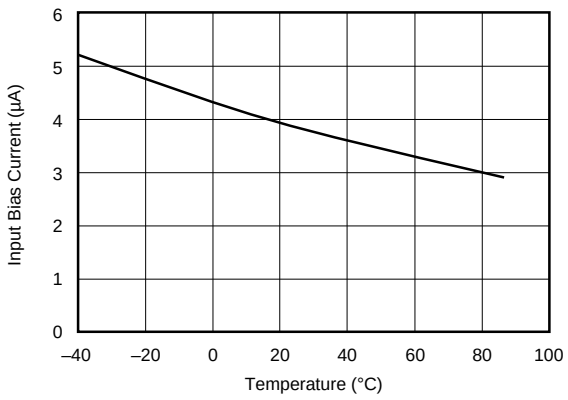
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

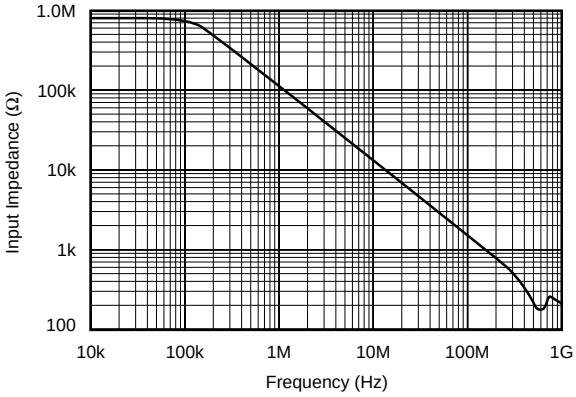
INPUT OFFSET VOLTAGE vs TEMPERATURE



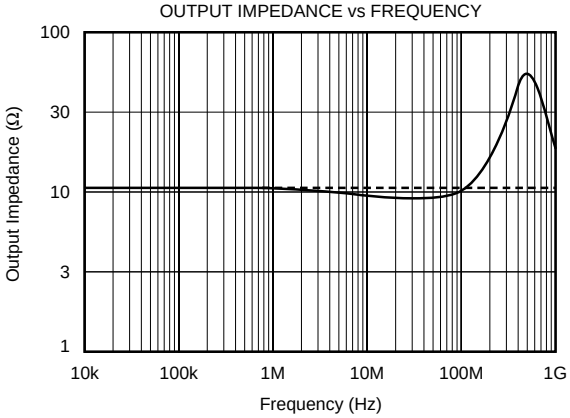
INPUT BIAS CURRENT vs TEMPERATURE



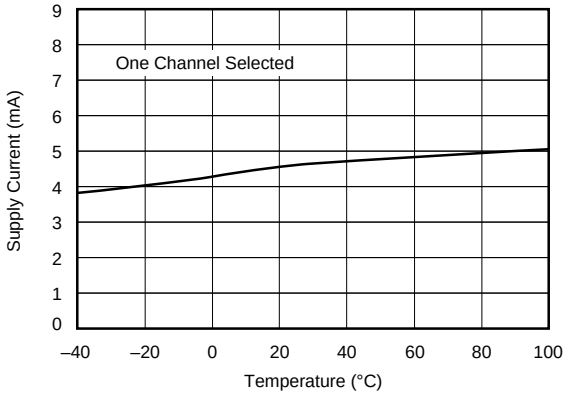
INPUT IMPEDANCE vs FREQUENCY



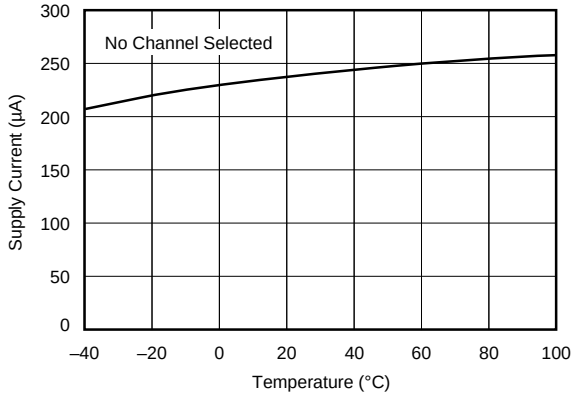
OUTPUT IMPEDANCE vs FREQUENCY



QUIESCENT CURRENT vs TEMPERATURE



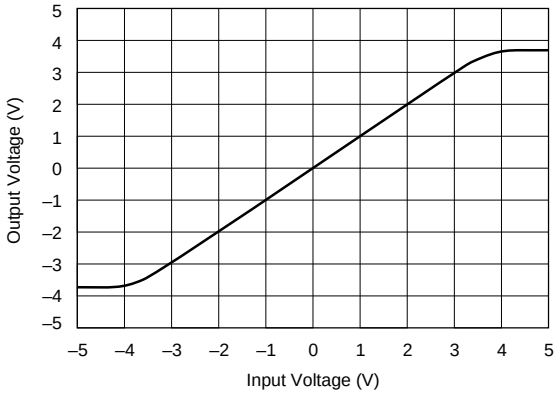
QUIESCENT CURRENT vs TEMPERATURE



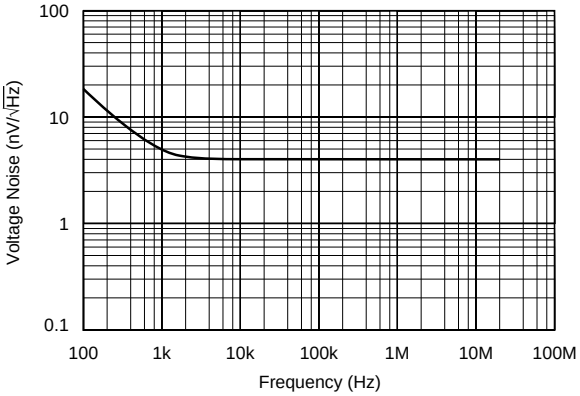
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

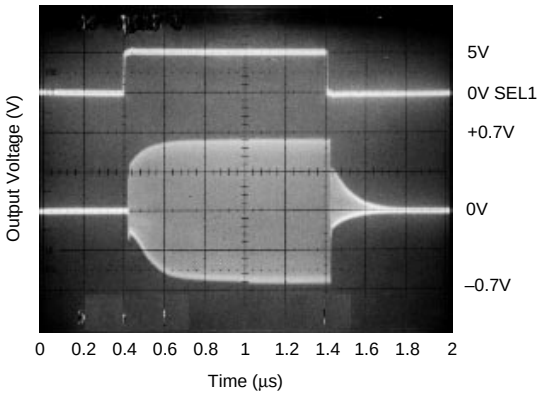
TRANSFER FUNCTION



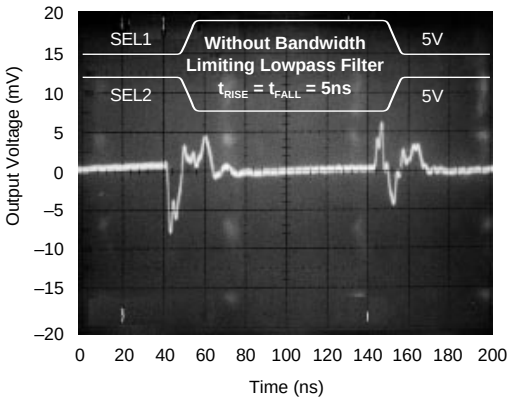
INPUT VOLTAGE NOISE SPECTRAL DENSITY

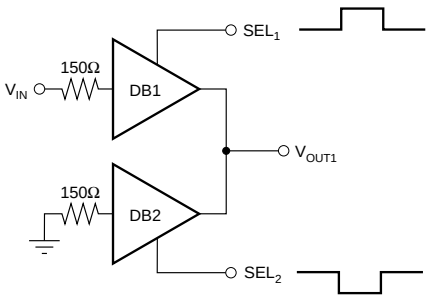


SWITCHING ENVELOPE
(Channel-to-Channel Switching)

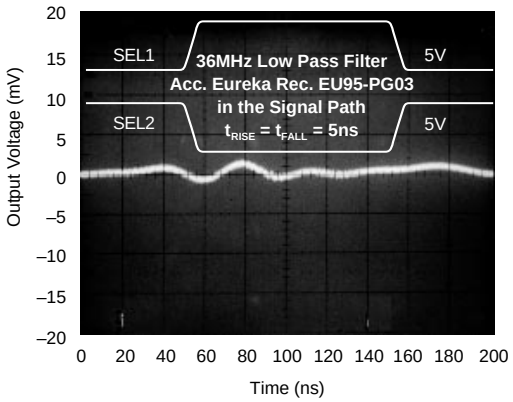


SWITCHING TRANSIENTS
(Channel-to-Channel)

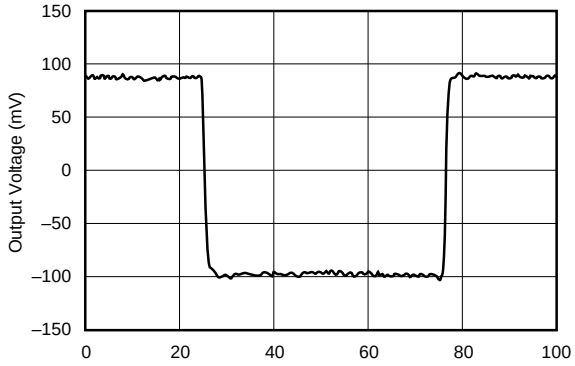




SWITCHING TRANSIENTS
(Channel-to-Channel)



SMALL SIGNAL PULSE RESPONSE

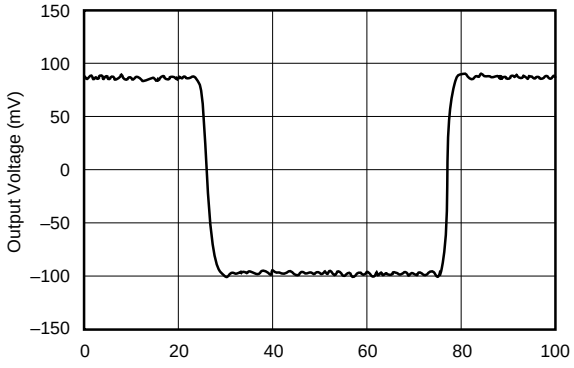


C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 2ns
(Generator), V_{IN} = 0.2Vp-p

TYPICAL PERFORMANCE CURVES (CONT)

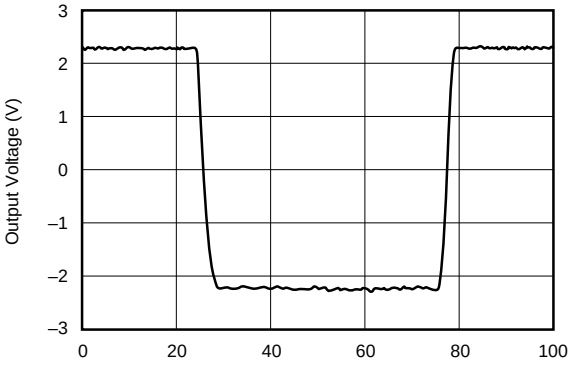
At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

SMALL SIGNAL PULSE RESPONSE



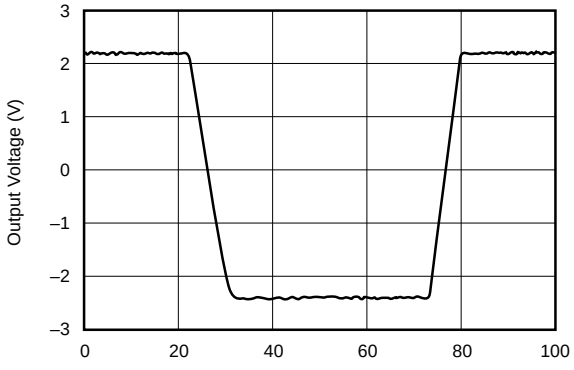
C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 2ns
(Generator), V_{IN} = 0.2Vp-p

LARGE SIGNAL PULSE RESPONSE



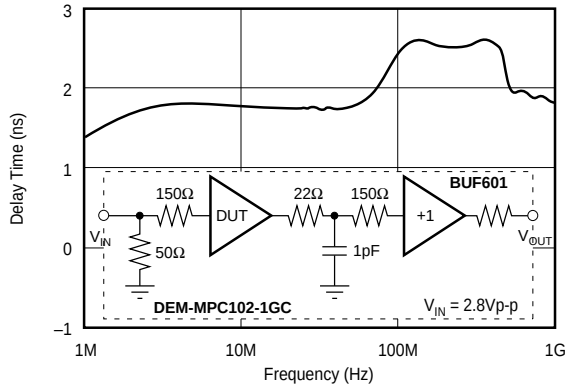
C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 5ns
(Generator), V_{IN} = 5Vp-p

LARGE SIGNAL PULSE RESPONSE

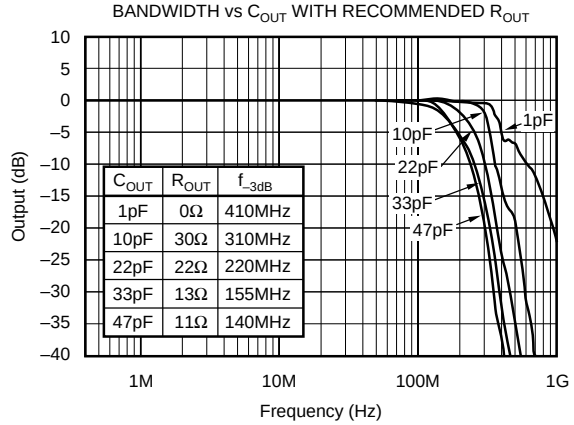


C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 5ns
(Generator), V_{IN} = 5Vp-p

GROUP DELAY TIME vs FREQUENCY

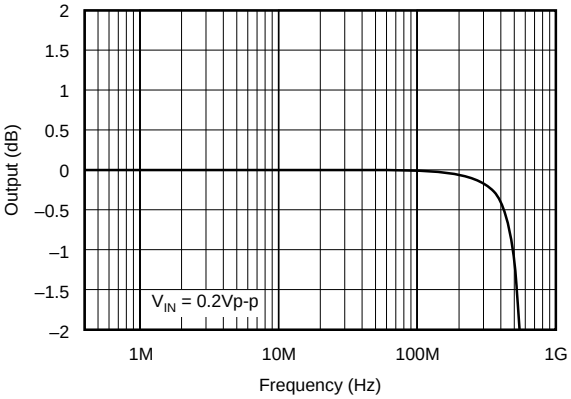


BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}



C_{OUT}	R_{OUT}	f_{-3dB}
1pF	0Ω	410MHz
10pF	30Ω	310MHz
22pF	22Ω	220MHz
33pF	13Ω	155MHz
47pF	11Ω	140MHz

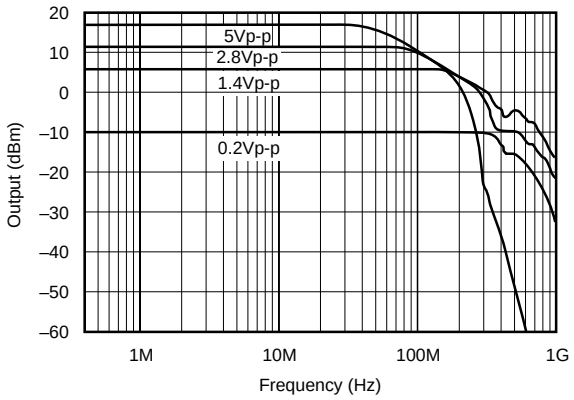
GAIN FLATNESS



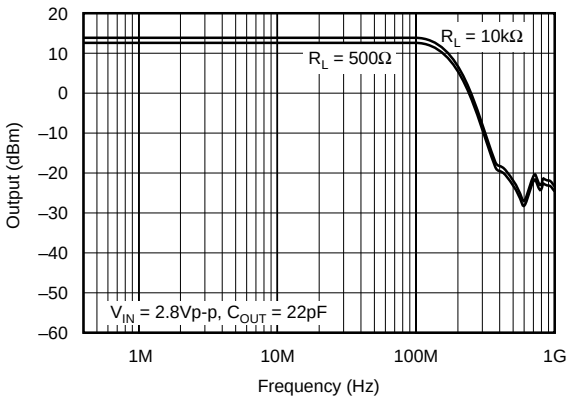
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{IN} = 150Ω, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

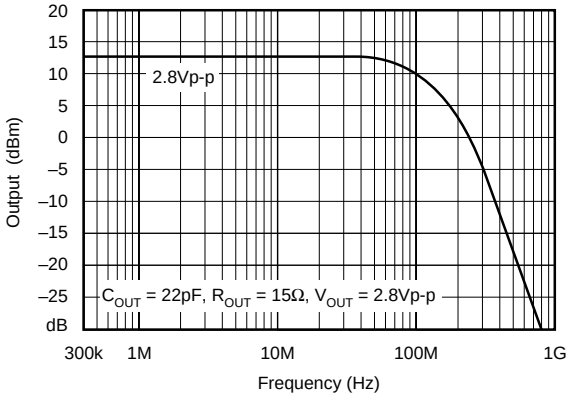
BANDWIDTH vs OUTPUT VOLTAGE



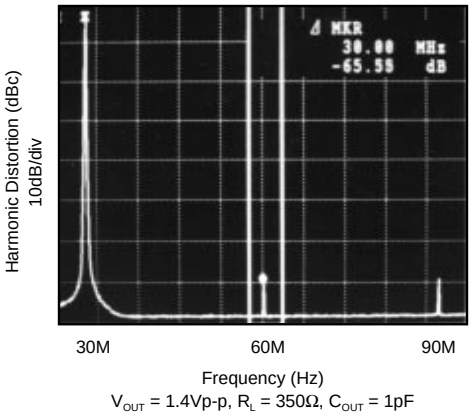
BANDWIDTH vs R_{LOAD}



BANDWIDTH MATCHING (DB1...DB4)

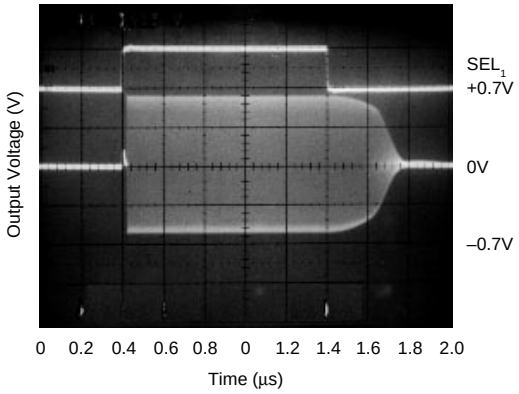


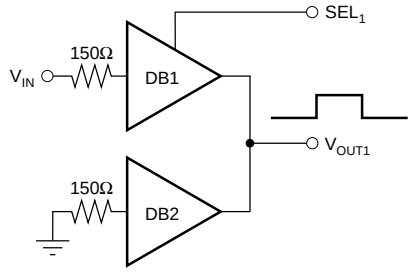
30MHz HARMONIC DISTORTION



V_{OUT} = 1.4Vp-p, R_L = 350Ω, C_{OUT} = 1pF

ON/OFF CHARACTERISTIC





APPLICATIONS INFORMATION

The MPC102 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

As shown below, all pins on the MPC102 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the characteristics of the buffer amplifier input without necessarily destroying the device. In precision buffer amplifiers, such damage may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC102.

Static damage has been well-recognized as a problem for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC102 incorporates on-chip ESD protection diodes as shown in Figure 1. Thus the user does not need to add external protection diodes, which can add capacitance and degrade AC performance.

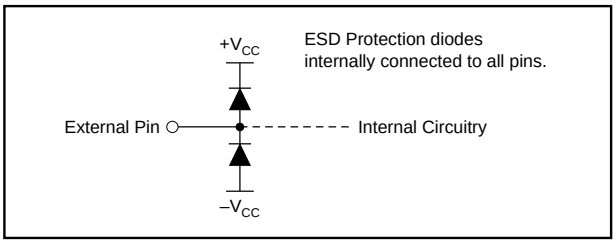


FIGURE 1. Internal ESD Protection.

DISCUSSION OF PERFORMANCE

The MPC102 is a dual, 2 x 1, wide-band analog signal multiplexer. It allows the user to connect one of the two inputs (IN_1/IN_2 or IN_3/IN_4) to the corresponding output. The switching speed between two input channels is typically less than 300ns.

However, in contrast to signal switches using CMOS or DMOS transistors, the switching transients are very low at +6mV and –8mV. The MPC102 consists of four identical unity-gain buffer amplifiers. Two of the four amplifiers are connected together internally at the output. The open-loop buffer amps, which consist of complementary emitter followers, apply no feedback so their low-frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements, the bipolar complementary buffers form a unidirectional transmission path, thus providing high output-to-input isolation. Switching stages compatible to TTL-level digital signals are provided for each buffer to select the input channel. When no channel is selected, the outputs of the device are high-impedance. This allows the user to wire several MPC102s together to create multichannel switch matrices.

Chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases bus-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the multiplexer, in effect, a quad switchable high-speed buffer. The buffers require DC coupling and termination resistors when driven directly from a low-impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated, high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. Bandwidth of over 210MHz at an output voltage of 1.4Vp-p allows the design of multi-channel crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz. The buffer amplifiers also offer low differential gain (0.02%) and phase (0.02°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the luminance signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity and does not vary with power supply voltage variations. The low output capacitance of 1.5pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC102 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to another causes the signal to mix at the output for a short time, but it interferes minimally with the input signals. The transient peaks remain less than +6mV and –8mV. The generated output transients are extremely small, so DC

clamping during switching between channels is unnecessary. DC clamping during the switching dead time is required to avoid synchronization by large negative output glitches in subsequent equipment.

The SEL-to-channel-ON time is typically 25ns and is always shorter than the typical SEL-to-channel-OFF time of 250ns. In the worst case, an ON/OFF margin of 150ns ensures safe switching even for timing spreads in the digital control latches. The short interchannel switching time of 300ns allows channel change during the vertical blanking time, even in high-resolution graphic or broadcast systems. As shown in the typical performance curves, the signal envelope during transition from one channel to another rises and falls symmetrically and shows less overshooting and DC settling effects.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Since most of the buffer amplifiers are in the off-state, one important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of ±250µA when no channel is selected and ±4.6mA when one channel is selected, as well as the reduced ±5V supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC102 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for signal and power lines should be wide to reduce impedance.
- Make short and low inductance traces. The entire circuit layout should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets are required, use zero-profile solderless sockets.
- Use low-inductance and surface-mounted components for best ac-performance.
- A resistor (100Ω to 200Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential.

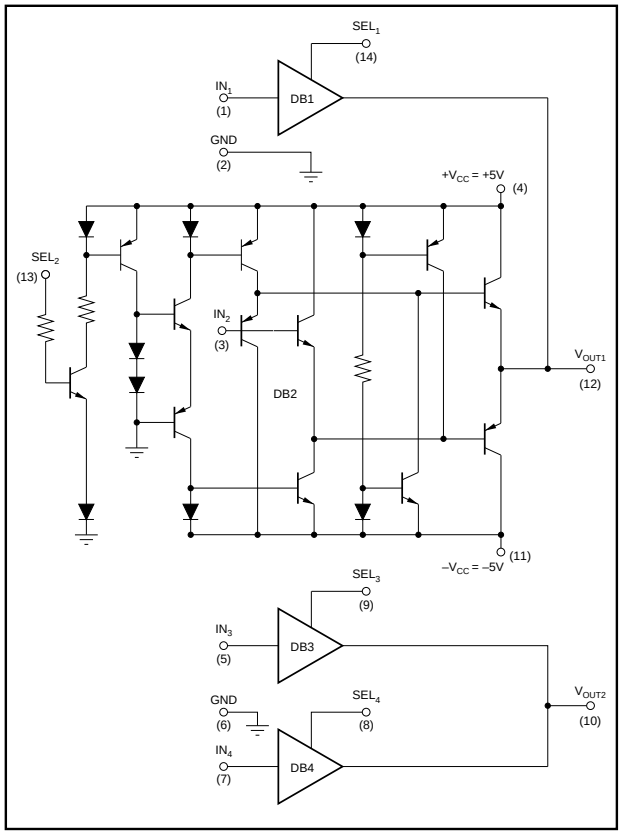


FIGURE 2. Simplified Circuit Diagram.

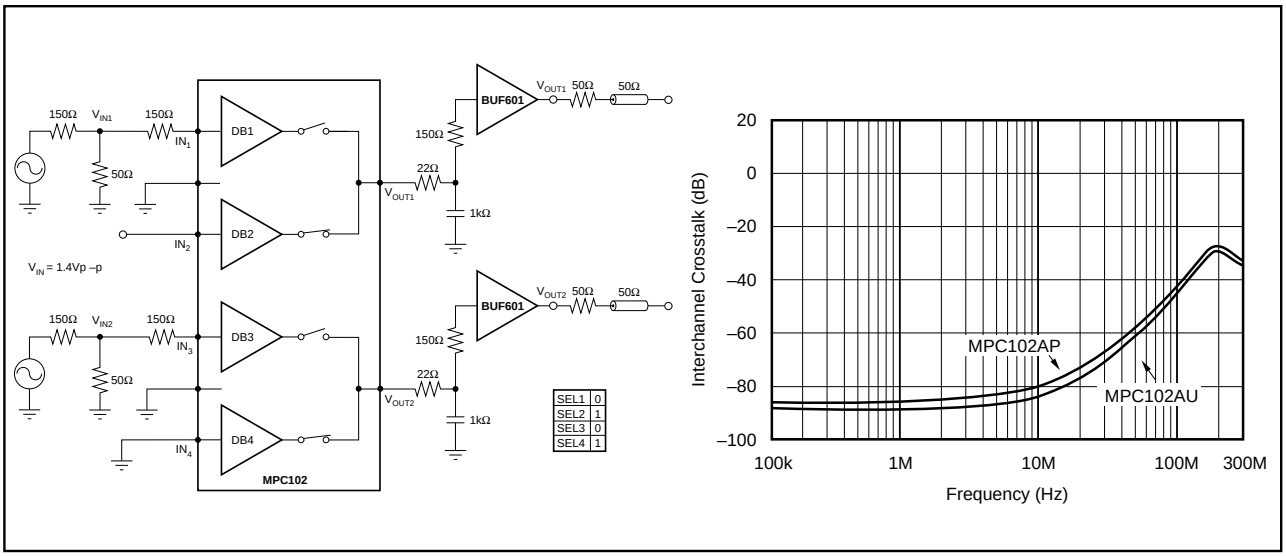


FIGURE 3. All Hostile Crosstalk – Grounded Input.

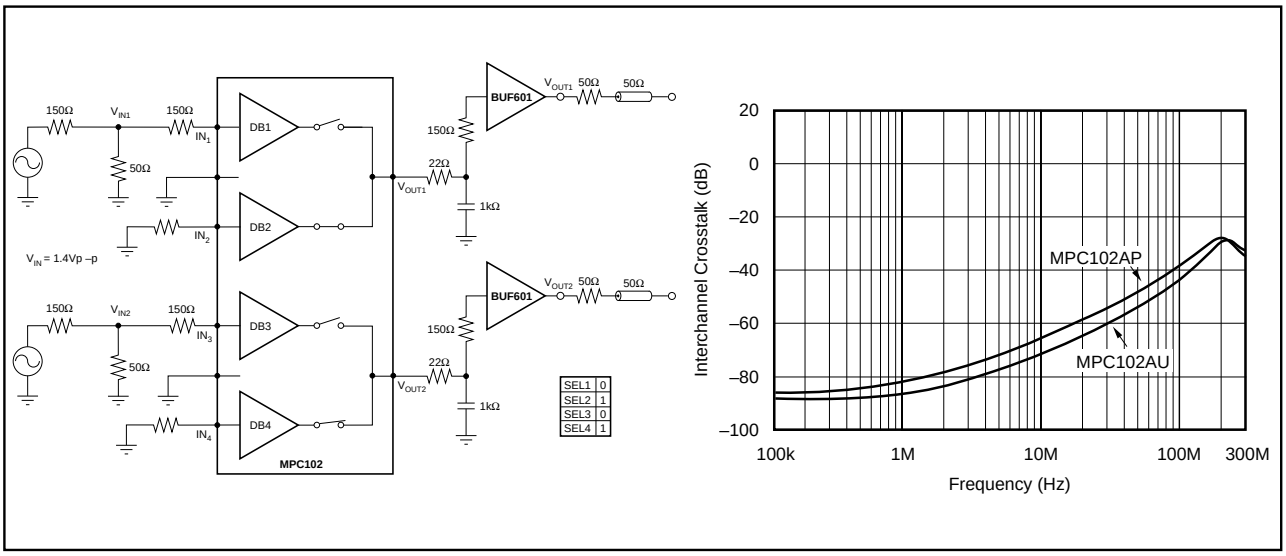


FIGURE 4. Off Isolation Crosstalk 150Ω Input.

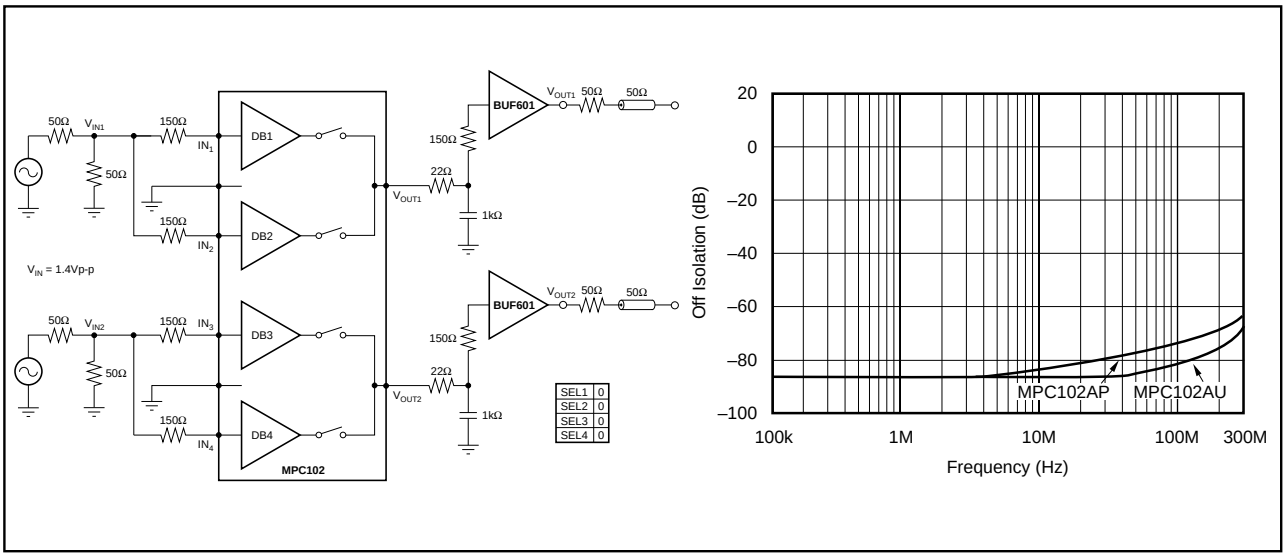
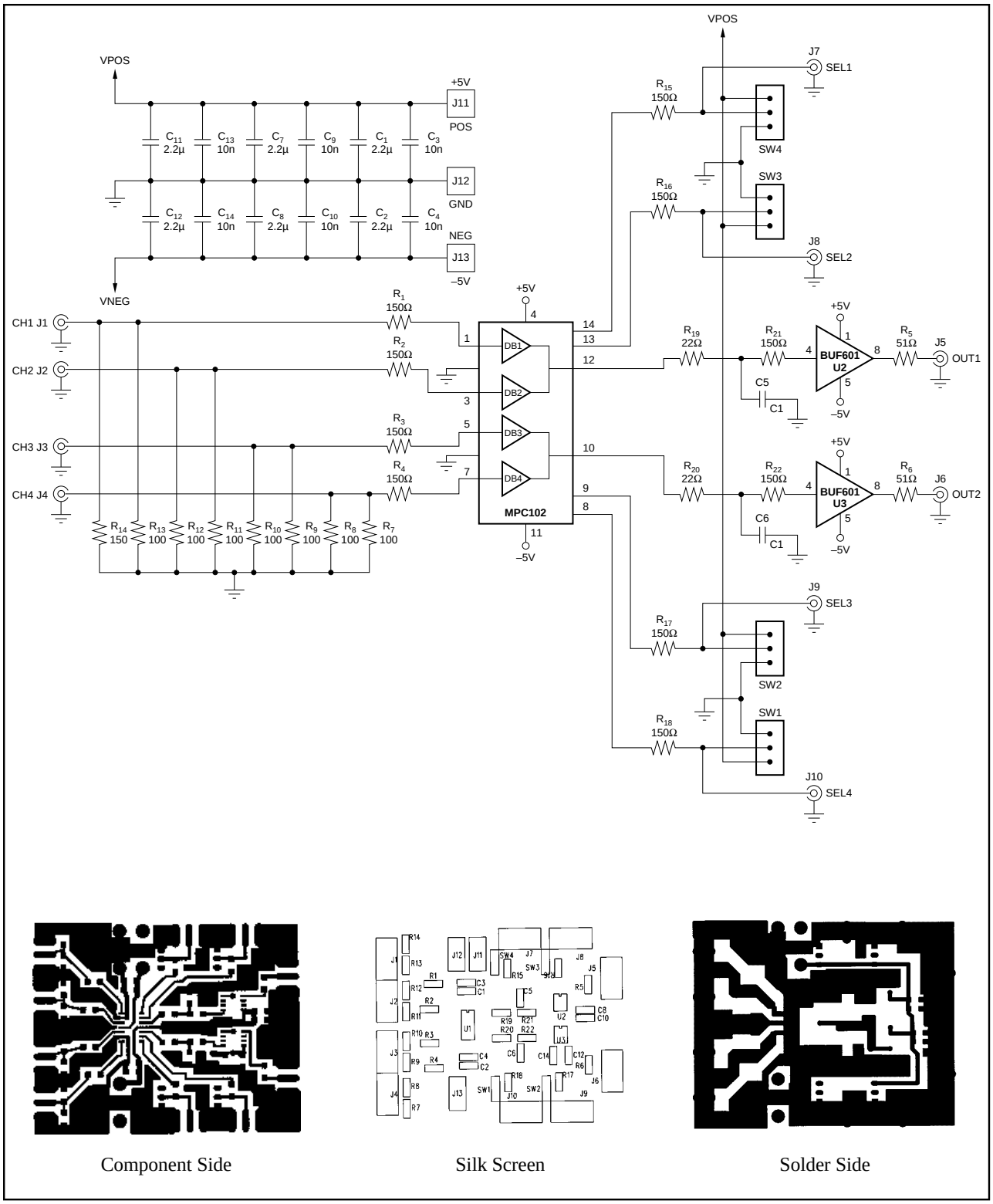


FIGURE 5. Off Isolation Crosstalk Test Circuit 2.



Component Side Silk Screen Solder Side

FIGURE 7. Test Circuit and Board Layout.

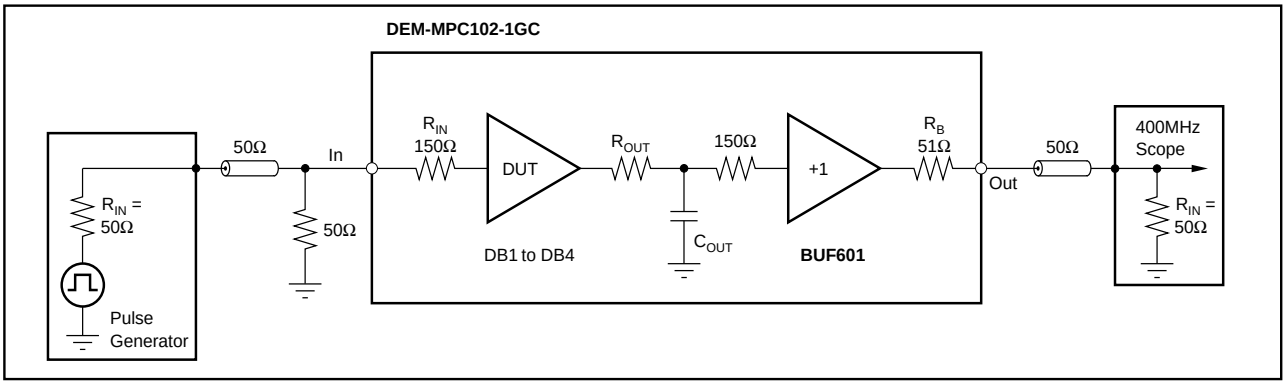


FIGURE 8. Test Circuit Pulse Response.

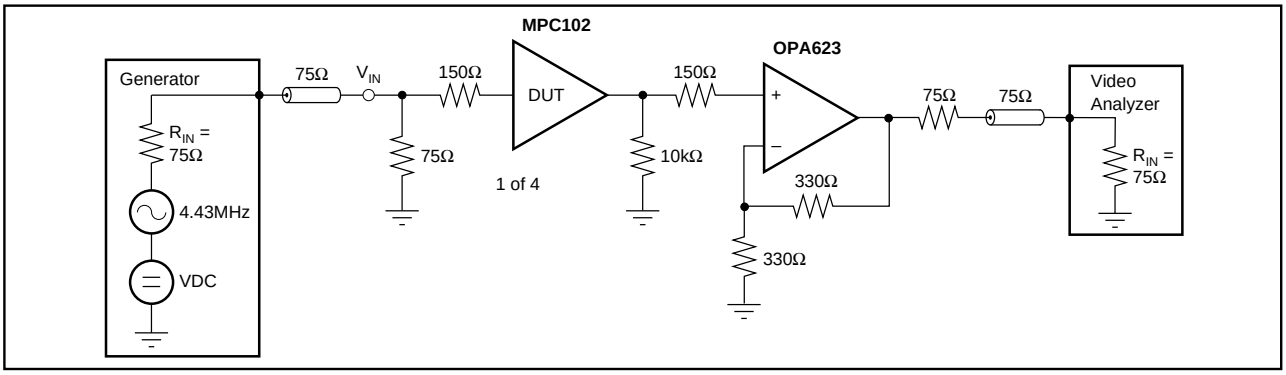


FIGURE 9. Test Circuit Differential Gain and Phase.

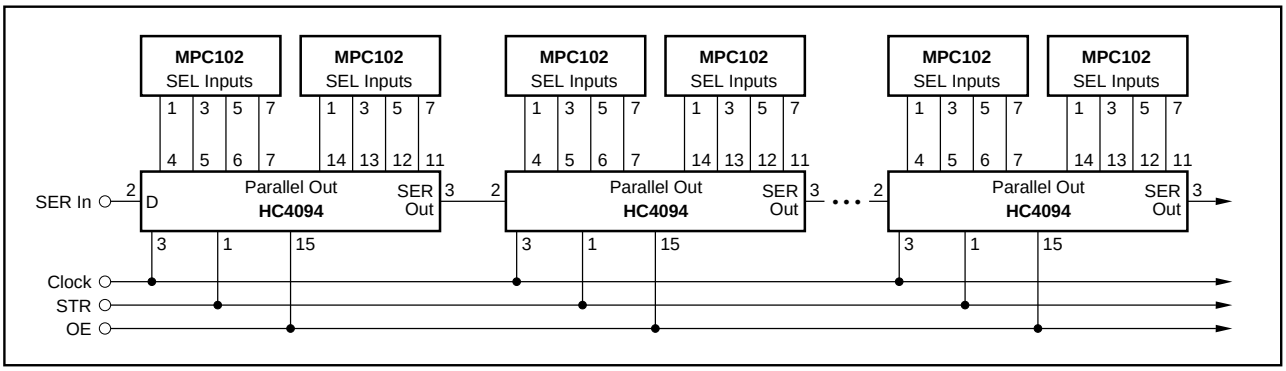
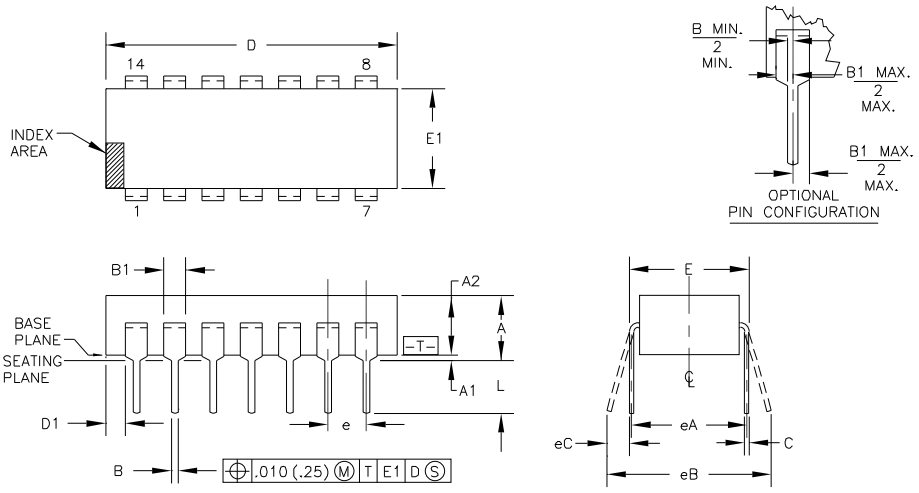


FIGURE 10. Serial Bus-Controlled Distribution Field.

PACKAGE DRAWINGS

Package Number 010 - 14-Pin Plastic, Single-Wide DIP



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
B	.014	.022	0.36	0.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	0.20	0.38	
D	.725	.795	18.42	20.19	4
D1	.005	--	0.13	--	
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
L	.115	.160	2.92	4.06	3

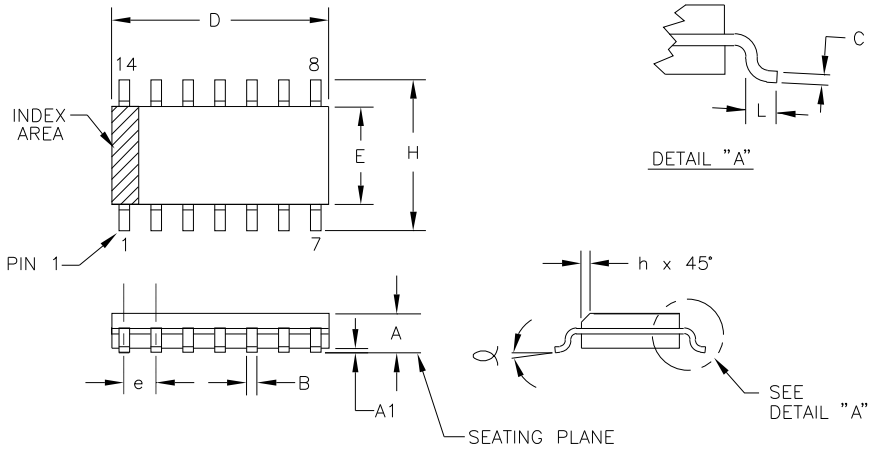
DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
N	14		14		7

NOTES:

1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 7, 8, AND 14) MAY BE CONFIGURED AS SHOWN IN THE OPTIONAL PIN CONFIGURATION.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ010	REV.: F
JEDEC NUMBER: MS-001	

Package Number 235 - 14-Lead SOIC



DIM	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	.054	.068	1.37	1.73	
A1	.004	.009	0.10	0.23	
B	.014	.019	0.36	0.48	
C	.008	.0098	0.20	0.25	
D	.337	.344	8.56	8.74	2
E	.150	.157	3.81	3.99	2
e	.050 BASIC		1.27 BASIC		
H	.229	.244	5.82	6.20	
h	.010	.019	0.25	0.48	3
L	.016	.050	0.41	1.27	4
N	14		14		5
∝	0°	8°	0°	8°	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.006 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

PACKAGE NUMBER: ZZ235	REV.: C
JEDEC NUMBER: MS-012	