

# Master-Slave Flip-Flop

Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Power Dissipation = 220 mW typ (No Load)

$f_{Tog}$  = 350 MHz typ

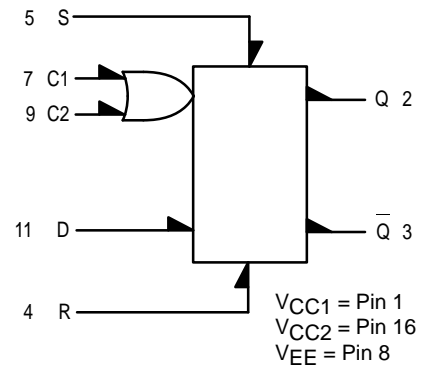


**TRUTH TABLE**

R	S	D	C	$Q_{n+1}$
L	H	X	X	H
H	L	X	X	L
H	H	X	X	N.D.
L	L	L	L	$Q_n$
L	L	L	H	L
L	L	L	L	$Q_n$
L	L	H	L	$Q_n$
L	L	H	H	H
L	L	H	L	$Q_n$

ND = Not Defined  
C = C1 + C2

**LOGIC DIAGRAM**



**ELECTRICAL CHARACTERISTICS**

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	$I_E$	—	—	—	48	—	—	mAdc
Input Current Set, Reset Clock Data	$I_{inH}$	—	—	—	550	—	—	$\mu$ Adc
Switching Times								ns
Propagation Delay	$t_{pd}$	1.0	2.7	1.1	2.5	1.1	2.9	
Rise Time (10% to 90%)	$t^+$	0.9	2.7	1.0	2.5	1.0	2.9	ns
Fall Time (10% to 90%)	$t^-$	0.5	2.1	0.6	1.9	0.6	2.3	ns
Setup Time	$t_{S"1"}$ $t_{S"0"}$	—	—	0.4	—	—	—	ns
Hold Time	$t_{H"1"}$ $t_{H"0"}$	—	—	0.3	—	—	—	ns
Toggle Frequency	$f_{Tog}$	270	—	300	—	270	—	MHz

**PIN ASSIGNMENT**

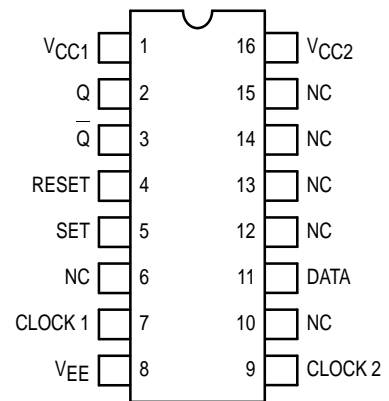
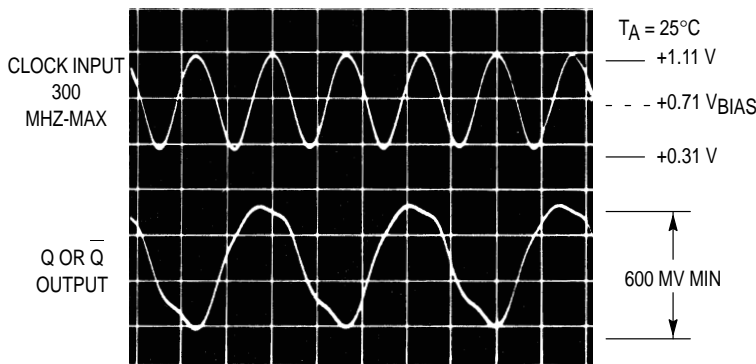


FIGURE 1 — TOGGLE FREQUENCY WAVEFORMS



The maximum toggle frequency of the MC1670 has been exceeded when either:

1. The output peak-to-peak voltage swing falls below 600 millivolts, OR
2. The device ceases to toggle (divide by two).

FIGURE 2 — MAXIMUM TOGGLE FREQUENCY (TYPICAL)

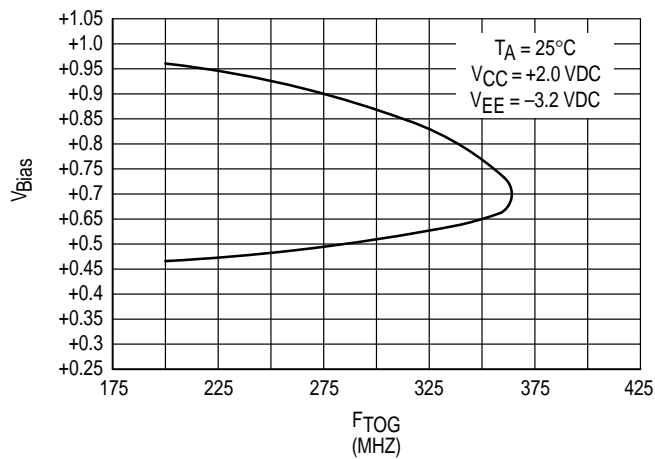
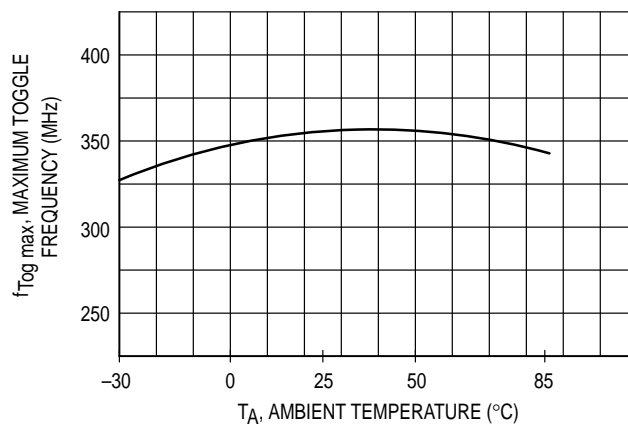


Figure 2 illustrates the variation in toggle frequency with the dc offset voltage ( $V_{Bias}$ ) of the input clock signal. Figures 4 and 5 illustrate minimum clock pulse width recommended for reliable operation of the MC1670.

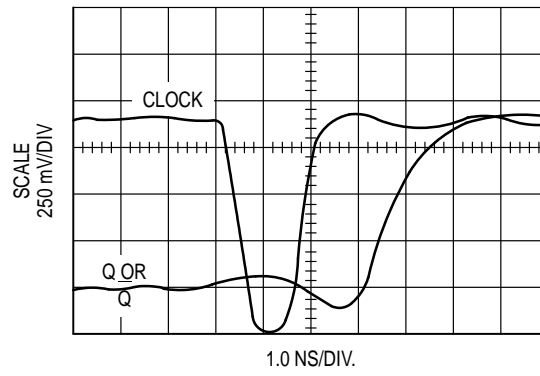
FIGURE 3 — TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



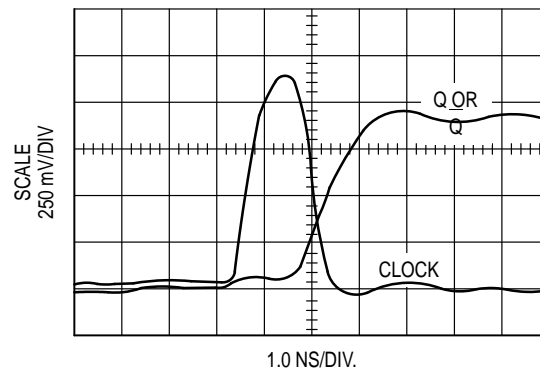
Temperature	-30°C	+25°C	+85°C
$V_{Bias}$	+0.66 Vdc	+0.71 Vdc	+0.765 Vdc

Note: All power supply and logic levels are shown shifted 2.0 volts positive.

**FIGURE 4 — MINIMUM “DOWN TIME” TO CLOCK  
OUTPUT LOAD = 50 Ω**

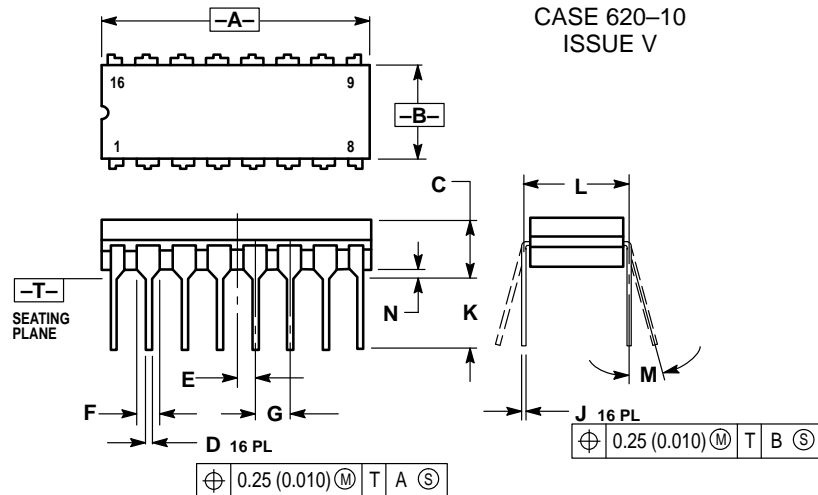


**FIGURE 5 — MINIMUM “UP TIME” TO CLOCK  
OUTPUT LOAD = 50 Ω**



OUTLINE DIMENSIONS

L SUFFIX  
CERAMIC DIP PACKAGE  
CASE 620-10  
ISSUE V



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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