

**MC14569B**

**Programmable Divide-By-N  
Dual 4-Bit Binary/BCD  
Down Counter**

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14568B, MC14522B or MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning

**MAXIMUM RATINGS\*** (Voltages Referenced to V<sub>SS</sub>)

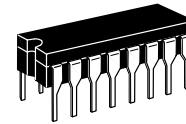
Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	- 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
P <sub>D</sub>	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

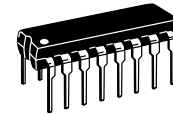
† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



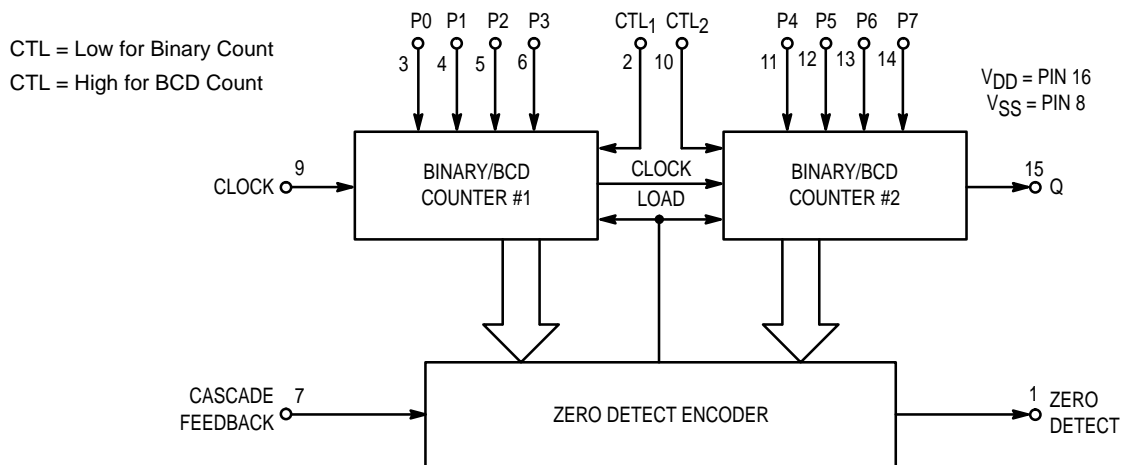
**DW SUFFIX**  
SOIC  
CASE 751G

**ORDERING INFORMATION**

MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBDW SOIC

T<sub>A</sub> = - 55° to 125°C for all packages.

**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ #	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
15		—	0.05	—	0	0.05	—	0.05			
V <sub>in</sub> = 0 or V <sub>DD</sub>	V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc	
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc	
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
			5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—	
			10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—	
			15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—	
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink	I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
			10	1.6	—	1.3	2.25	—	0.9	—	
			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.58 μA/kHz) f + I <sub>DD</sub>							μAdc	
10	I <sub>T</sub> = (1.20 μA/kHz) f + I <sub>DD</sub>										
15	I <sub>T</sub> = (1.95 μA/kHz) f + I <sub>DD</sub>										

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

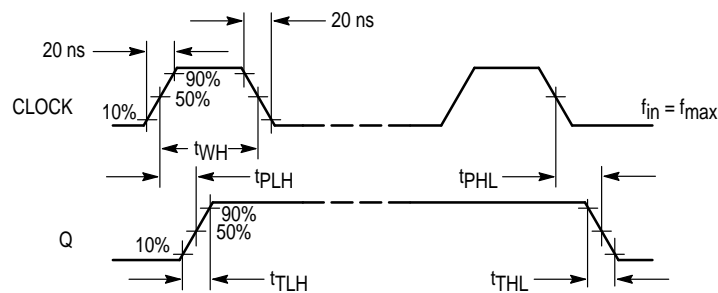
**This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.**

**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

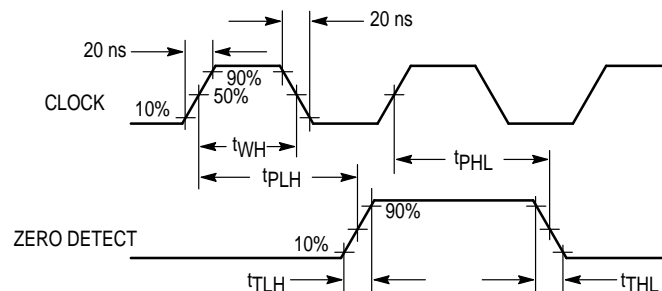
Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit	
			Min	Typ #	Max		
Output Rise Time	$t_{TLH}$	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Output Fall Time	$t_{THL}$	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Turn-On Delay Time Zero Detect Output	$t_{PLH}$	5.0	—	420	700	ns	
		10	—	175	300		
		15	—	125	250		
	Q Output	$t_{PLH}$	5.0	—	675	1200	ns
			10	—	285	500	
			15	—	200	400	
Turn-Off Delay Time Zero Detect Output	$t_{PHL}$	5.0	—	380	600	ns	
		10	—	150	300		
		15	—	100	200		
	Q Output	$t_{PHL}$	5.0	—	530	1000	ns
			10	—	225	400	
			15	—	155	300	
Clock Pulse Width	$t_{WH}$	5.0	300	100	—	ns	
		10	150	45	—		
		15	115	30	—		
Clock Pulse Frequency	$f_{cl}$	5.0	—	3.5	2.1	MHz	
		10	—	9.5	5.1		
		15	—	13.0	7.8		
Clock Pulse Rise and Fall Time	$t_{TLH}, t_{THL}$	5.0	NO LIMIT			$\mu\text{s}$	
		10					
		15					

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**SWITCHING WAVEFORMS**



**Figure 1.**



**Figure 2.**

## PIN DESCRIPTIONS

### INPUTS

**P0, P1, P2, P3 (Pins 3, 4, 5, 6)** — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

**P4, P5, P6, P7 (Pins 11, 12, 13, 14)** — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

**Clock (Pin 9)** — Preset data is decremented by one on each positive transition of this signal.

### OUTPUTS

**Zero Detect (Pin 1)** — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

**Q (Pin 15)** — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

### CONTROLS

**Cascade Feedback (Pin 7)** — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are “don't cares.” Refer to Table 1 for output characteristics.

**CTL<sub>1</sub> (Pin 2)** — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

**CTL<sub>2</sub> (Pin 10)** — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

### SUPPLY PINS

**V<sub>SS</sub> (Pin 18)** — Negative Supply Voltage. This pin is usually connected to ground.

**V<sub>DD</sub> (Pin 16)** — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

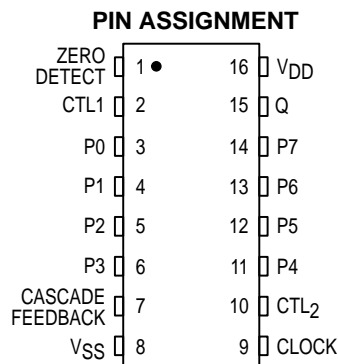
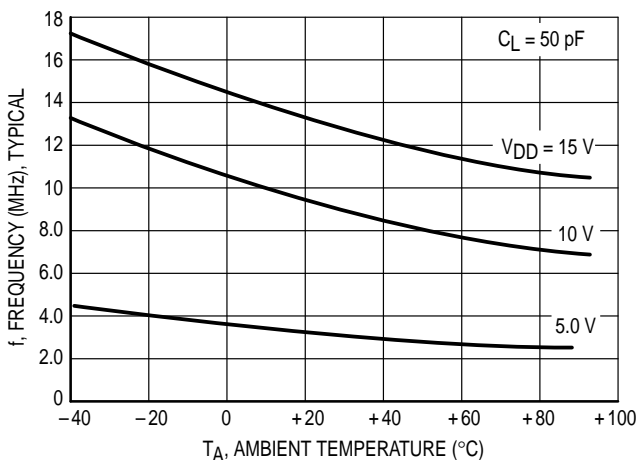
## OPERATING CHARACTERISTICS

The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL<sub>1</sub> and CTL<sub>2</sub>.

The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles, one

pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14568B, MC14522B or the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to “0”, Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V<sub>DD</sub>.



**Table 1. Mode Controls** (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL <sub>1</sub>	CTL <sub>2</sub>	Zero Detect	Q
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

NOTE: Data Preset Inputs (P0–P7) are “Don't Cares” while Cascade Feedback is Low.

**Table 2. Mode Controls** (CTL<sub>1</sub> = Low, CTL<sub>2</sub> = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	256	256	Max Count Illegal State Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	0	0	0	1	1	1	1	15	X		
0	0	0	1	0	0	0	0	16	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	0	1	0	0	0	0	0	32	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	0	0	0	0	0	0	64	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
•	•	•	•	•	•	•	•	•	X		
0	1	1	1	1	1	1	1	127	X		
1	0	0	0	0	0	0	0	128	128		Q Output Active ↓
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
1	0	0	0	1	0	0	0	136	136		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	•		
1	1	1	1	1	1	1	1	255	255		
2 <sup>7</sup>	2 <sup>6</sup>	2 <sup>5</sup>	2 <sup>4</sup>	2 <sup>3</sup>	2 <sup>2</sup>	2 <sup>1</sup>	2 <sup>0</sup>			Bit Value	
128	64	32	16	8	4	2	1			Counting Sequence	
Counter #2 Binary				Counter #1 Binary							

X = No Output (Always Low)

**Table 3. Mode Controls** (CTL<sub>1</sub> = High, CTL<sub>2</sub> = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments		
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q			
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count		
0	0	0	0	0	0	0	1	X	X			
0	0	0	0	0	0	1	0	2	X			
0	0	0	0	0	0	1	1	3	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
0	0	0	0	1	0	0	1	9	X			
0	0	0	1	0	0	0	0	10	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
0	0	0	1	1	0	0	1	19	X			
0	0	1	0	0	0	0	0	20	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
0	0	1	1	0	0	0	0	30	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
0	1	0	0	0	0	0	0	40	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
0	1	0	1	0	0	0	0	50	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
0	1	1	0	0	0	0	0	60	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
0	1	1	1	0	0	0	0	70	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
.	.	.	.	.	.	.	.	.	X			
1	0	0	0	0	0	0	0	80	80		Q Output Active ↓ Bit Value	
.	.	.	.	.	.	.	.	.	.			
.	.	.	.	.	.	.	.	.	.			
.	.	.	.	.	.	.	.	.	.			
1	0	0	1	0	0	0	0	90	90			
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.	.	.	.	.	.	.	.	.	.			
.	.	.	.	.	.	.	.	.	.			
1	1	1	1	0	0	0	0	150	150			
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.	.	.	.	.	.	.	.	.	.			
.	.	.	.	.	.	.	.	.	.			
1	1	1	1	1	0	0	1	159	159			
80	40	20	10	8	4	2	1					Bit Value
Counter #2 Binary				Counter #1 BCD								Counting Sequence

X = No Output (Always Low)

**Table 4. Mode Controls** (CTL<sub>1</sub> = Low, CTL<sub>2</sub> = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
.	.	.	.	.	.	.	.	.	X	
.	.	.	.	.	.	.	.	.	X	
0	0	1	1	0	0	0	0	48	X	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
0	1	0	0	0	0	0	0	64	X	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
0	1	0	1	0	0	0	0	80	X	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
0	1	1	1	0	0	0	0	112	X	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	0	0	0	0	0	128	128	Q Output Active ↓
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	1	0	0	0	0	144	144	
.	.	.	.	.	.	.	.	.	.	
.	.	.	.	.	.	.	.	.	.	
1	0	0	1	1	1	1	1	159	159	
<sup>27</sup>	<sup>26</sup>	<sup>25</sup>	<sup>24</sup>	<sup>23</sup>	<sup>22</sup>	<sup>21</sup>	<sup>20</sup>			Bit Value
128	64	32	16	8	4	2	1			Counting Sequence
Counter #2 BCD				Counter #1 Binary						

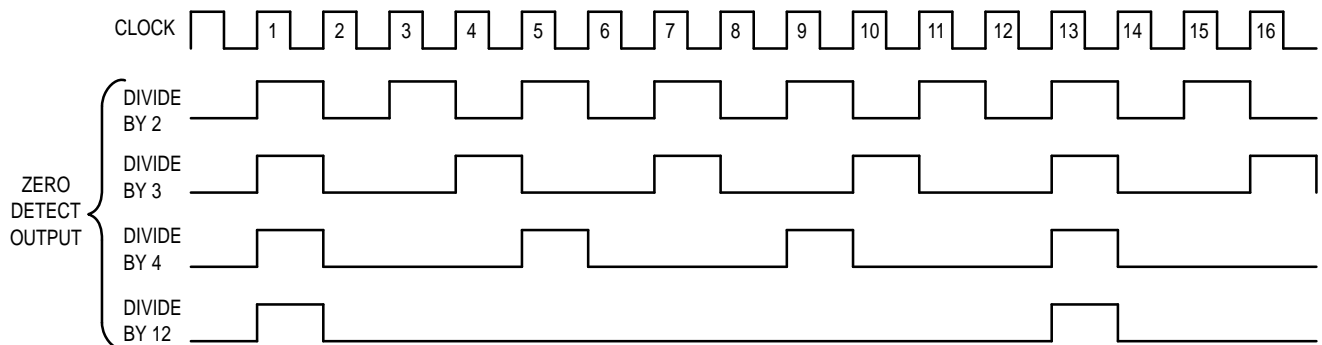
X = No Output (Always Low)

**Table 5. Mode Controls** (CTL<sub>1</sub> = High, CTL<sub>2</sub> = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	100	100	Max Count illegal state Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	0	0	1	0	0	1	9	X		
0	0	0	1	0	0	0	0	10	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	0	1	1	0	0	0	0	30	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	0	0	0	0	0	0	40	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	0	1	0	0	0	0	50	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
0	1	1	1	0	0	0	0	70	X		
.	.	.	.	.	.	.	.	.	X		
.	.	.	.	.	.	.	.	.	X		
1	0	0	0	0	0	0	0	80	80	Q Output Active ↓	
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	0	0	1	0	0	0	0	90	90		
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
.	.	.	.	.	.	.	.	.	.		
1	0	0	1	1	0	0	1	99	99		
.	.	.	.	.	.	.	.	.	.		
80	40	20	10	8	4	2	1			Bit Value	
Counter #2 BCD				Counter #1 BCD							Counting Sequence

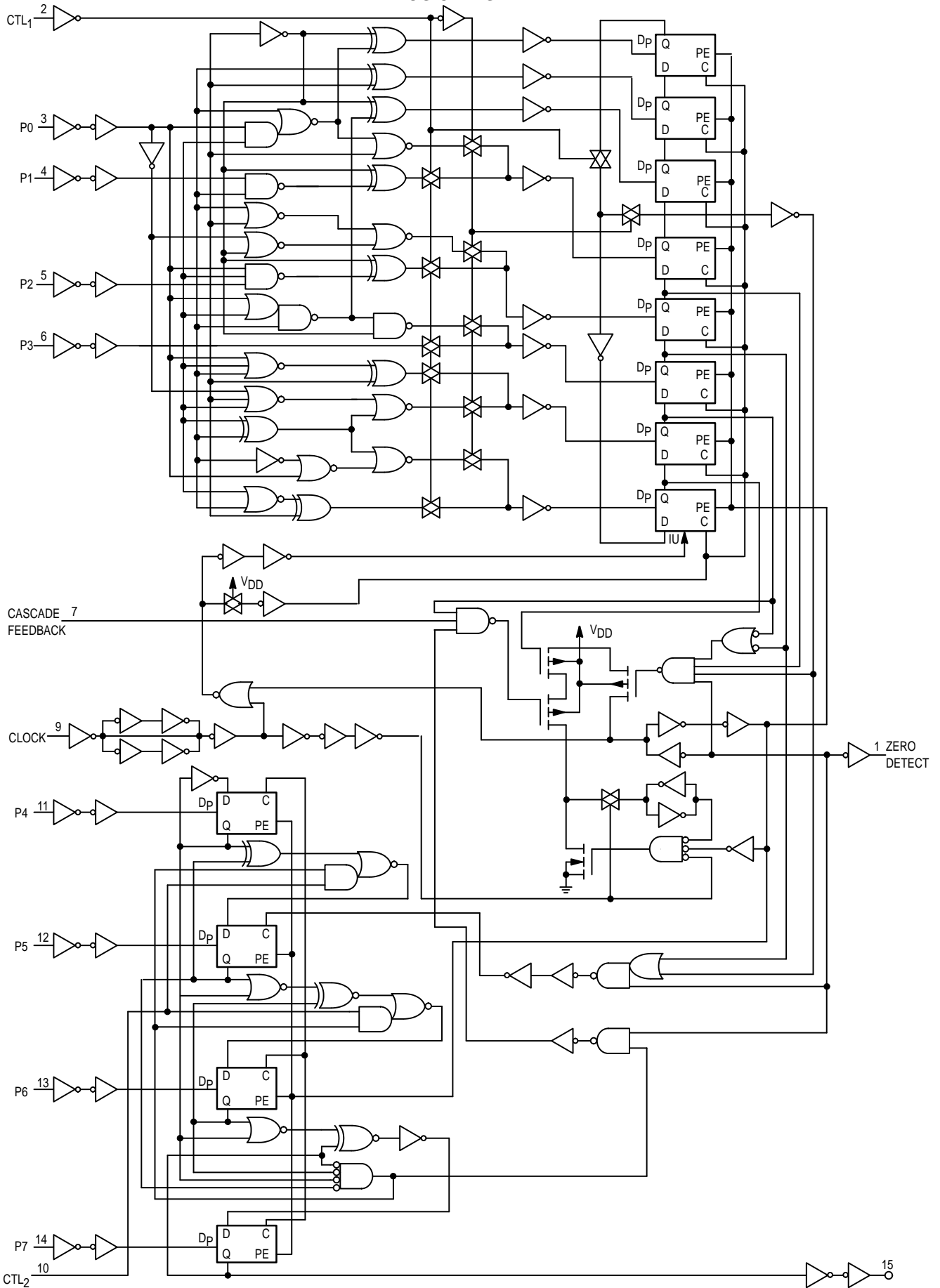
X = No Output (Always Low)

### TIMING DIAGRAM MC14569B





### LOGIC DIAGRAM



## TYPICAL APPLICATIONS

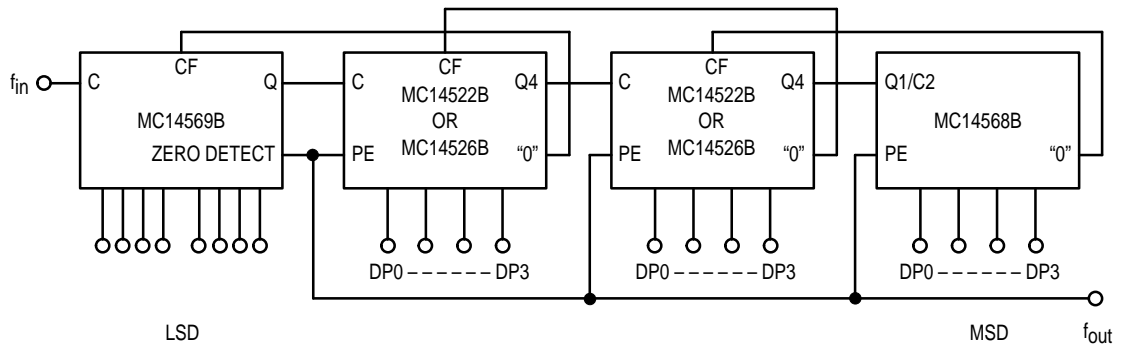


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

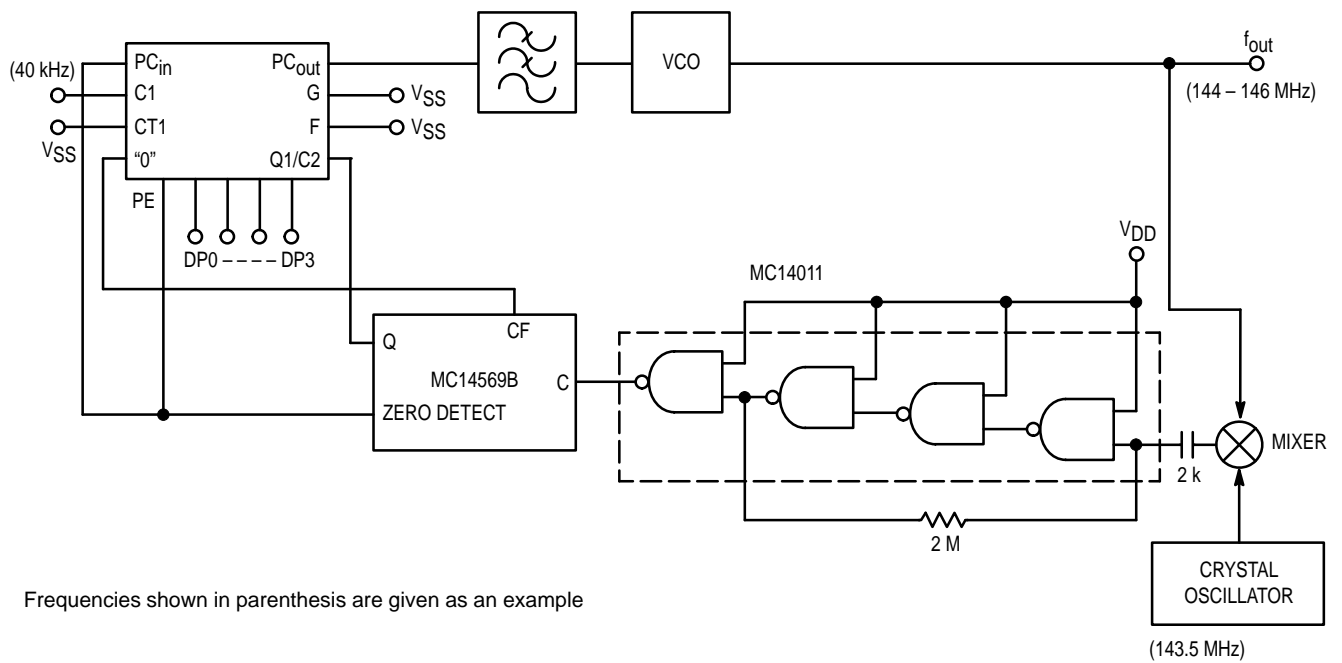
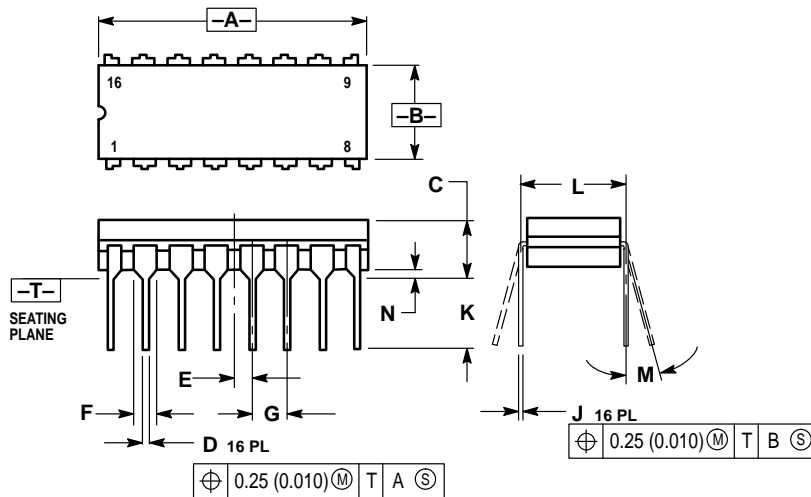


Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

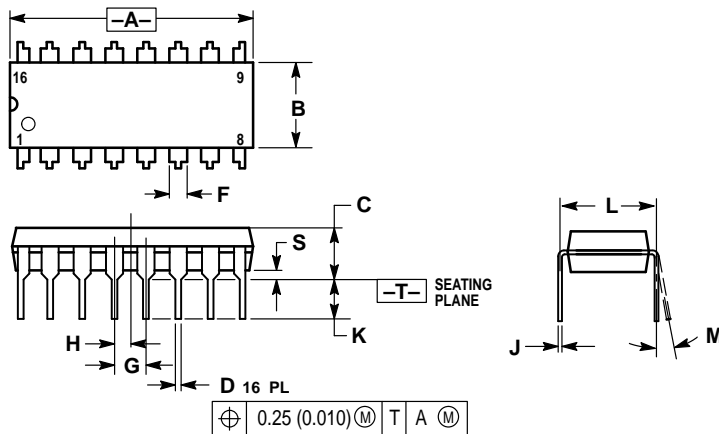


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



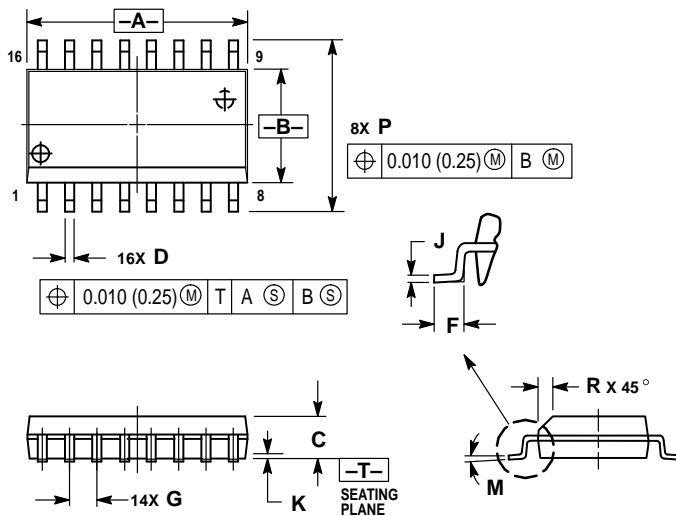
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

# OUTLINE DIMENSIONS

## DW SUFFIX PLASTIC SOIC PACKAGE CASE 751G-02 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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**How to reach us:**  
**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution;  
 P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,  
 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

**MFAX:** RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609  
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 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MC14569B/D

