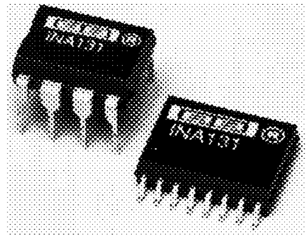
BURR - BROWN®



INA131

Precision G = 100 INSTRUMENTATION AMPLIFIER

FEATURES

- LOW OFFSET VOLTAGE: 50μV max
- LOW DRIFT: 0.25μV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 110dB min
- INPUT OVERVOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA
- 8-PIN PLASTIC DIP, SOL-16 SOIC

APPLICATIONS

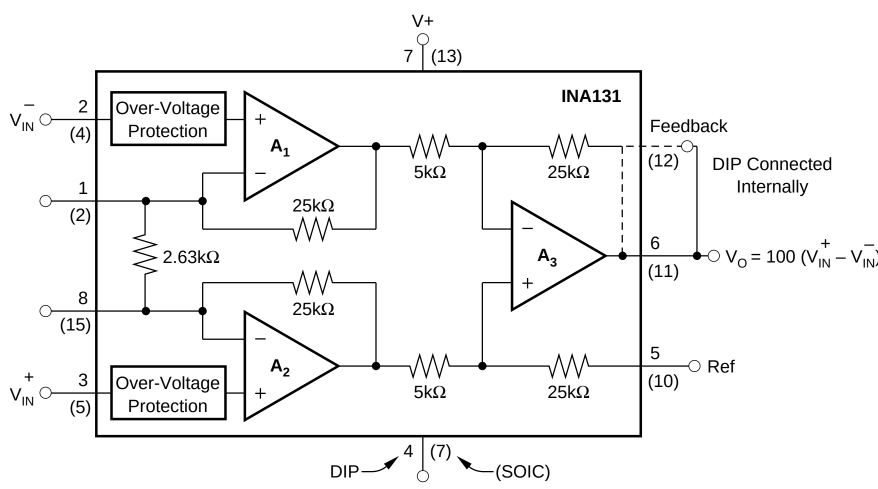
- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

DESCRIPTION

The INA131 is a low cost, general purpose G = 100 instrumentation amplifier offering excellent accuracy. Its 3-op amp design and small size make it ideal for a wide range of applications.

On-chip laser trimmed resistors accurately set a fixed gain of 100. The INA131 is laser trimmed to achieve very low offset voltage (50μV), drift (0.25μV/°C), and high CMR (110dB). Internal input protection can withstand up to ±40V inputs without damage.

The INA131 is available in 8-pin plastic DIP and SOL-16 surface-mount packages. They are specified over the –40°C to +85°C temperature range.



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Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

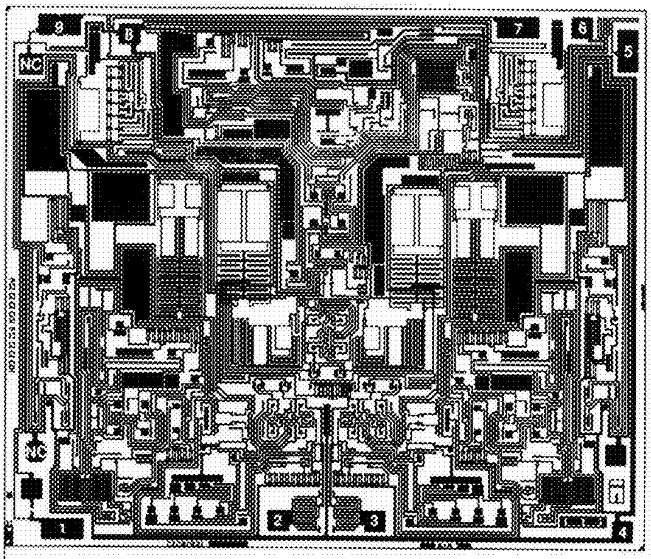
T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

		INA131BP, BU			INA131AP, AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±10	±50		±25	±125	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±0.1	±0.25		±0.25	±1	µV/°C
vs Power Supply	V_S = ±2.25V to ±18V		0.5	3		*	*	µV/V
Long-Term Stability			0.2			*		µV/mo
Impedance, Differential			10^{10} || 6			*		Ω || pF
Common-Mode			10^{10} || 6			*		Ω || pF
Input Common-Mode Range		±11	±13.5		*	*		V
Safe Input Voltage				±40			*	V
Common-Mode Rejection	V_{CM} = ±10V, ΔR_S = 1kΩ	110	120		106	110		dB
BIAS CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
OFFSET CURRENT			±0.5	±2		*	±5	nA
vs Temperature			±8			*		pA/°C
NOISE VOLTAGE, RTI	R_S = 0Ω							
f = 10Hz			16			*		nV/√Hz
f = 100Hz			12			*		nV/√Hz
f = 1kHz			12			*		nV/√Hz
f = 10kHz			12			*		nV/√Hz
f_B = 0.1Hz to 10Hz			0.4			*		µVp-p
Noise Current								
f = 10Hz			0.4			*		pA/√Hz
f= 1kHz			0.2			*		pA/√Hz
f_B = 0.1Hz to 100Hz			18			*		pAp-p
GAIN								
Gain Error(1)			±0.01	±0.024		*	±0.1	%
Resistor Value(2)			±10	±40		*	*	%
Gain vs Temperature			±5	±10		*	±20	ppm/°C
Nonlinearity			±0.0003	±0.002		*	±0.004	% of FSR
OUTPUT								
Voltage	I_O = 5mA, T_{MIN} to T_{MAX}	±13.5	±13.7		*	*		V
	V_S = ±11.4V, R_L = 2kΩ	±10	10.5		*	*		V
	V_S = ±2.25V, R_L = 2kΩ	±1	1.5		*	*		V
Load Capacitance, max	Stable Operation		1000			*		pF
Short Circuit Current			+20/–15			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB			70			*		kHz
Slew Rate	V_O = ±10V	0.3	0.7		*	*		V/µs
Settling Time, 0.01%			100			*		µs
Overload Recovery	50% Overdrive		20			*		µs
POWER SUPPLY								
Voltage Range		±2.25	±15	±18	*	*	*	V
Current	V_{IN} = 0V		±2.2	±3		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating		–40		125	*		*	°C
θ_{JA}			100			*		°C/W

* Specification same as INA131BP/BU.

NOTES: (1) R_L = 10kΩ. (2) Absolute value of internal gain-setting resistors. (Gain depends on resistor ratios.)

DICE INFORMATION



INA131 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	R_G	6	V_O
2	V^-_{IN}	7	Feedback
3	V^+_{IN}	8	V+
4	V–	9	R_G
5	Ref		

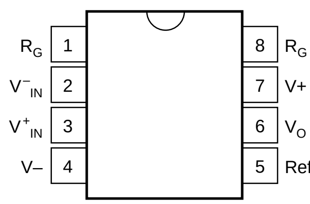
NC = No Connection.
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

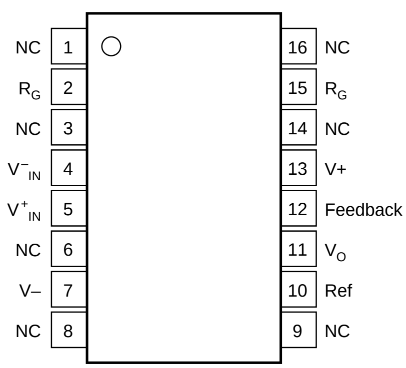
	MILS (0.001")	MILLIMETERS
Die Size	141 x 120 ±5	3.58 x 3.05 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

PIN CONFIGURATIONS

Top View — **P-Package/8-Pin DIP**



Top View — **U-Package/16-Pin SOIC**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering –10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA131AP	8-Pin Plastic DIP	–40°C to +85°C
INA131BP	8-Pin Plastic DIP	–40°C to +85°C
INA131AU	SOL-16 Surface-Mount	–40°C to +85°C
INA131BU	SOL-16 Surface-Mount	–40°C to +85°C

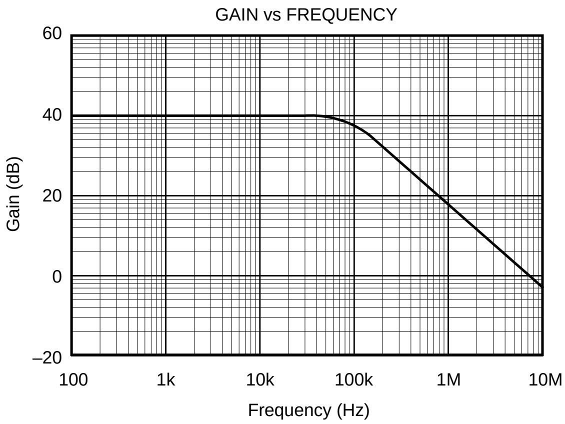
PACKAGE INFORMATION

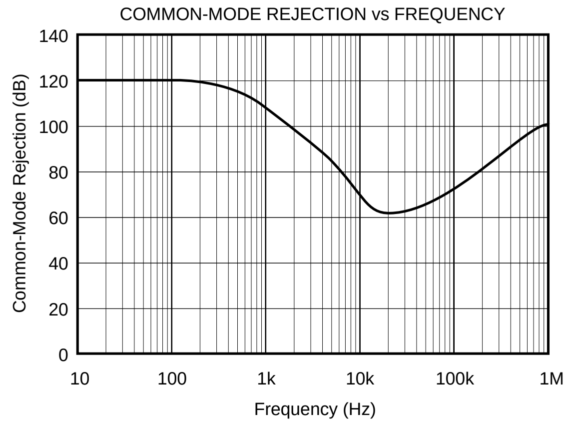
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA131AP	8-Pin Plastic DIP	006
INA131BP	8-Pin Plastic DIP	006
INA131AU	SOL-16 Surface-Mount	211
INA131BU	SOL-16 Surface-Mount	211

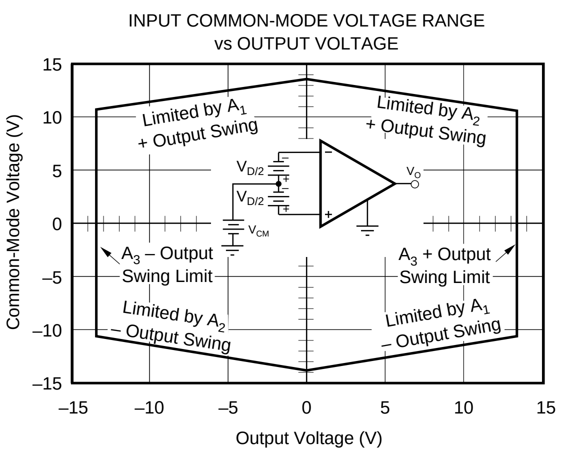
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

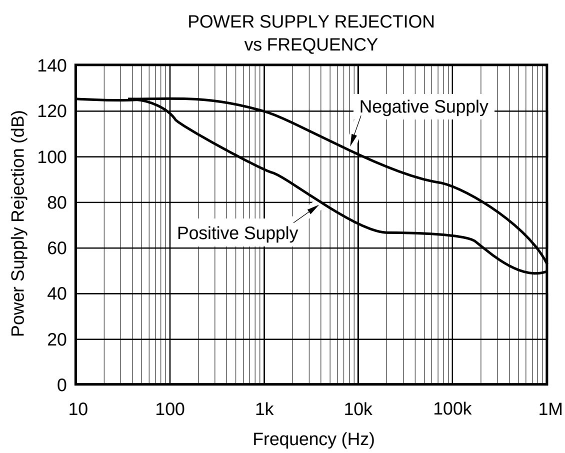
TYPICAL PERFORMANCE CURVES

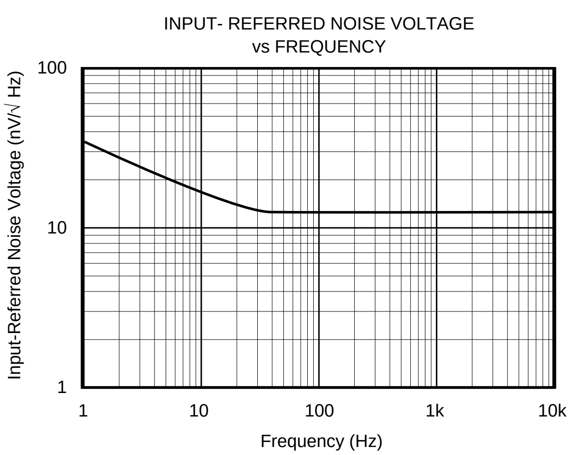
At 25°C, V_S = ±15V, unless otherwise noted.

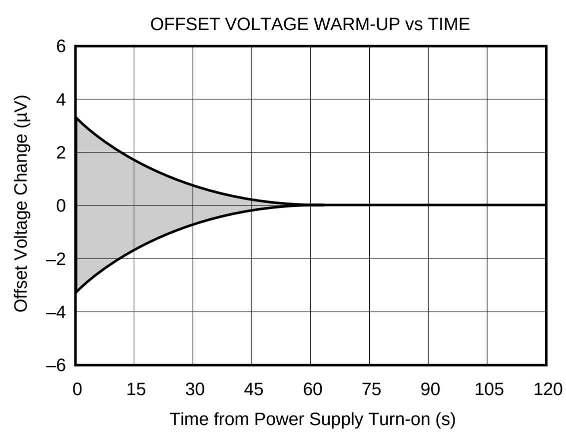








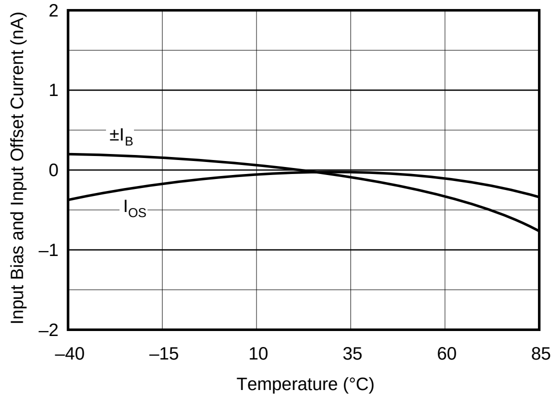




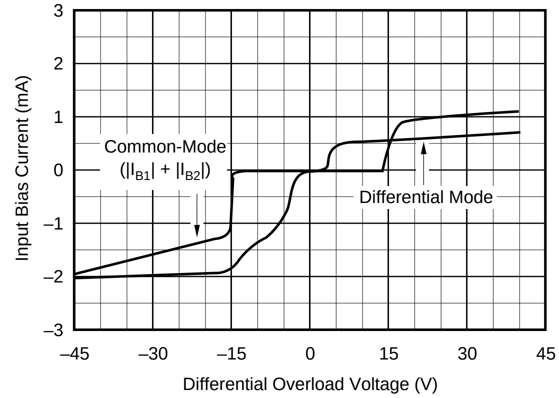
TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, V_S = ±15V, unless otherwise noted.

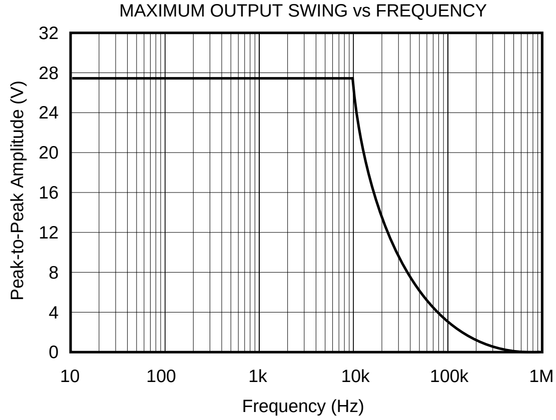
INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE



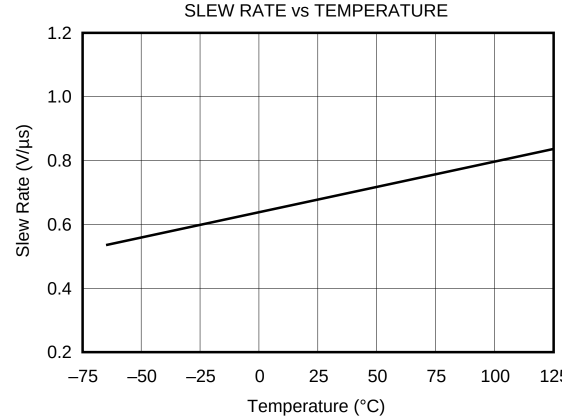
INPUT BIAS CURRENT vs INPUT VOLTAGE



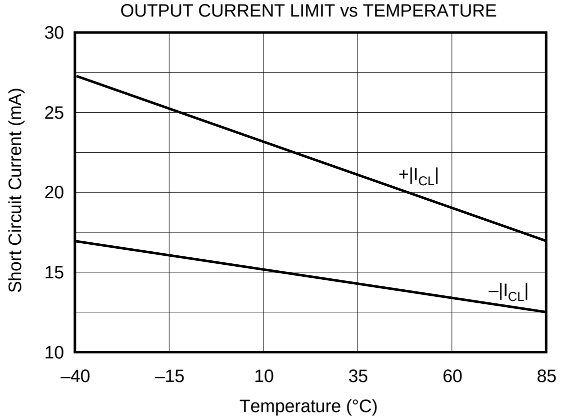
MAXIMUM OUTPUT SWING vs FREQUENCY



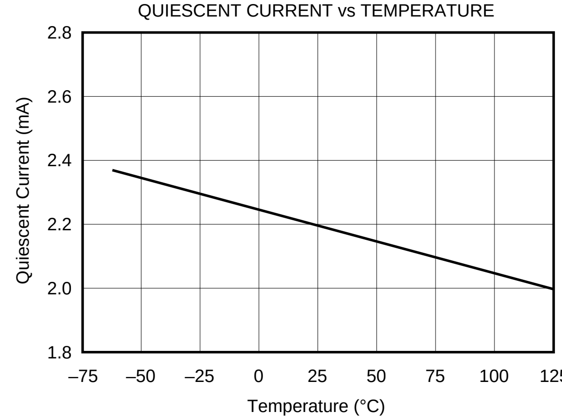
SLEW RATE vs TEMPERATURE



OUTPUT CURRENT LIMIT vs TEMPERATURE



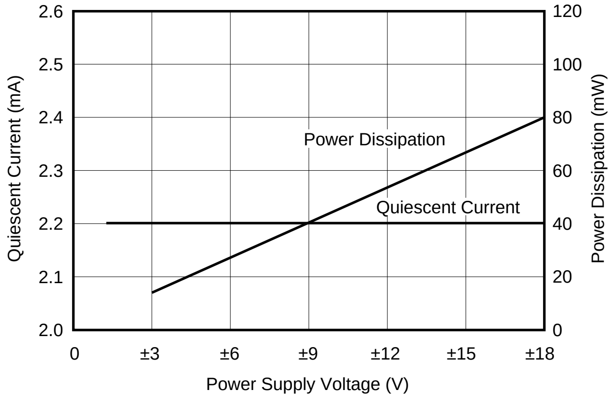
QUIESCENT CURRENT vs TEMPERATURE



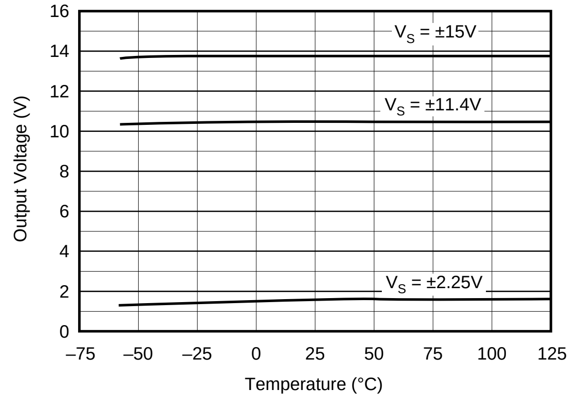
TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, V_S = ±15V, unless otherwise noted.

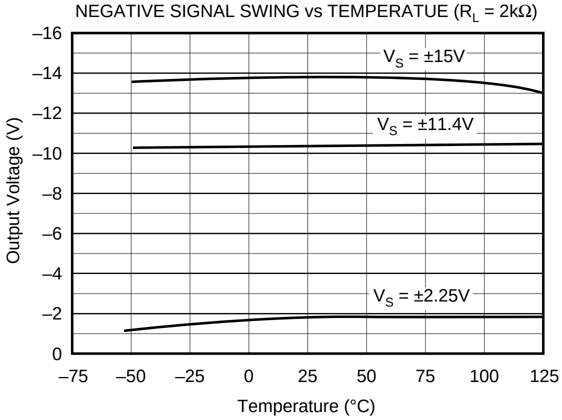
QUIESCENT CURRENT AND POWER DISSIPATION
vs POWER SUPPLY VOLTAGE



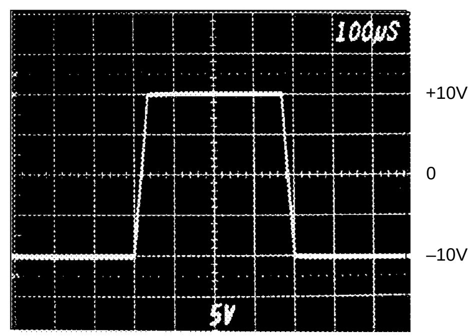
POSITIVE SIGNAL SWING vs TEMPERATUE (R_L = 2kΩ)



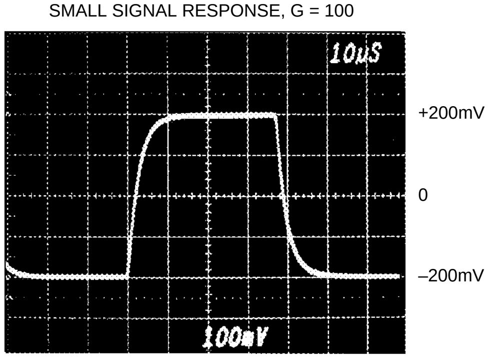
NEGATIVE SIGNAL SWING vs TEMPERATUE (R_L = 2kΩ)



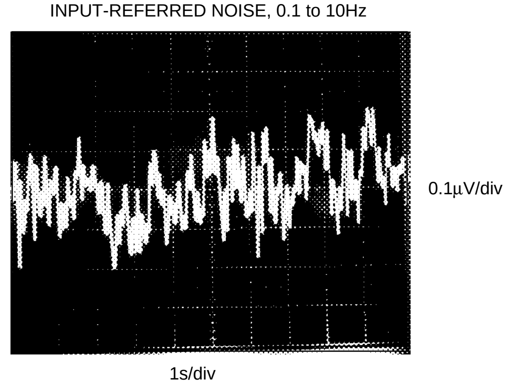
LARGE SIGNAL RESPONSE, G = 100



SMALL SIGNAL RESPONSE, G = 100



INPUT-REFERRED NOISE, 0.1 to 10Hz



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA131. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a device with 110dB CMR to degrade to approximately 106dB CMR.

SETTING THE GAIN

No external resistors are required for G = 100. On-chip laser-trimmed resistors set the gain, providing excellent gain accuracy and temperature stability. Gain is distributed between the input and output stages of the INA131. Bandwidth is increased by approximately five times (compared to the INA114 in G = 100). Input common-mode range is also improved (see "Input Common-Mode Range").

Although the INA131 is primarily intended for fixed G = 100 applications, the gain can be increased by connecting an external resistor to the R_G pins. The internal resistors are trimmed for precise ratios, not to absolute values, so the influence of an external resistor will vary from device to device. Absolute accuracy of the internal values is ±40%. The nominal gain with an external R_G resistor can be calculated by:

$$G = 100 + \frac{250\ k\Omega}{R_G} \quad (1)$$

Where: R_G is the external gain resistor.
Accuracy of the 250kΩ term is ±40%.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1).

NOISE PERFORMANCE

The INA131 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA131 is approximately 0.4µVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of state-of-the-art chopper-stabilized amplifiers.

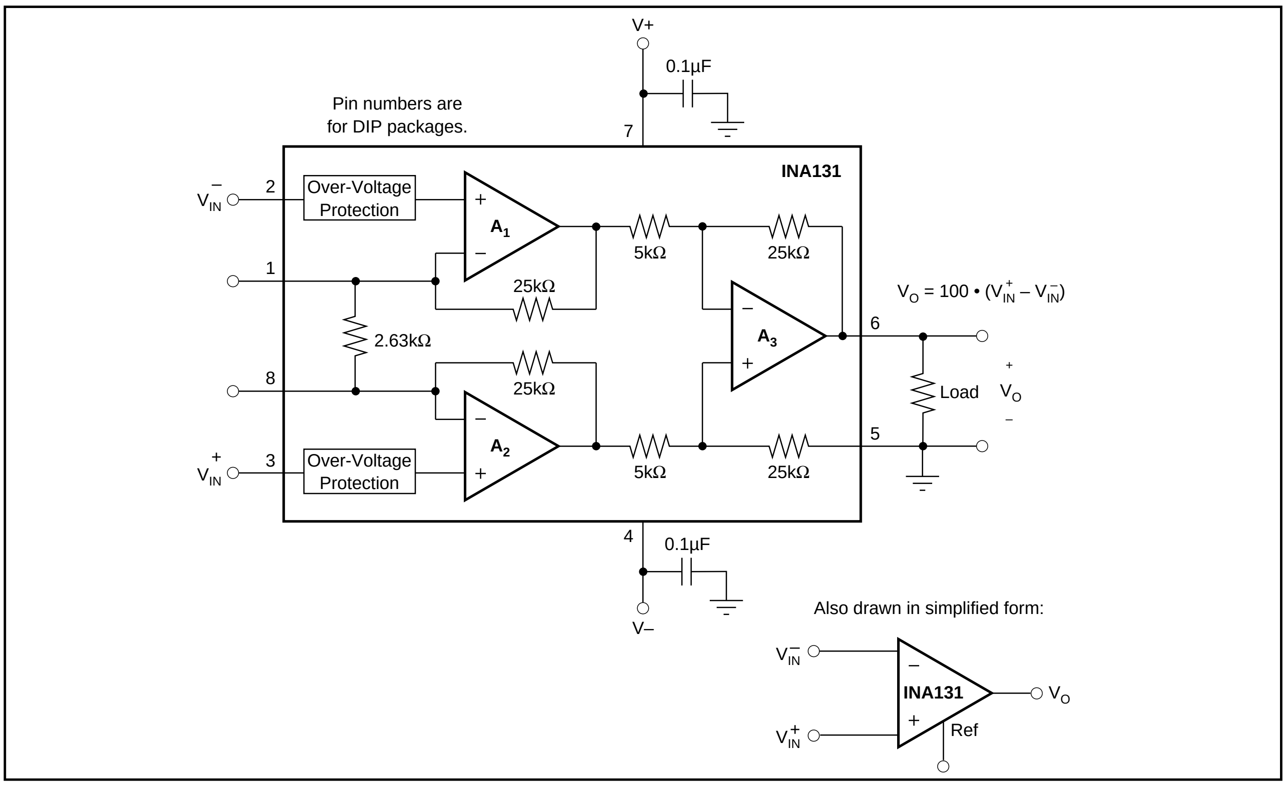


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA131 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

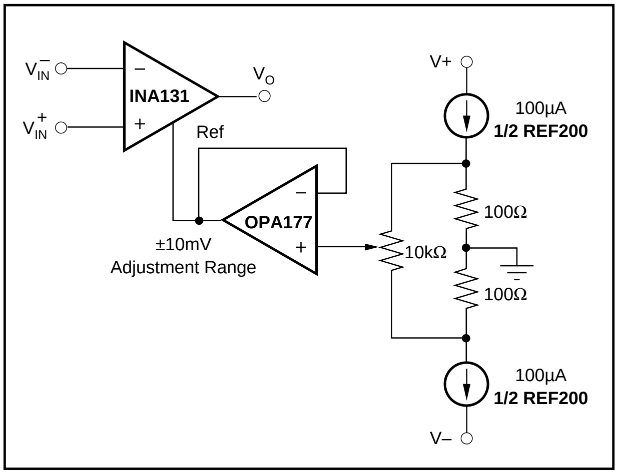


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA131 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA131 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA131 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA131 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range is limited by the output voltage swing of the input amplifiers, A_1 and A_2. The 5V/V output stage gain of the INA131 reduces this effect. Compared to the INA114 and other unity output gain instrumentation amplifiers, the INA131 provides several additional volts of input common-mode range with full output voltage swing. See the typical performance curve "Input Common-Mode Range vs Output Voltage".

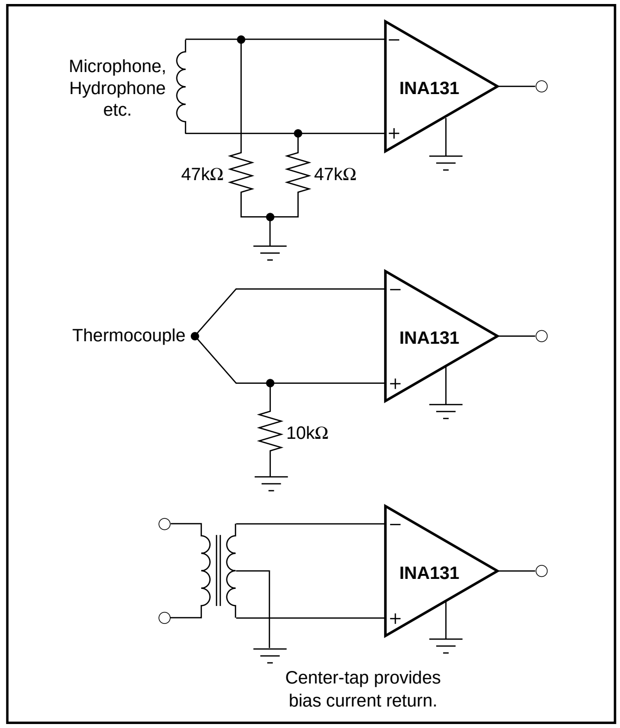


FIGURE 3. Providing an Input Common-Mode Current Path.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA131 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA131 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA131 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA131.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 4 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1. Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 5).

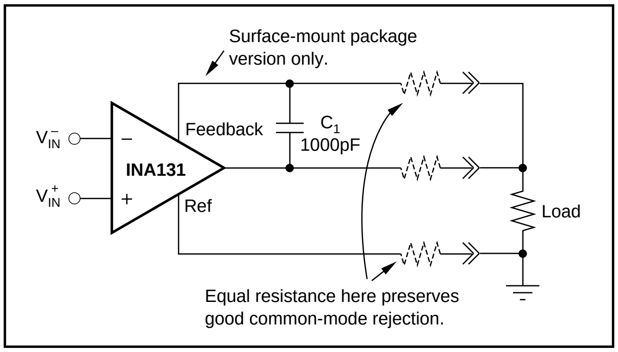


FIGURE 4. Remote Load and Ground Sensing.

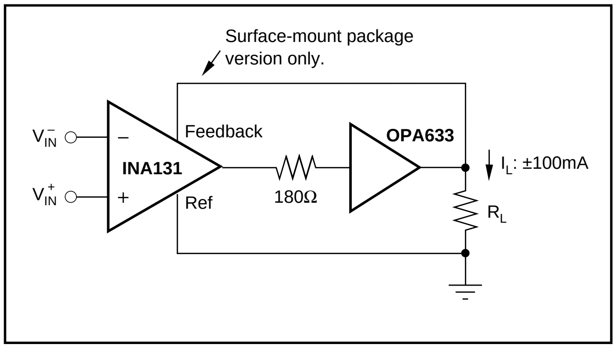


FIGURE 5. Buffered Output for Heavy Loads.

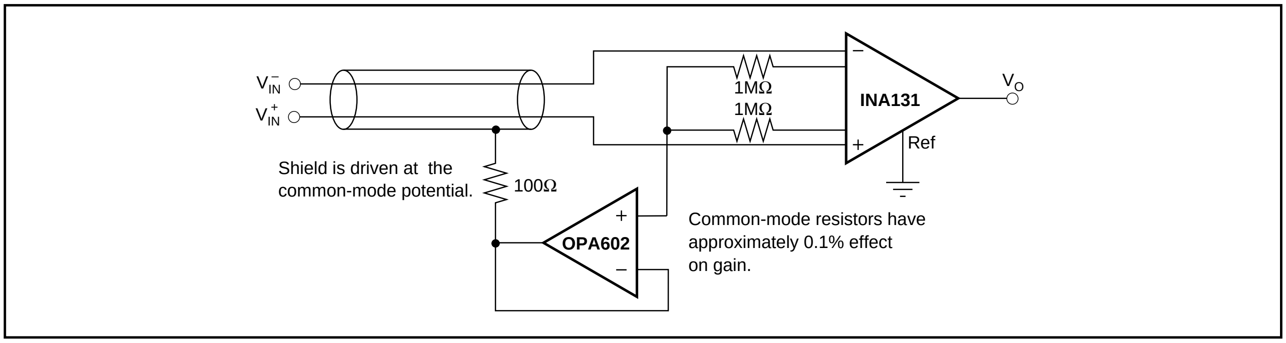


FIGURE 6. Shield Driver Circuit.

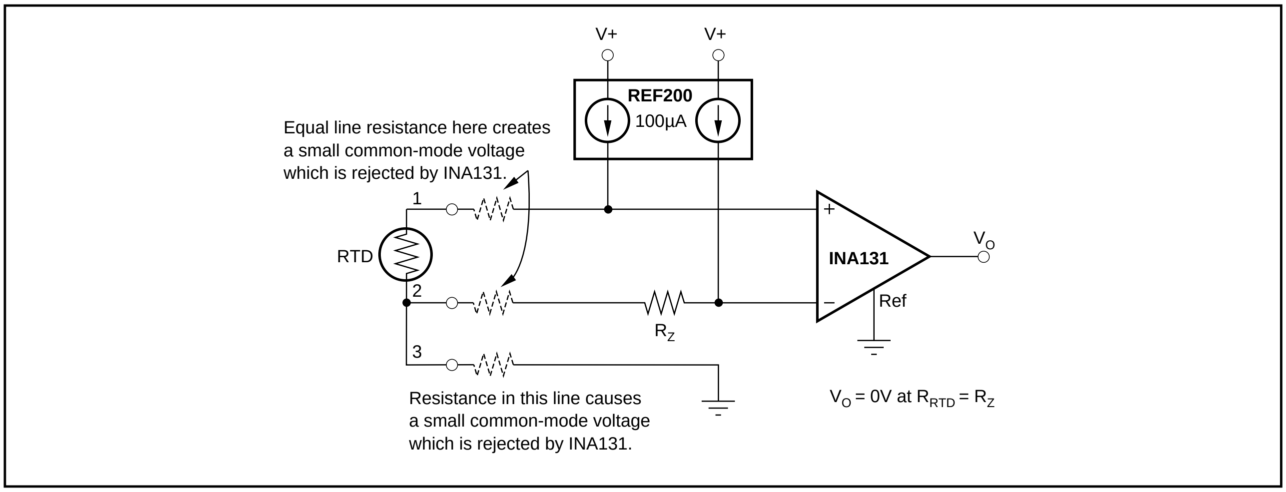
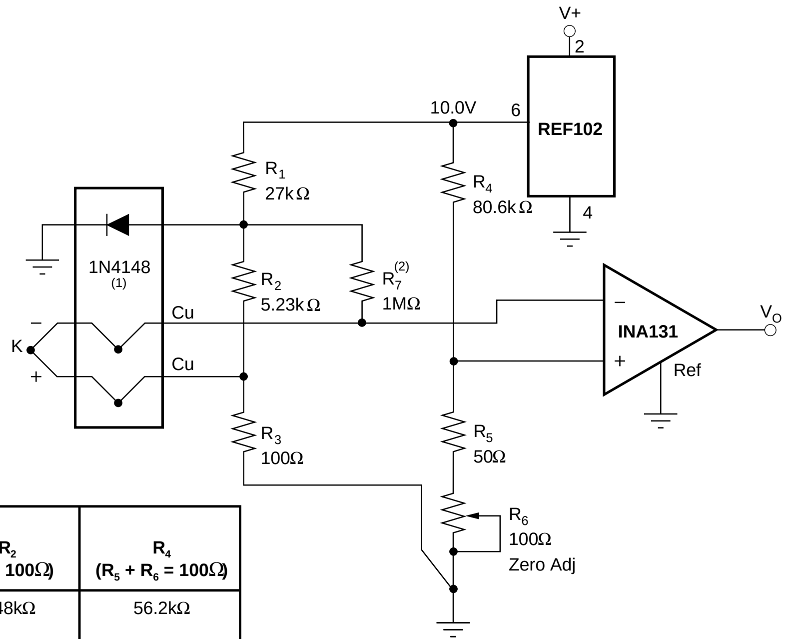


FIGURE 7. RTD Temperature Measurement Circuit.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper Constantan	38.0	5.49kΩ	84.5kΩ

NOTES: (1) –2.1mV/°C at 200µA. (2) R_7 provides down-scale burn-out indication.

FIGURE 8. Thermocouple Amplifier with Cold Junction Compensation.

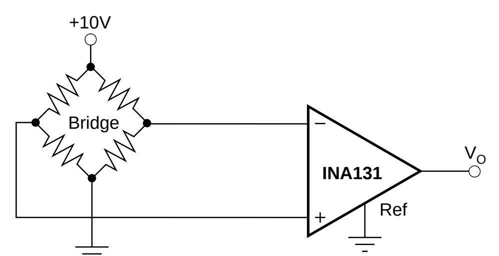


FIGURE 9. Bridge Transducer Amplifier.

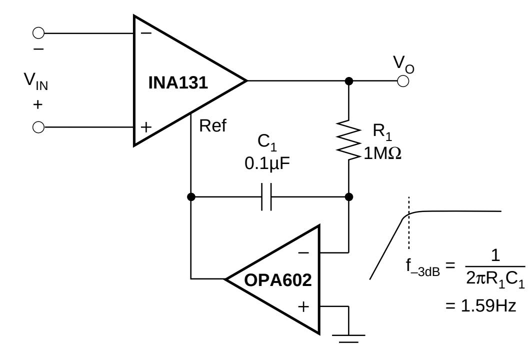
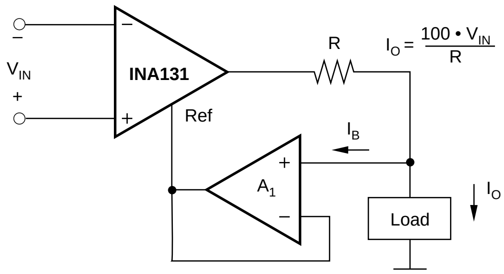


FIGURE 10. AC-Coupled Instrumentation Amplifier.



A_1	I_B Error
OPA177	±1.5nA
OPA602	1pA
OPA128	75fA

FIGURE 11. Differential Voltage to Current Converter.

PACKAGE DRAWINGS

Package Number 006 - 8-Pin Plastic, Single-Wide DIP

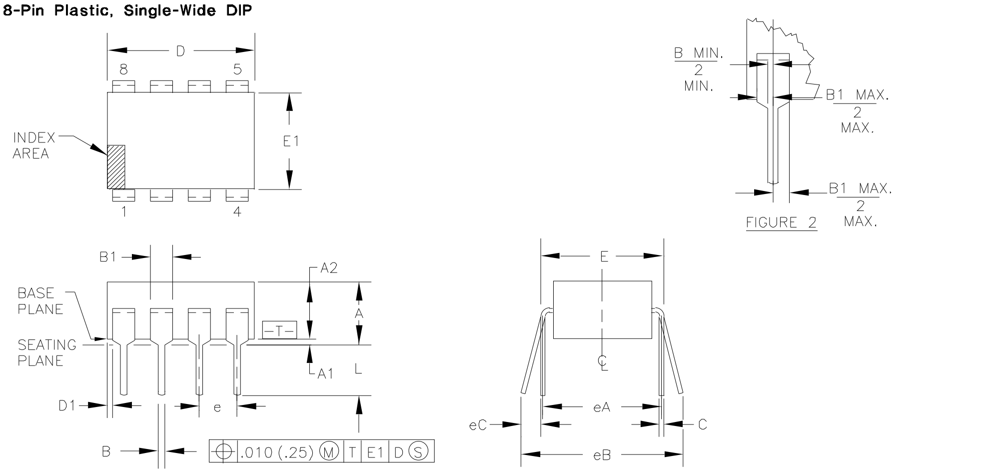


FIGURE 1

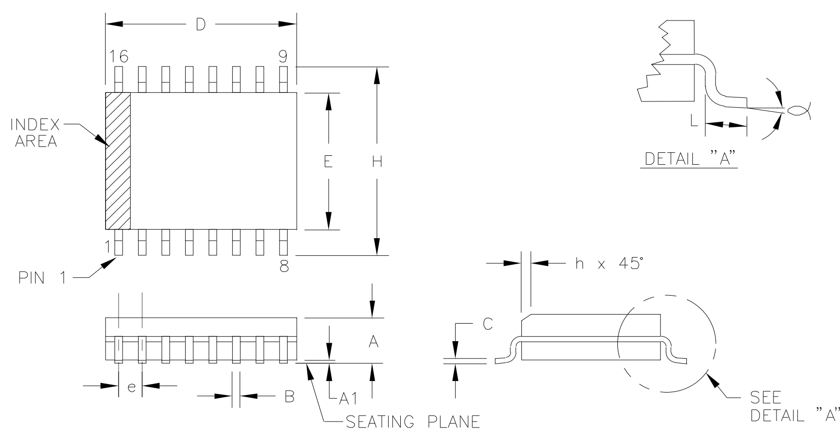
DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	--	.210	--	5.33	3
A1	.015	--	0.38	--	3
A2	.115	.195	2.92	4.95	
B	.014	.022	0.36	0.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	0.20	0.38	
D	.348	.430	8.84	10.92	4
D1	.005	--	0.13	--	
E	.300	.325	7.62	8.26	5
E1	.240	.280	6.10	7.11	4
e	.100 BASIC		2.54 BASIC		
eA	.300 BASIC		7.63 BASIC		5
eB	--	.430	--	10.92	6
L	.115	.160	2.92	4.06	3
N	8		8		7

NOTES:

1. CONTROLLING DIMENSION: INCH. IN CASE OF CONFLICT BETWEEN THE ENGLISH AND METRIC DIMENSIONS, THE INCH DIMENSIONS CONTROL.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
3. DIMENSIONS A, A1, AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. D AND E1 DIMENSIONS FOR PLASTIC PACKAGES DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.25mm).
5. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED. eC MUST BE ZERO OR GREATER.
7. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
8. CORNER LEADS (1, 4, 5, AND 8) MAY BE CONFIGURED AS SHOWN IN FIGURE 2.
9. FOR AUTOMATIC INSERTION, ANY RAISED IRREGULARITY ON THE TOP SURFACE (STEP, MESA, ETC.) SHALL BE SYMMETRICAL ABOUT THE LATERAL AND LONGITUDINAL PACKAGE CENTERLINES.

PACKAGE NUMBER: ZZ006 REV.: D
JEDEC NUMBER: MS-001

Package Number 211 - 16-Lead SOIC



DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTE
A	.093	.104	2.36	2.64	
A1	.004	.011	0.10	0.28	
B	.014	.019	0.36	0.48	
C	.0095	.012	0.24	0.30	
D	.398	.413	10.11	10.49	2
E	.292	.299	7.42	7.59	2
e	.050 BASIC		1.27 BASIC		
H	.394	.419	10.01	10.64	
h	.010	.029	0.25	0.74	3
L	.016	.050	0.41	1.27	4
N	16		16		5
∝	0°	8°	0°	8°	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
2. "D" AND "E" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15mm (.006 in.).
3. THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE CROSS-HATCHED AREA.
4. "L" IS THE LENGTH OF THE TERMINAL FOR SOLDERING TO A SUBSTRATE.
5. "N" IS THE NUMBER OF TERMINAL POSITIONS.
6. LEAD TO LEAD COPLANARITY SHALL BE LESS THAN .004 INCHES FROM SEATING PLANE.

PACKAGE NUMBER: ZZ211 REV.: D
JEDEC NUMBER: MS-013