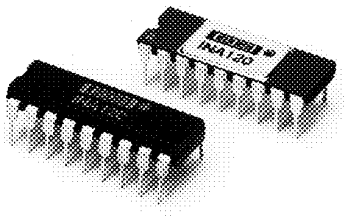
BURR - BROWN®



INA120

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE: 25μV max**
- **LOW OFFSET VOLTAGE DRIFT: 0.25μV/°C max**
- **PIN-STRAPPED GAINS: 1, 10, 100, 1000**
- **LOW GAIN DRIFT: 30ppm/°C max at G = 100**
- **HIGH COMMON-MODE REJECTION: 106dB at 60Hz, G = 100**

APPLICATIONS

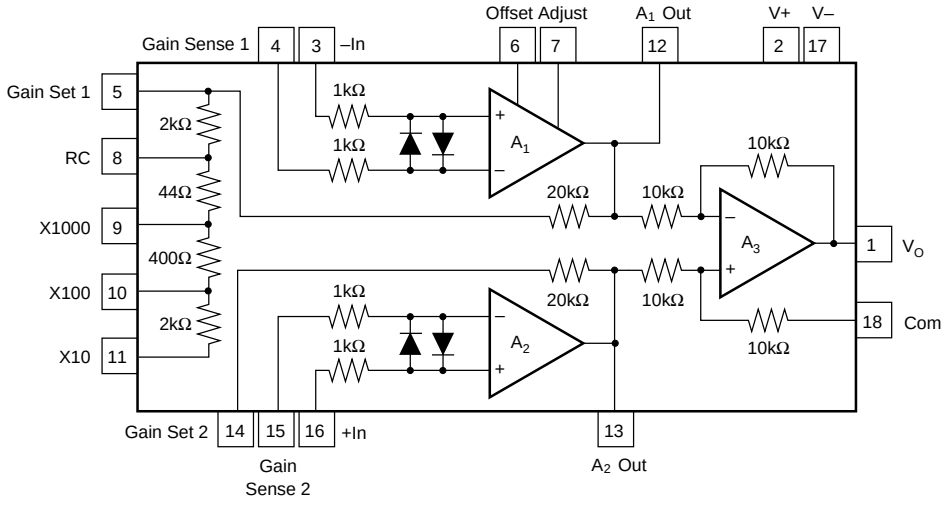
- **BRIDGE AMPLIFIER**
- **THERMOCOUPLE AMPLIFIER**
- **RTD SENSOR AMPLIFIER**
- **MEDICAL INSTRUMENTATION**
- **DATA ACQUISITION SYSTEM**
- **SWITCHED-GAIN AMPLIFIER**

DESCRIPTION

The INA120 is a precision instrumentation amplifier ideal for accurate signal acquisition. It combines precision, protected-input operational amplifiers, laser-trimmed gain-setting resistors, and a high common-mode rejection difference amplifier on a single chip.

Simple pin-strapped connections set precise gains of 1, 10, 100 or 1000. External resistors can be used to set any gain from one to 5000. Gains can be digitally selected with an external multiplexer. Gain-sense connections on the INA120 maintain accuracy when using multiplexer or gain-switching circuitry. Low power dissipation and careful on-chip thermal management reduce warm-up drift and assure excellent long-term stability.

The INA120 is available in both plastic and ceramic 18-pin DIP packages, specified for the industrial temperature range.



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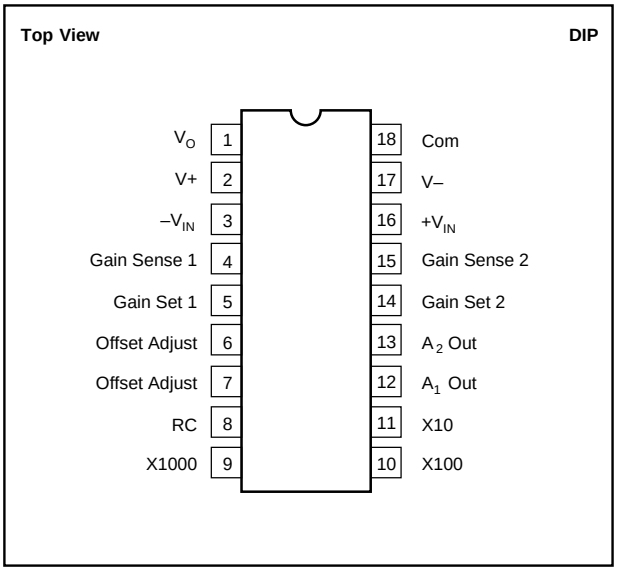
SPECIFICATIONS

At T_A = +25°C and V_S = ±15V unless otherwise specified.

PARAMETER	CONDITIONS	INA120CG MIN	INA120CG TYP	INA120CG MAX	INA120BG, BP MIN	INA120BG, BP TYP	INA120BG, BP MAX	INA120AP MIN	INA120AP TYP	INA120AP MAX	UNITS
GAIN											
Range of Gain		1		1000	1		1000	1		1000	V/V
Gain Equation			$1 + (2R_F/R_G)$			$1 + (2R_F/R_G)$			$1 + (2R_F/R_G)$		V/V
Gain Error	G = 1		0.01	0.05		0.01	0.05		0.02	0.1	%
	G = 10		0.05	0.1		0.05	0.2		0.1	0.2	%
	G = 100		0.1	0.2		0.1	0.3		0.2	0.5	%
	G = 1000		0.3	0.5		0.3	1		0.5	1	%
Gain Temp Coefficient	G = 1		4	10		4	20		6	20	ppm/°C
	G = 10		4	10		4	20		8	40	ppm/°C
	G = 100		6	30		6	40		10	60	ppm/°C
	G = 1000		22	50		22	50		40	100	ppm/°C
Nonlinearity	G = 1		0.001	0.005		0.001	0.01		0.001	0.01	% of FS
	G = 10		0.002	0.005		0.002	0.01		0.002	0.01	% of FS
	G = 100		0.004	0.01		0.004	0.02		0.004	0.02	% of FS
	G = 1000		0.008	0.05		0.008	0.1		0.008	0.1	% of FS
OFFSET VOLTAGE											
Initial Offset			(10+ 300/G)	(25+ 600/G)		(50+ 300/G)	(100+ 1000/G)		(50+ 600/G)	(200+ 2000/G)	µV
vs Temperature			(.25 + 10/G)			(1 + 20/G)			(2 + 20/G)		µV/°C
vs Power Supply	V_S = ±6V to ±18V		(1 + 20/G)	(10 + 150/G)		(1 + 20/G)	(20 + 250/G)		(1 + 20/G)	(40 + 300/G)	µV/V
INPUT BIAS CURRENT											
Initial Bias Current			±7	±20		±7	±20		±20	±50	nA
vs Temperature			±0.2			±0.2			±0.2		nA/°C
Initial Offset Current			±5	±10		±5	±20		±10	±50	nA
vs Temperature			±0.2			±0.2			±0.2		nA/°C
Impedance: Differential			10^{10} || 3			10^{10} || 3			10^{10} || 3		Ω || pF
Common-Mode			10^{10} || 3			10^{10} || 3			10^{10} || 3		Ω || pF
INPUT VOLTAGE RANGE											
Range, Linear Response		±10	±12.5		±10	±12.5		±10	±12.5		V
CMRR (DC, 1kΩ Source Imbalance)	G = 1	80	90		74	90		70	85		dB
	G = 10	96	106		90	106		86	95		dB
	G = 100	106	110		106	110		100	105		dB
	G = 1000	106	110		106	110		100	105		dB
NOISE											
Input Voltage Noise											
f_B = 0.1Hz to 10Hz	G = 1000		0.7			0.7			0.7		µV p-p
Density; f = 10Hz	G = 1000		14			14			14		nV/√Hz
f = 100Hz			11			11			11		nV/√Hz
f = 1000Hz			10			10			10		nV/√Hz
Input Current Noise											
f_B = 0.1Hz to 10Hz			50			50			50		pAp-p
Density; f = 10Hz			1.8			1.8			1.8		pA/√Hz
f = 1kHz			0.4			0.4			0.4		pA/√Hz
Output Voltage Noise											
f_B = 0.1Hz to 10Hz			8			8			8		µVp-p
DYNAMIC RESPONSE											
Small Signal Bandwidth (–3dB)	G = 1		2			2			2		MHz
	G = 10		200			200			200		kHz
	G = 100		20			20			20		kHz
	G = 1000		2			2			2		kHz
Slew Rate		0.4	0.6		0.4	0.6		0.4	0.6		V/µs
Settling Time to 0.01%	G = 1		24			24			24		µs
	G = 10		30			30			30		µs
	G = 100		50			50			50		µs
	G = 1000		200			200			200		µs
Full Power Bandwidth, G < 200	V_O = ±10V, R_L = 2kΩ		9			9			9		kHz
Overload Recovery	50% Overdrive		2			2			2		µs
OUTPUT											
Voltage, R_L = 2kΩ	Over Temperature	±10.5	±12.8		±10.5	±12.8		±10.5	±12.8		V
Current	Over Temperature	5	15		5	15		5	15		mA
Short-Circuit Current			24			24			24		mA
Capacitive Load, Stable Operation			4000			4000			4000		pF
POWER SUPPLY											
Rated Voltage			±15			±15			±15		V
Voltage Range		±6		±18	±6		±18	±6		±18	V
Supply Current	V_O = 0V		±2.7	±4		±2.7	±4		±2.7	±4	mA
TEMPERATURE RANGE											
Specification		–25		+85	–25		+85	–25		+85	°C
Operation BP,AP					–40		+85	–40		+85	°C
Operation CG,BG		–55		+125	–55		+125				°C
Storage		–65		+150	–65		+150	–65		+150	°C
		See Absolute Maximum Table.									

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	(V+) +2 to (V–) –2V
Differential Input Voltage	Total V_S +4V
Operating Temperature	
Ceramic G Package	–65°C to +150°C
Plastic P Package	–40°C to +125°C
Storage Temperature	
Ceramic G Package	–65°C to +150°C
Plastic P Package	–40°C to +125°C
Junction Temperature	
Ceramic G Package	+175°C
Plastic P Package	+125°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA120AP	18-Pin Plastic DIP	218
INA120BP	18-Pin Plastic DIP	218
INA120BG	18-Pin Ceramic DIP	158
INA120CG	18-Pin Ceramic DIP	158

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

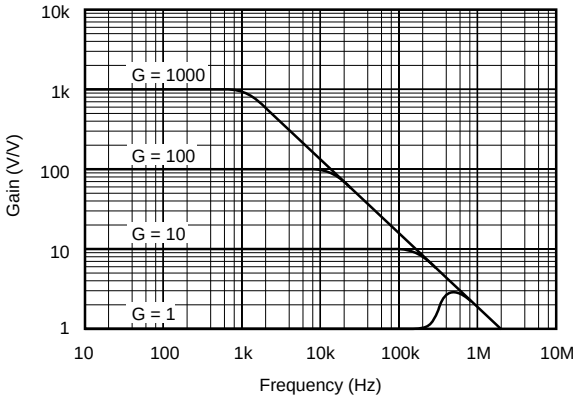
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA120AP	18-Pin Plastic DIP	–25°C to +85°C
INA120BP	18-Pin Plastic DIP	–25°C to +85°C
INA120BG	18-Pin Ceramic DIP	–25°C to +85°C
INA120CG	18-Pin Ceramic DIP	–25°C to +85°C

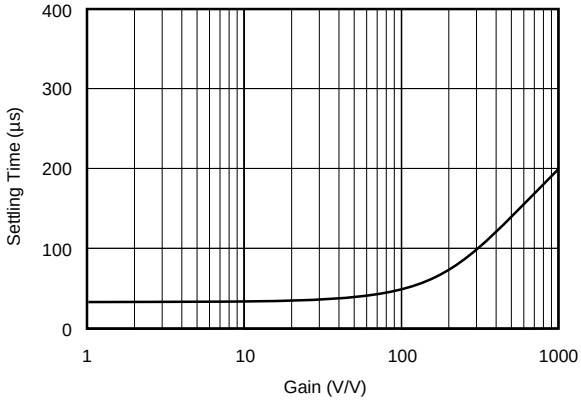
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

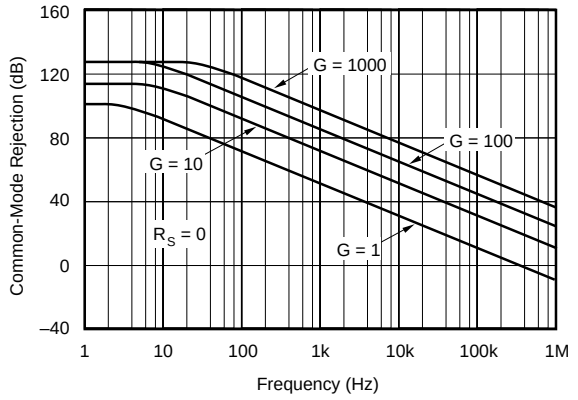
GAIN vs FREQUENCY



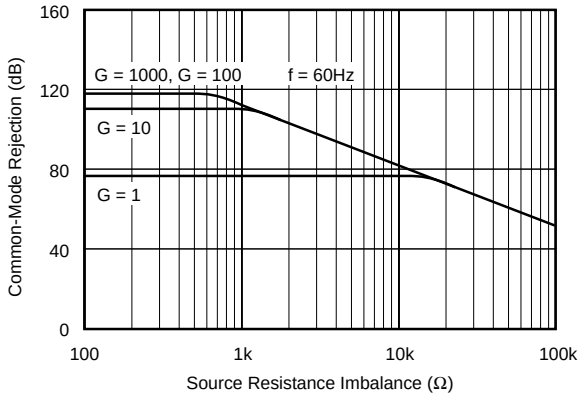
SETTLING TIME vs GAIN (0.1%)



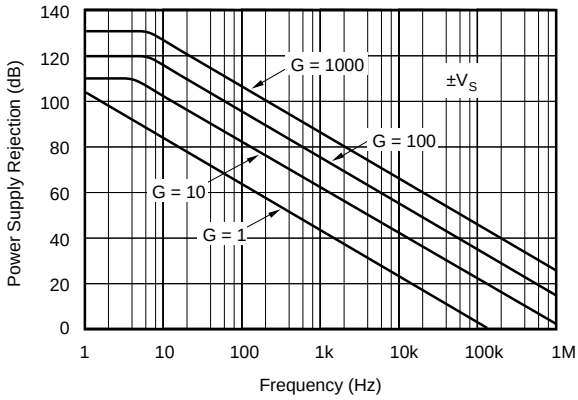
COMMON-MODE REJECTION
vs FREQUENCY



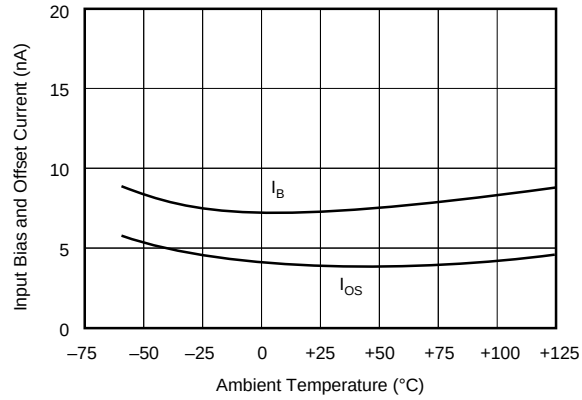
COMMON-MODE REJECTION
vs SOURCE RESISTANCE IMBALANCE



POWER SUPPLY REJECTION
vs FREQUENCY



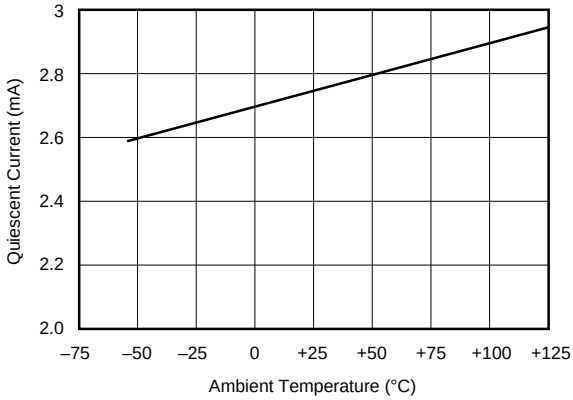
INPUT BIAS AND OFFSET CURRENT
vs TEMPERATURE



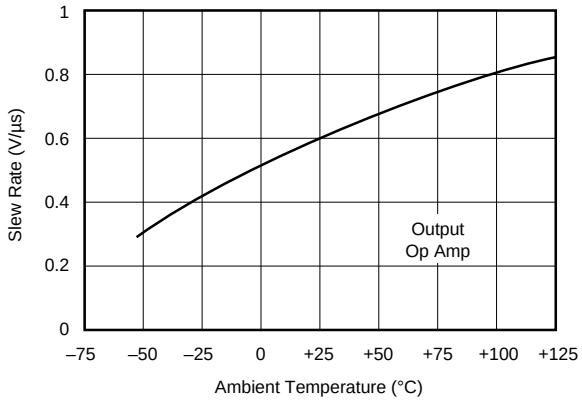
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

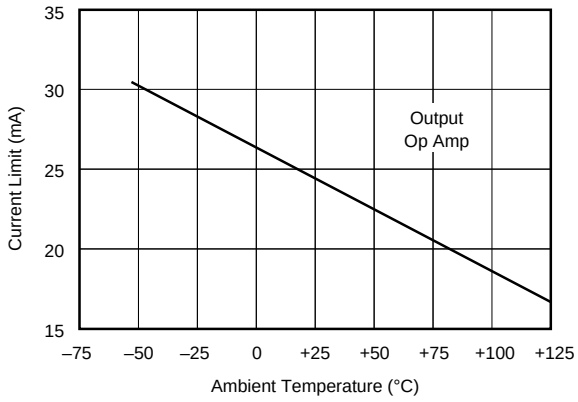
QUIESCENT CURRENT vs TEMPERATURE



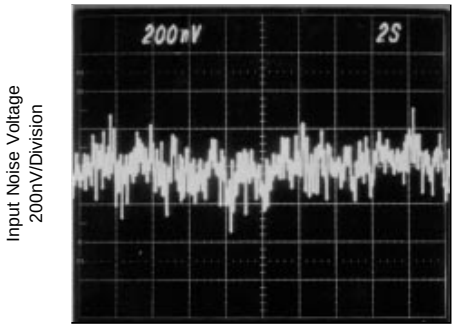
SLEW RATE vs TEMPERATURE



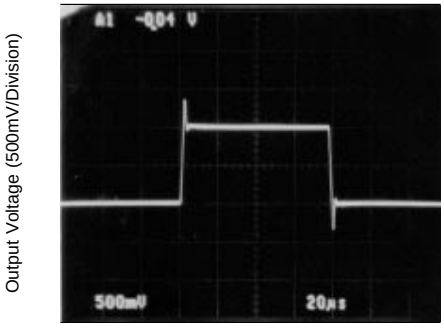
CURRENT LIMIT vs TEMPERATURE



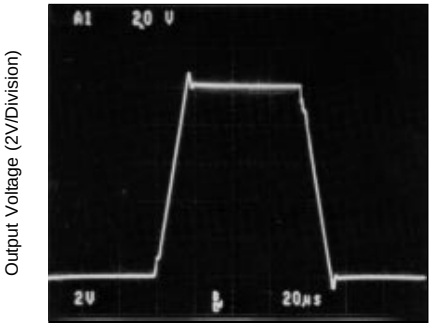
INPUT-REFERRED NOISE
G = 1000



SMALL-SIGNAL TRANSIENT RESPONSE
G = 1



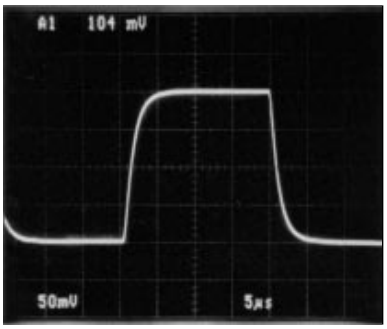
LARGE-SIGNAL TRANSIENT
RESPONSE G = 1



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

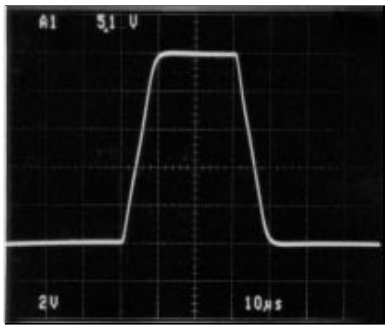
SMALL-SIGNAL TRANSIENT RESPONSE
G = 100



Output Voltage (50mV/Division)

Time (5µs/ Division)

LARGE-SIGNAL TRANSIENT
RESPONSE G = 100



Output Voltage (2V/Division)

Time (10µs/ Division)

APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA120. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins as shown. The differential input voltage is applied to pins 16 and 3.

The output is referred to the output common reference terminal, pin 18. This terminal must have a low-impedance connection to ground. A resistance of 1Ω or greater in series with the common terminal could degrade common-mode rejection beyond the specified value.

SETTING THE GAIN

Gains of 1, 10, 100 or 1000 can be configured by interconnecting the gain-set pins as shown in the table of Figure 1. These pin-strapped gains provide best gain accuracy and drift because they are determined by the ratios of accurately trimmed and matched on-chip resistors.

Digital gain control can be achieved using an analog multiplexer as shown in Figure 2. Since the switches are in series with the high impedance gain-sense connections, pins 4 and 15, their series resistance does not significantly affect gain error or drift. Gain error at G = 1 is slightly higher than with direct pin connections shown in Figure 1. The gain is selected with a two-bit address, A_0 and A_1. The Multiplexer Enable control is directly connected to V+ since a logic "low" on this line would cause the input amplifiers to run open-loop.

Other gains may be set by connecting an external resistor, R_G, as shown in Figure 3a. Gain accuracy using an external gain-setting resistor is a function of R_G and the internal 20kΩ resistors. The internal resistors are typically within ±0.2% of nominal value and their drift under ±80ppm/°C. Inaccuracy and drift of R_G will contribute additional gain error and drift.

Figure 3b shows an external gain-setting resistor connected in parallel with internal resistors. By forming a portion of the effective R_G with internal resistors, gain accuracy and drift can be somewhat improved.

Connections available on the INA120 allow all input stage gain-setting resistors to be provided externally. A custom precision resistor network could be connected to provide the highest accuracy and lowest gain drift for non-standard gains. Impedance of this external network should be made close to that of the internal network for best performance.

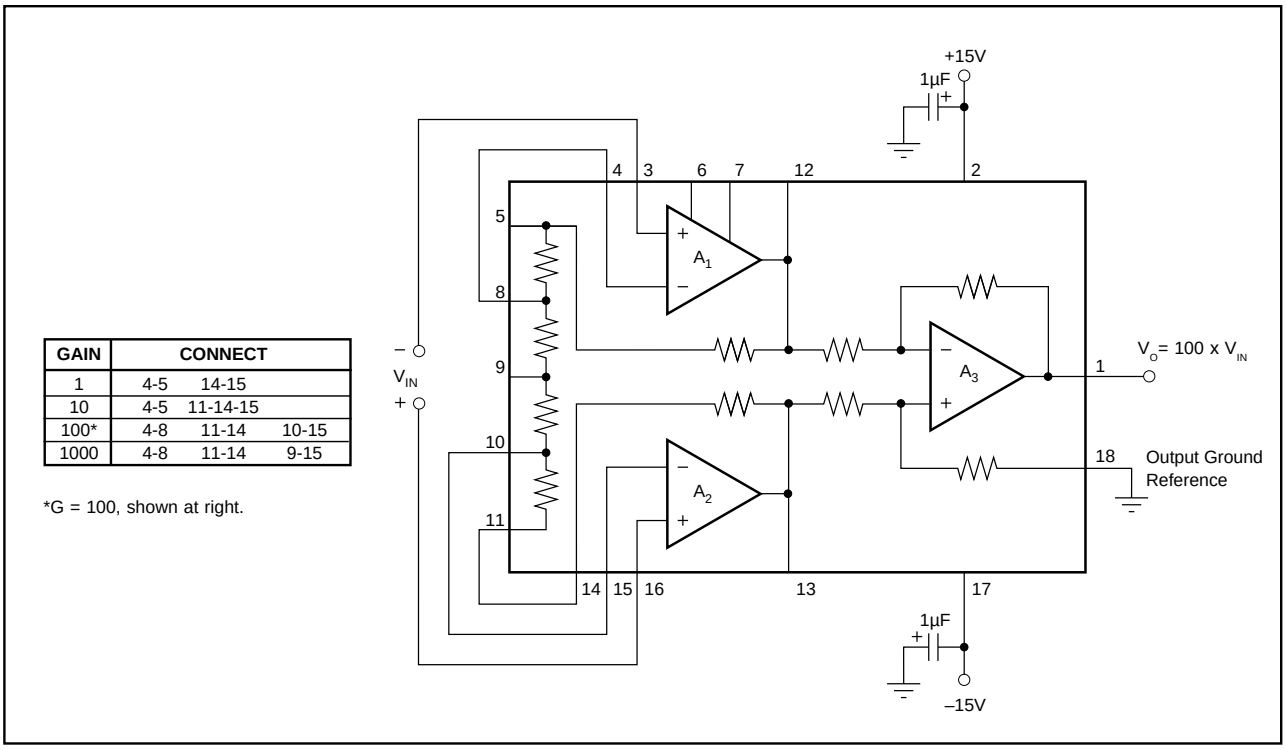
OFFSET TRIMMING

Many applications require no external offset voltage trimming. Figure 4 shows optional circuits for trimming offset voltage. Since the INA120 has two amplification stages, the offset voltage is comprised of two components—the input stage offset and output stage offset.

The input stage offset is equal to the combined offset of op amps A_1 and A_2. This input stage offset dominates at high gain. When used in gains of 100 to 1000, it is often sufficient to adjust the input stage offset with a potentiometer connected to pins 6 and 7 as shown. Connect both inputs to ground and adjust for 0V at the output, pin 1. Do not use pins 6 and 7 to trim offset voltage at G = 1 or to correct for offset in devices following the INA120 since this can cause excessive offset voltage drift.

At G = 1, offset is dominated by the output stage. Output stage offset can be trimmed by applying a correction voltage at the output reference terminal, pin 18. Low impedance must be maintained at this node to preserve the high CMR of the INA120. This is achieved by buffering the trim voltage with an op amp as shown.

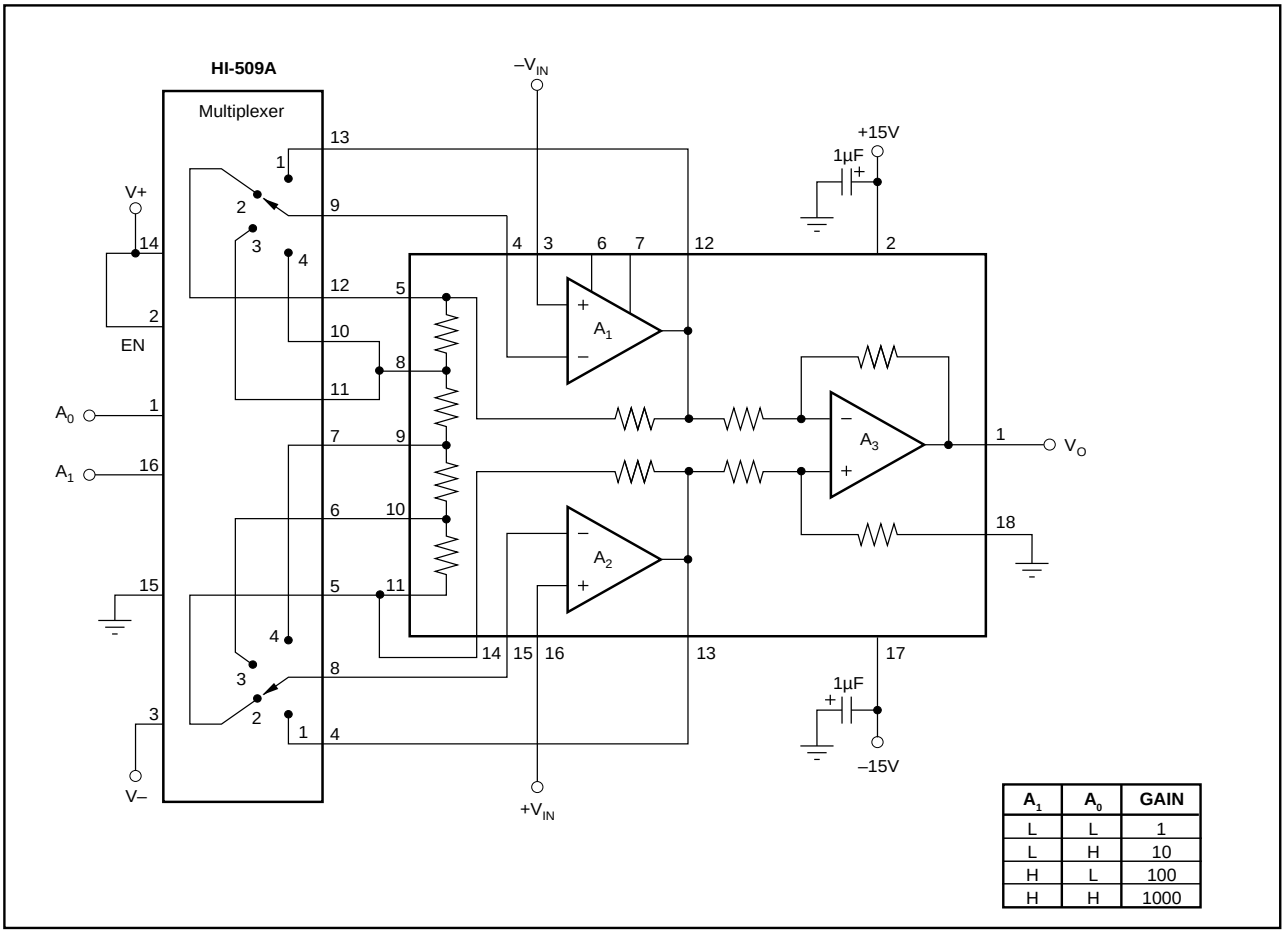
At intermediate gains it may be necessary to provide both input stage and output stage offset adjustments. Again, ground both inputs. Connect a jumper between pins 9 and 11 (temporarily connects the INA120 in high gain) and adjust R_1 for 0V at the output, pin 1. Then disconnect the jumper and adjust the output offset control for 0V output.



GAIN	CONNECT		
1	4-5	14-15	
10	4-5	11-14-15	
100*	4-8	11-14	10-15
1000	4-8	11-14	9-15

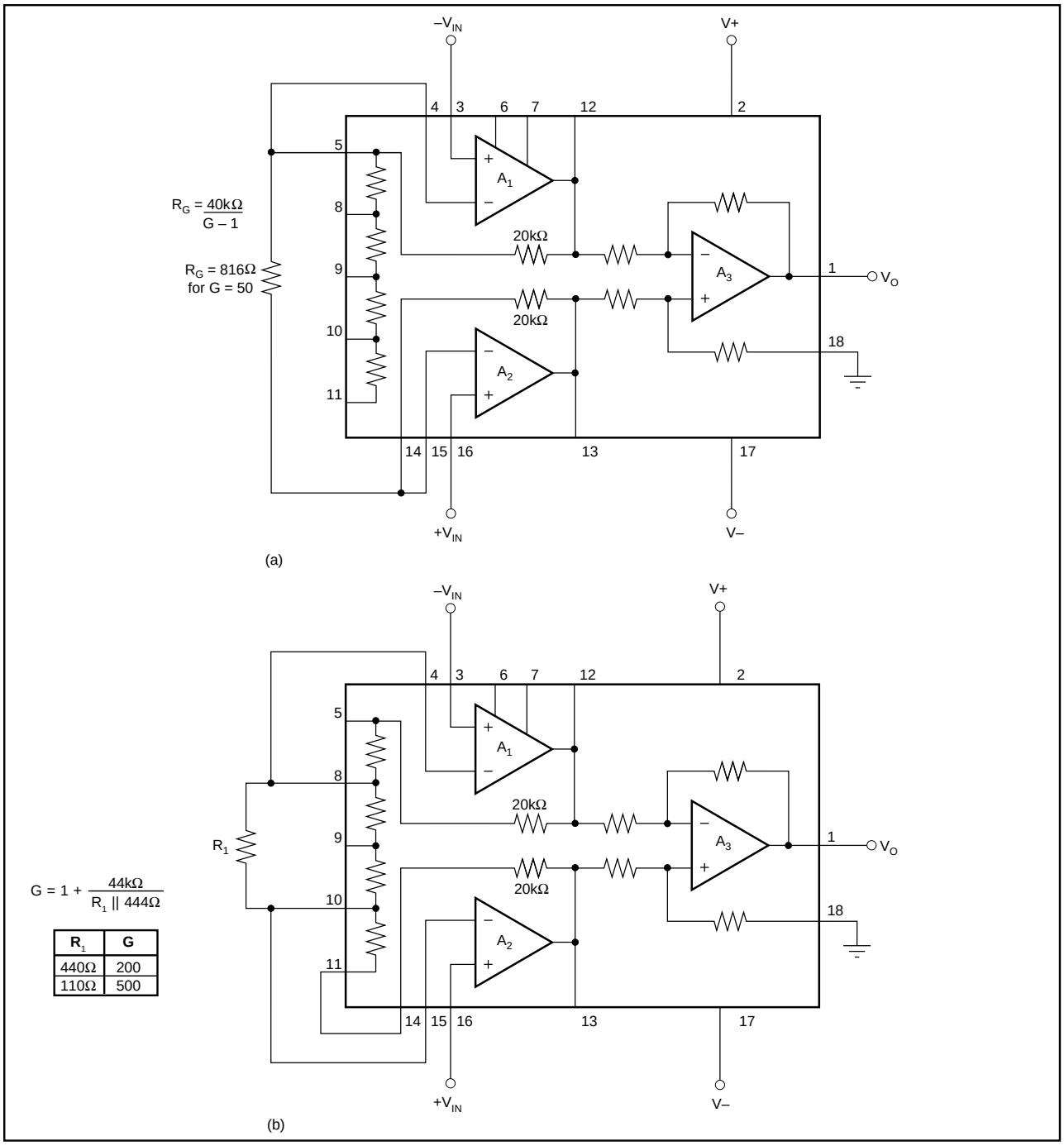
*G = 100, shown at right.

FIGURE 1. Basic Connection.



A_1	A_0	GAIN
L	L	1
L	H	10
H	L	100
H	H	1000

FIGURE 2. Digital Gain Control.



R_1	G
440Ω	200
110Ω	500

FIGURE 3. External Gain-Setting Resistors.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA120 is extremely high—approximately $10^{10}\Omega$. This does not mean, however, that no current flows in the input terminals. The input bias current of the INA120 is typically ±10nA (it can be either polarity). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA120 is to function. Figure 5 shows various provisions for an input bias current path. Without an appropriate current path, the inputs will float to a potential which exceeds the common-mode range of the INA120 and the input amplifiers will saturate.

INPUT PROTECTION

The inputs of the INA120 are protected for input voltages up to 2V beyond the power supply voltages. If the input can exceed these conditions, input clamp diodes should be provided as shown in Figure 6. R_S may not be required if the input cannot supply more than 100mA. If the input can supply larger currents, choose R_S according to the maximum source voltage, limiting current to under 100mA.

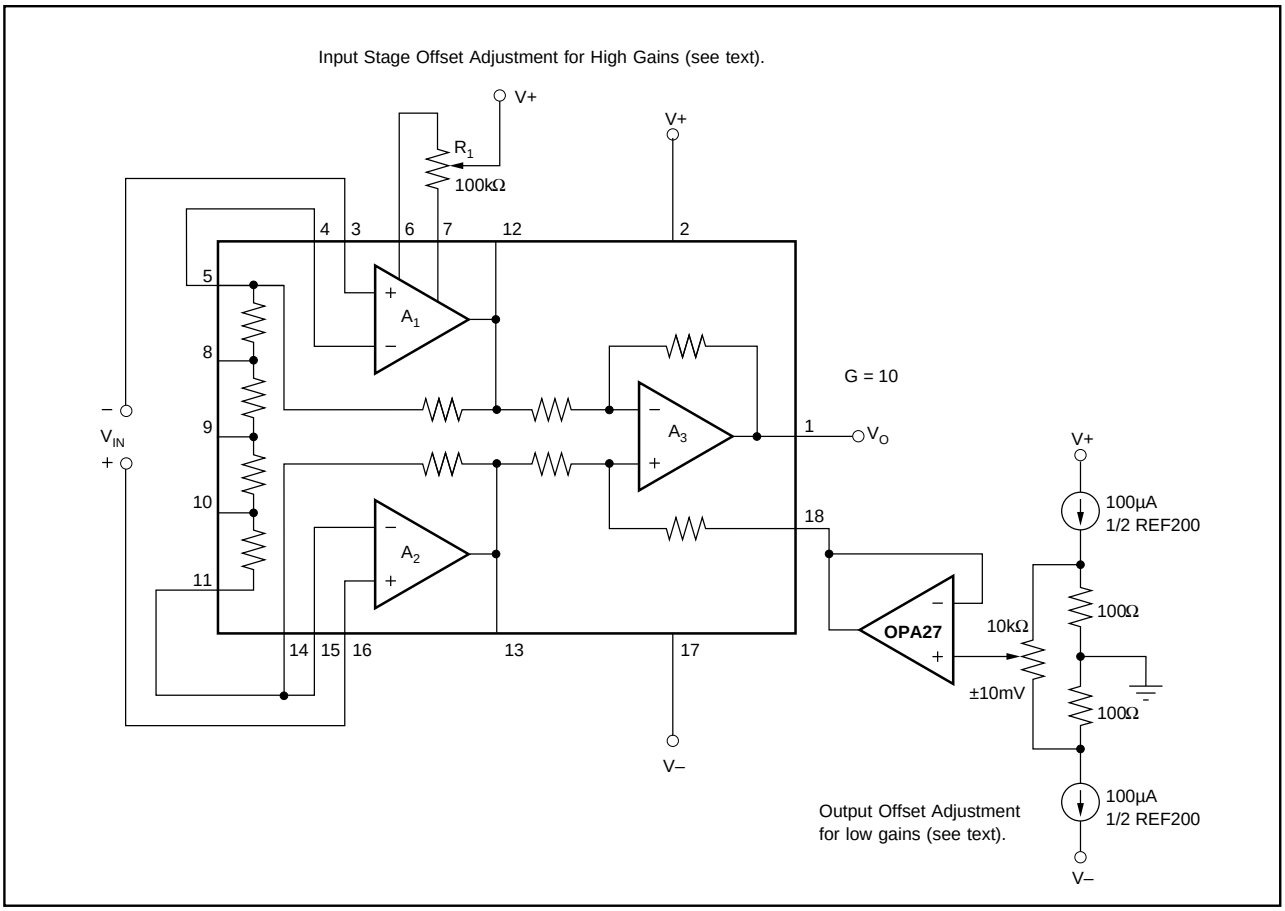


FIGURE 4. Offset Adjustment Circuits.

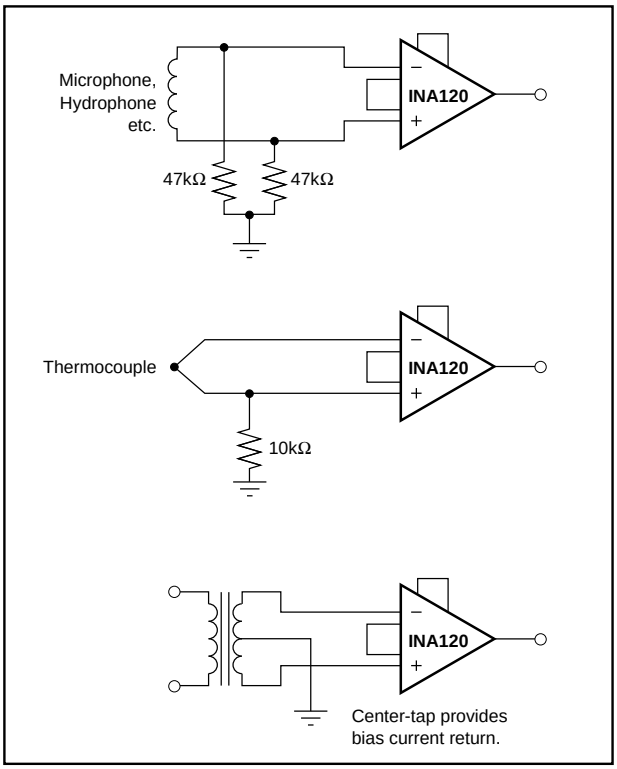


FIGURE 5. Providing an Input Bias Current Path.

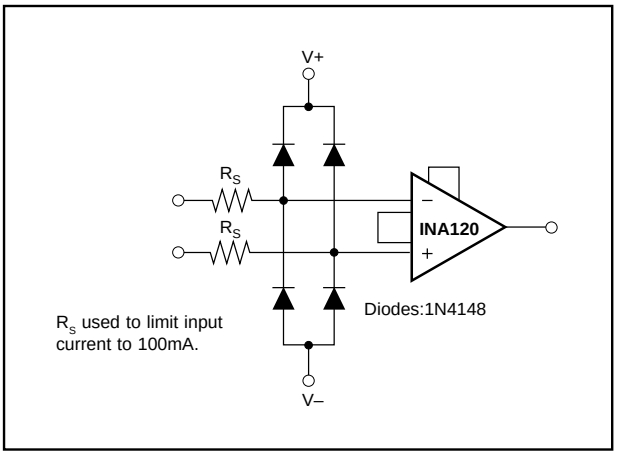
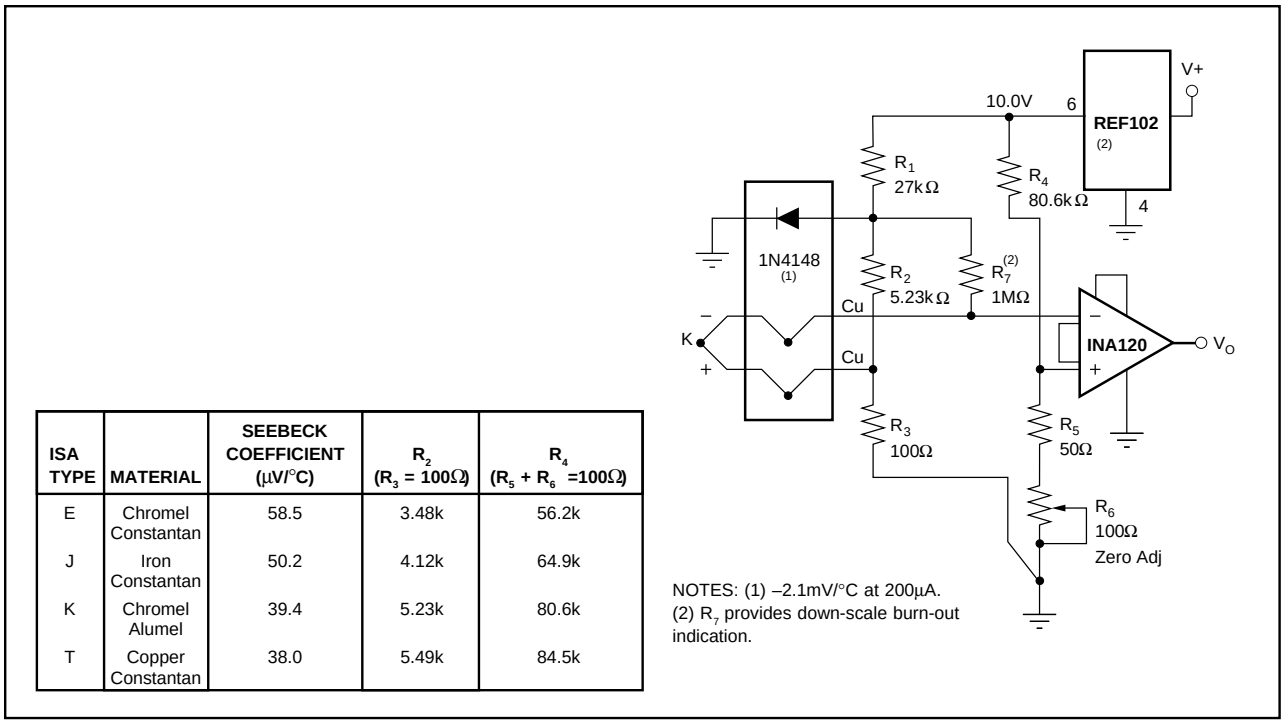


FIGURE 6. Input Protection Circuit.



ISA TYPE	MATERIAL	SEEBECK COEFFICIENT (µV/°C)	R_2 (R_3 = 100Ω)	R_4 (R_5 + R_6 =100Ω)
E	Chromel Constantan	58.5	3.48k	56.2k
J	Iron Constantan	50.2	4.12k	64.9k
K	Chromel Alumel	39.4	5.23k	80.6k
T	Copper Constantan	38.0	5.49k	84.5k

NOTES: (1) –2.1mV/°C at 200µA.
(2) R_7 provides down-scale burn-out indication.

FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.

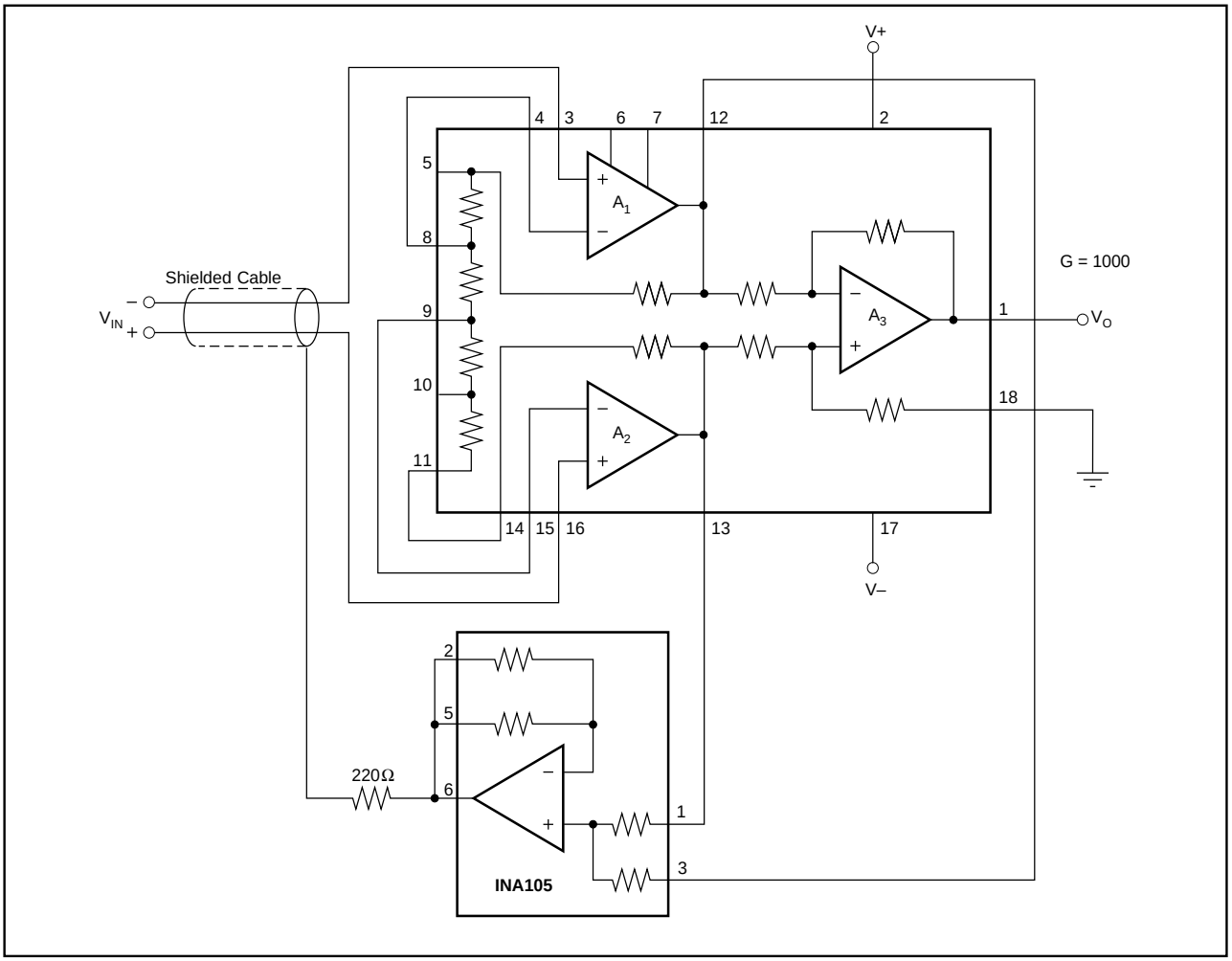
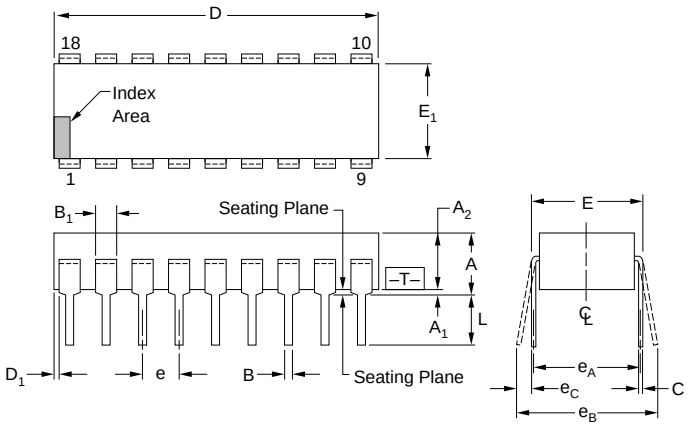


FIGURE 8. Guard Drive Circuit.

MECHANICALS

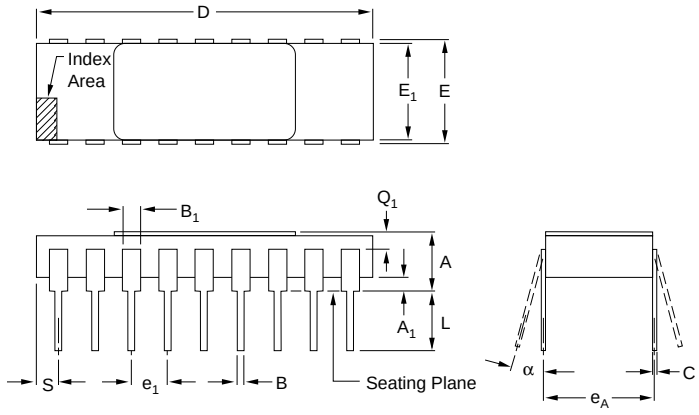
Package Number 218 — 18-Pin Plastic Single-Wide DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A (3)	—	.210	—	5.33
A_1 (3)	.015	—	0.38	—
A_2	.115	.195	2.92	4.95
B	.014	.022	0.36	0.56
B_1	.045	.070	1.14	1.78
C	.008	.015	0.20	0.38
D (4)	.845	.925	21.46	23.50
D_1	.005	—	0.13	—
E (5)	.300	.325	7.62	8.26
E_1 (4)	.240	.280	6.10	7.11
e	.100 BASIC		2.54 BASIC	
e_A (5)	.300 BASIC		7.63 BASIC	
e_B (6)	—	.430	—	10.92
L (3)	.115	.160	2.92	4.06
N (7)	18		18	

NOTES: (1) Controlling Dimension: Inch. In case of conflict between the English and metric dimensions, the inch dimensions control.
(2) Dimensioning and tolerancing per ANSI Y14.5M–1982.
(3) Dimensions A, A_1, and L are measured with the package seated in JEDEC seating plane gauge GS-3.
(4) D and E_1 dimensions for plastic packages do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
(5) E and e_A measured with the leads constrained to be perpendicular to plane T.
(6) e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
(7) N is the maximum number of terminal positions.
(8) Corner leads (1, 9, 10, and 18) may be configured as shown in Figure 2.
(9) For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package center-lines

Package Number 158 — 18-Lead, Ceramic Side Braze DIP, .300 Row Spacing



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.105	.175	2.68	4.45
A_1	.025	.055	0.64	1.40
B	.015	.021	0.38	0.53
B_1	.038	.060	0.97	1.52
C	.008	.012	0.20	0.30
D	.880	.930	22.35	23.62
E	.290	.325	7.37	8.26
E_1	.280	.310	7.11	7.87
e_1	.100 TYPICAL		2.54 TYPICAL	
e_A	.300 TYPICAL		7.62 TYPICAL	
L	.125	.175	3.18	4.45
N	18		18	
Q_1	.010	—	0.25	—
S	.030	.065	0.76	1.65
α	0°	15°	0°	15°

NOTE: (1) Dimensioning and tolerancing per ANSI Y14.5-1973.
(2) Leads within .13mm (.005in) radius of true position (TP) with maximum material condition.
(3) α applies to spread leads prior to installation.
(4) N is the number of terminal positions.
(5) Outlines on which the seating plane is coincident with the base plane (A_1 = 0), terminals lead standoffs are not required, and B_1 may equal B along any part of the lead above the seating/base plane.
(6) E_1 does not include particles of packing material.
(7) Controlling dimension: Inch.