



FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT74FCT299/A/C

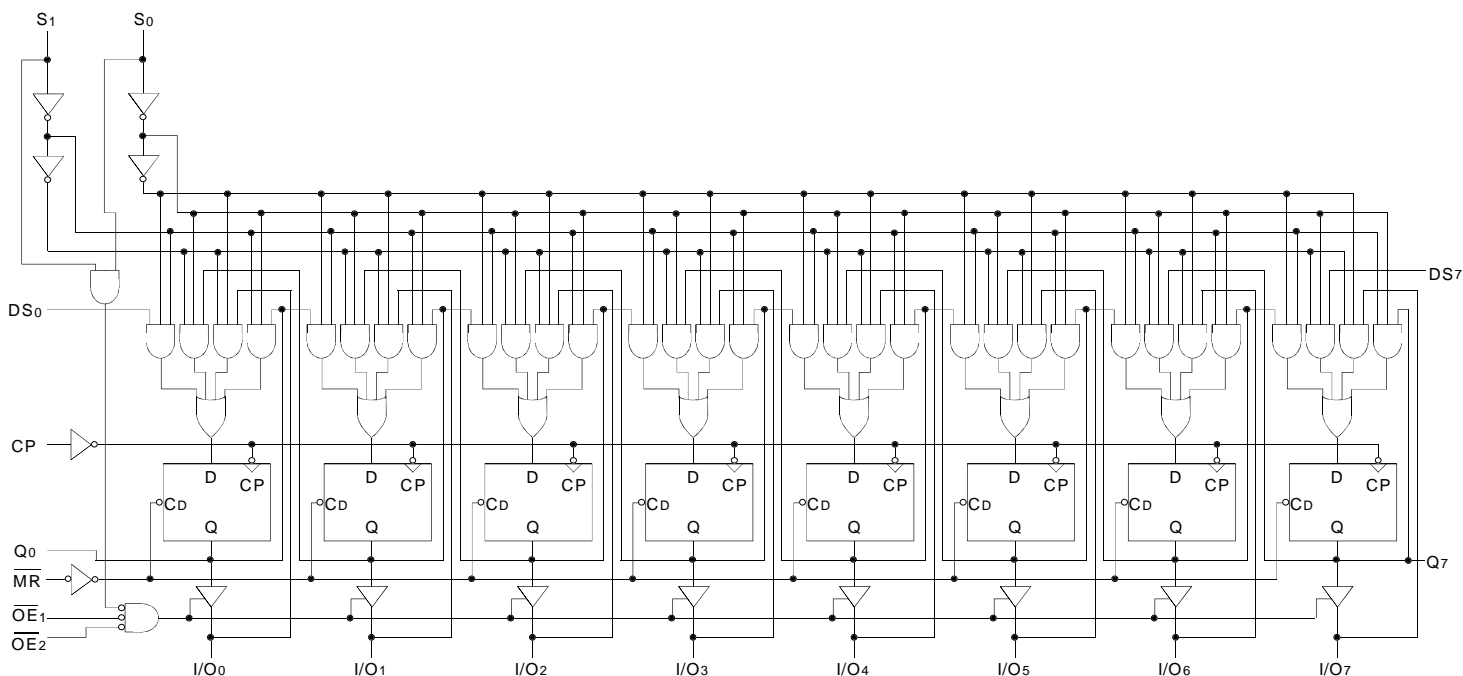
FEATURES:

- IDT74FCT299 equivalent to FAST™ speed and drive
- ID74FCT299A 25% faster than FAST
- IDT74FCT299C 35% faster than FAST
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- 8-input universal shift register

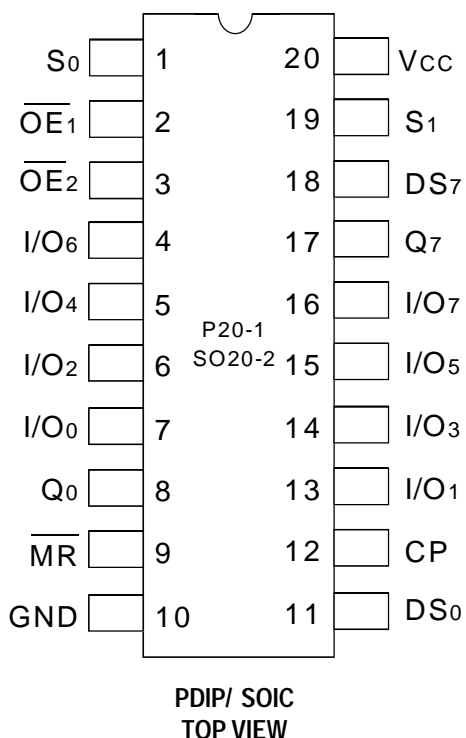
DESCRIPTION:

The IDT74FCT299 and IDT74FCT299A/C are built using an advanced dual metal CMOS technology. The IDT74FCT299 and IDT74FCT299A/C are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q0 and Q7 to allow easy serial cascading. A separate active low Master Reset is used to reset the register.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	0.5	W
I _{OUT}	DC Output Current	120	mA

8-link

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS ₀	Serial Data Input for Right Shift
DS ₇	Serial Data Input for Left Shift
S ₀ , S ₁	Mode Select Inputs
\overline{MR}	Asynchronous Master Reset Input (Active LOW)
$\overline{OE1}$, $\overline{OE2}$	3-State Output Enable Inputs (Active LOW)
I/O ₀ – I/O ₇	Parallel Data Inputs or 3-State Parallel Outputs
Q ₀ , Q ₇	Serial Outputs

FUNCTION TABLE (1)

Inputs				Response
\overline{MR}	S ₁	S ₀	CP	
L	X	X	X	Asynchronous Reset Q ₀ –Q ₇ = LOW
H	H	H	↑	Parallel Load: I/O _n →Q _n
H	L	H	↑	Shift Right: DS ₀ →Q ₀ , Q ₀ →Q ₁ , etc.
H	H	L	↑	Shift Left: DS ₇ →Q ₇ , Q ₇ →Q ₆ , ect.
H	L	L	X	Hold

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH clock transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O Pins)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA
I_{IL}	Input LOW Current (Except I/O Pins)		$V_I = 2.7V$	—	—	$5^{(4)}$	
			$V_I = 0.5V$	—	—	$-5^{(4)}$	
I_{IH}	Input HIGH Current (I/O Pins Only)	$V_{CC} = \text{Max.}$	$V_I = GND$	—	—	-5	μA
			$V_I = V_{CC}$	—	—	15	
	$V_I = 2.7V$		—	—	$15^{(4)}$		
	$V_I = 0.5V$		—	—	$-15^{(4)}$		
I_{IL}	Input LOW Current (I/O Pins Only)	$V_{CC} = \text{Max.}$	$V_I = GND$	—	—	-15	μA
V_{IK}	Clamp Diode Voltage		$V_{CC} = \text{Min.}, I_N = -18mA$		—	-0.7	
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$		-60	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	—	
			$I_{OH} = -15mA$	2.4	4.3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$		—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND	$V_{LC}^{(4)}$	
			$I_{OL} = 48mA$	—	0.3	0.5	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} ≥ V _{HC} ; V _{IN} ≤ V _{LC}		—	0.2	1.5	mA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2 = GND$ $\overline{MR} = V_{CC}$ S ₀ = S ₁ = V _{CC} DS ₀ = DS ₁ = GND One Input Toggling 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC}	—	0.15	0.25	mA/MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = GND$ $\overline{MR} = V_{CC}$ S ₀ = S ₁ = V _{CC} DS ₀ = DS ₇ = GND One Bit Toggling at f _i = 5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	1.7	4	mA
			V _{IN} = 3.4V V _{IN} = GND	—	2.2	6	
		V _{CC} = Max. Outputs Open f _{CP} = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2 = GND$ $\overline{MR} = V_{CC}$ S ₀ = S ₁ = V _{CC} DS ₀ = DS ₇ = GND Eight Bits Toggling at f _i = 2.5MHz 50% Duty Cycle	V _{IN} ≥ V _{HC} V _{IN} ≤ V _{LC} (FCT)	—	4	7.8 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND	—	6.2	16.8 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH \cdot NT + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
 DH = Duty Cycle for TTL Inputs High
 NT = Number of TTL Inputs at DH
 I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

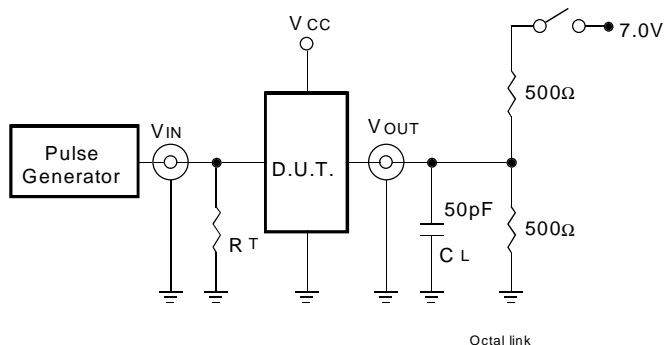
Symbol	Parameter	Condition ⁽¹⁾	IDT74FCT299		IDT74FCT299A		IDT74FCT299C		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay CP to Q ₀ or Q ₇	C _L = 50pF R _L = 500Ω	2	10	2	7.2	2	6.5	ns
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n		2	12	2	7.2	2	6.5	ns
t _{PHL}	Propagation Delay MR to Q ₀ or Q ₇		2	10	2	7.2	2	6.5	ns
t _{PHL}	Propagation Delay MR to I/O _n		2	15	2	8.7	2	6.5	ns
t _{PZH} t _{PZL}	Output Enable Time O _E _n to I/O _n		1.5	11	1.5	6.5	1.5	6.5	ns
t _{PHZ} t _{P LZ}	Output Disable Time O _E _n to I/O _n		1.5	7	1.5	6	1.5	6	ns
t _{SU}	Set-up Time HIGH or LOW S ₀ or S ₁ to CP		7.5	—	3.5	—	3.5	—	ns
t _H	Hold Time HIGH or LOW S ₀ or S ₁ to CP		1	—	1	—	1	—	ns
t _{SU}	Set-up Time HIGH or LOW I/O _n , DS ₀ or DS ₇ to CP		5.5	—	4	—	4	—	ns
t _H	Hold Time HIGH or LOW I/O _n , DS ₀ or DS ₇ to CP		1.5	—	1.5	—	1.5	—	ns
t _w	CP Pulse width HIGH or LOW		7	—	5	—	5	—	ns
t _w	MR Pulse Width LOW		7	—	5	—	5	—	ns
t _{REM}	Recovery Time MR to CP	7	—	5	—	5	—	ns	

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

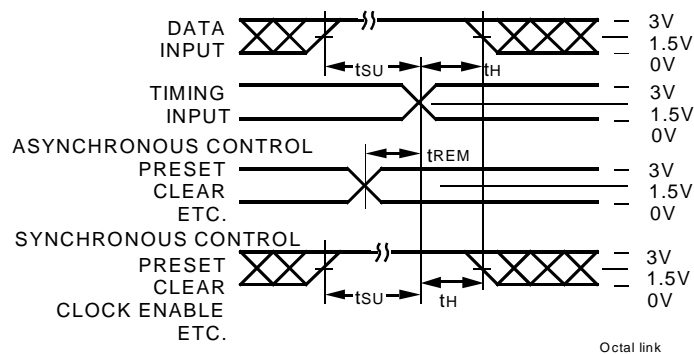
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

DEFINITIONS:

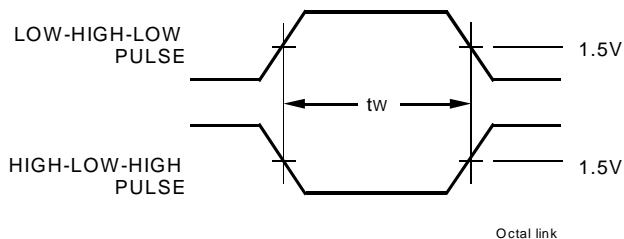
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

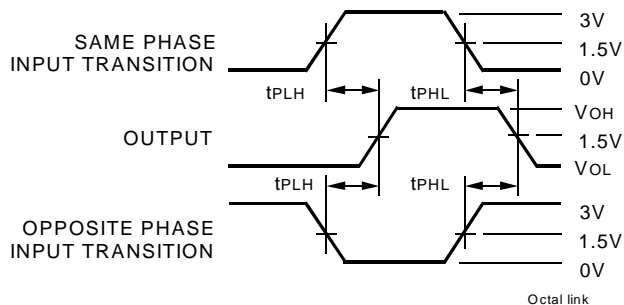
SET-UP, HOLD, AND RELEASE TIMES



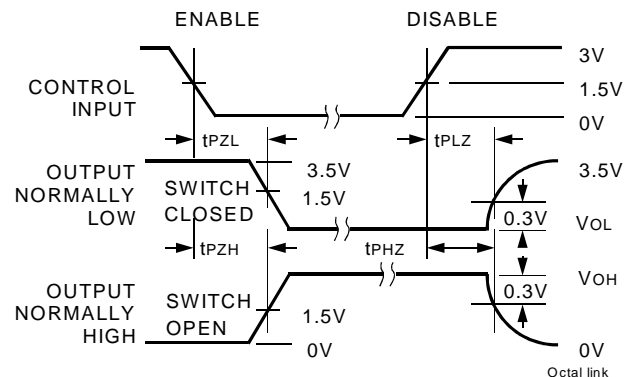
PULSE WIDTH



PROPAGATION DELAY



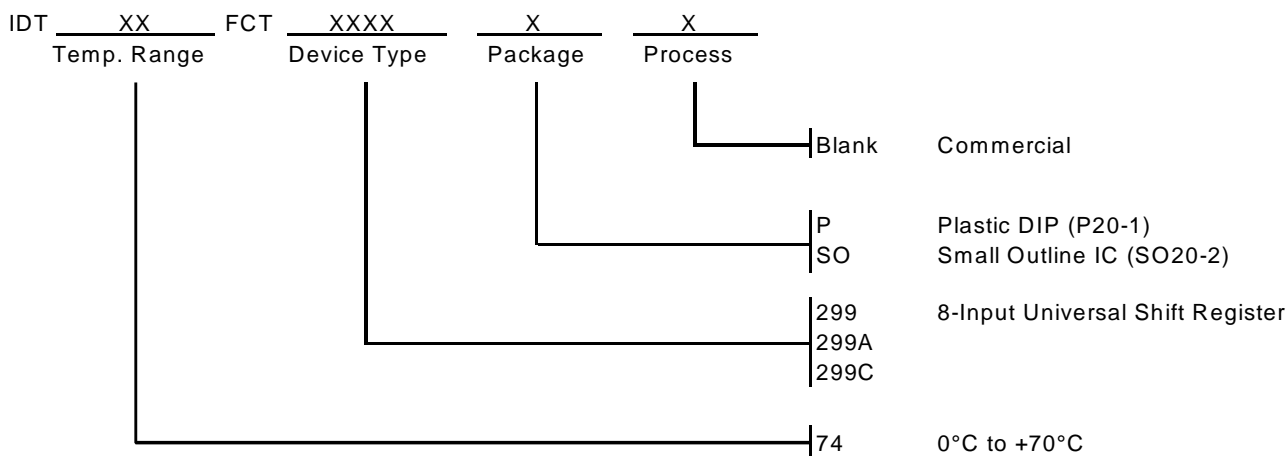
ENABLE AND DISABLE TIMES



NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o \leq 50\Omega$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.

ORDERING INFORMATION



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