

### Features

- High Frequency Counting - Guaranteed 15MHz, Typically 25MHz at 5V
- Low Power Operation - Typically Less Than 100µW Quiescent
- **STORE** and **RESET** Inputs Permit Operation as Frequency or Period Counter
- True **COUNT INHIBIT** Disables First Counter Stage
- **CARRY** Output for Cascading Four-Digit Blocks
- Schmitt-Trigger on the **COUNT** Input Allows Operation in Noisy Environments or with Slowly Changing Inputs
- Leading Zero Blanking **IN**put and **OUT**put for Correct Leading Zero Blanking with Cascaded Devices
- Provides Complete Onboard Oscillator and Divider Chain to Generate Backplane Frequency, or Backplane Driver May be Disabled Allowing Segments to be Slaved to a Master Backplane Signal

### Description

The ICM7224 device is a high-performance, CMOS 4<sup>1</sup>/<sub>2</sub> digit counter, including decoder, output latch, display driver, count inhibit, leading zero blanking, and reset circuitry.

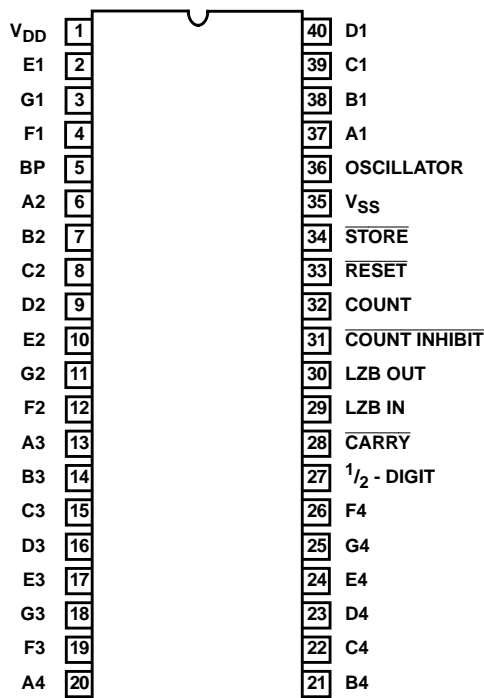
The counter section provides direct static counting, guaranteed from DC to 15MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25MHz. The **COUNT** input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. The **COUNT INHIBIT**, **STORE** and **RESET** inputs allow a direct interface with the ICM7207 and ICM7207A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The **CARRY** output allows the counter to be cascaded, while the Leading Zero Blanking **IN**put and **OUT**put allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display.

These devices provide maximum count of 19999. The display drivers are not of the multiplexed type and each display segment has its own individual drive pin, providing high quality display outputs.

### Pinout

ICM7224  
(PDIP)  
TOP VIEW



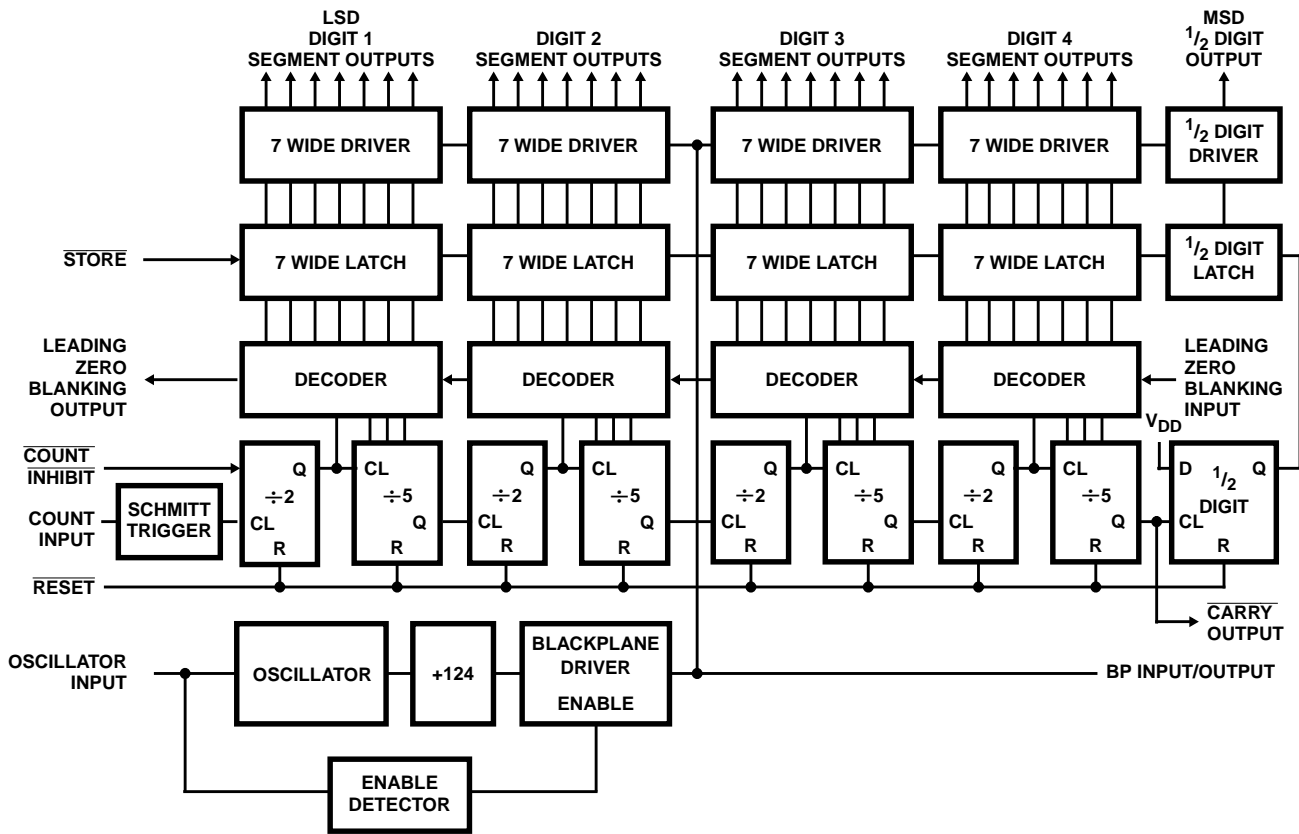
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ICM7224IPL	-25 to 85	40 Ld PDIP	E40.6
ICM7224RIPL †	-25 to 85	40 Ld PDIP	E40.6

† "R" Indicates Device With Reversed Leads Configuration.

# ICM7224

## Functional Block Diagram



# ICM7224

## Absolute Maximum Ratings

Supply Voltage ( $V_{DD} - V_{SS}$ ) ..... 6.5V  
 Input Voltage (Any Terminal) (Note 1) ..... ( $V_{DD} + 0.3V$ ) to ( $V_{SS} - 0.3V$ )

## Operating Conditions

Temperature Range ..... -25°C to 85°C

## Thermal Information

Thermal Resistance (Typical, Note 2) .....  $\theta_{JA}$  (°C/W)  
 PDIP Package ..... 50  
 Maximum Junction Temperature ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering, 10s) ..... 300°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than  $V_{DD}$  or less than  $V_{SS}$  may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224 be turned on first.
2.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications $V_{DD} = 5V, V_{SS} = 0V, T_A = 25^\circ C$ , Unless Otherwise Indicated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current, $I_{DD}$	Test Circuit, Display Blank	-	10	50	$\mu A$
Operating Supply Voltage Range ( $V_{DD} - V_{SS}$ ), $V_{SUPPLY}$		3	-	6	V
OSCILLATOR Input Current, $I_{OSCI}$	Pin 36	-	$\pm 2$	$\pm 10$	$\mu A$
Segment Rise/Fall Time, $t_r, t_f$	$C_{LOAD} = 200pF$	-	0.5	-	$\mu s$
BackPlane Rise/Fall Time, $t_r, t_f$	$C_{LOAD} = 5000pF$	-	1.5	-	$\mu s$
Oscillator Frequency, $f_{OSC}$	Pin 36 Floating	-	19	-	kHz
Backplane Frequency, $f_{BP}$	Pin 36 Floating	-	150	-	Hz
Input Pullup Currents, $I_p$	Pins 29, 31, 33, 34, $V_{IN} = V_{DD} - 3V$	-	10	-	$\mu A$
Input High Voltage, $V_{IH}$	Pins 29, 31, 33, 34	3	-	-	V
Input Low Voltage, $V_{IL}$	Pins 29, 31, 33, 34	-	-	1	V
$\overline{COUNT}$ Input Threshold, $V_{CT}$		-	2	-	V
$\overline{COUNT}$ Input Hysteresis, $V_{CH}$		-	0.5	-	V
Output High Current, $I_{OH}$	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 $V_{OUT} = V_{DD} - 3V$	-350	-500	-	$\mu A$
Output Low Current, $I_{OL}$	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 $V_{OUT} = +3V$	350	500	-	$\mu A$
Count Frequency, $f_{COUNT}$	$4.5V < V_{DD} < 6V$	0	-	15	MHz
$\overline{STORE}, \overline{RESET}$ Minimum Pulse Width, $t_S, t_F$		3	-	-	$\mu s$

## Timing Waveforms

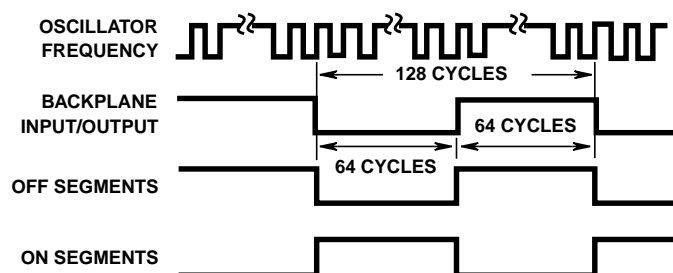


FIGURE 1. ICM7224 DISPLAY WAVEFORMS

Typical Performance Curves

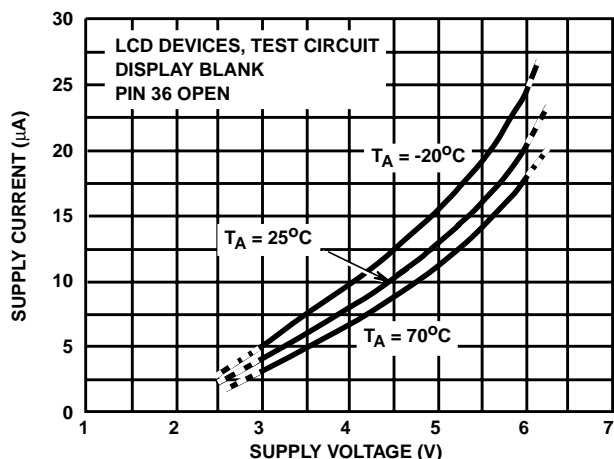


FIGURE 2. OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

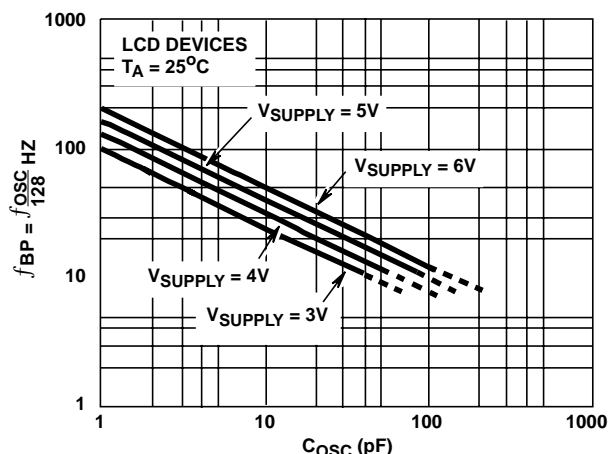


FIGURE 3. BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR C<sub>OSC</sub>

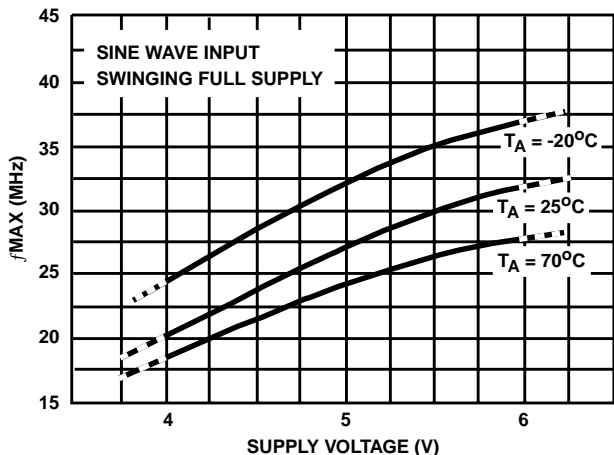


FIGURE 4. MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE

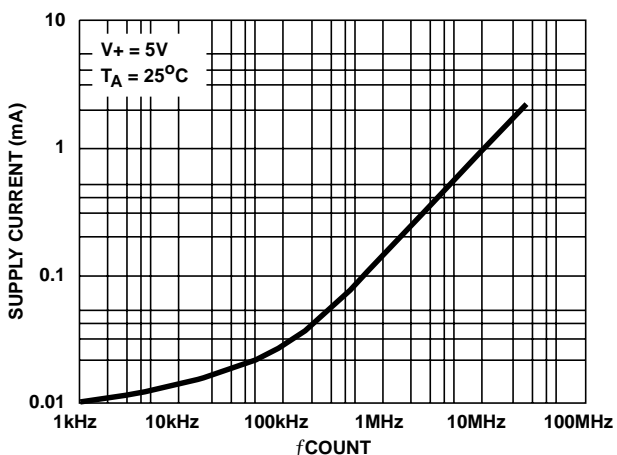


FIGURE 5. SUPPLY CURRENT AS A FUNCTION OF COUNT FREQUENCY

TABLE 1. CONTROL INPUT DEFINITIONS

TERMINAL	INPUT	VOLTAGE	FUNCTION
29	Leading Zero Blanking Input	V <sub>DD</sub> or Floating	Leading Zero Blanking Enabled
		V <sub>SS</sub>	Leading Zeroes Displayed
31	COUNT INHIBIT	V <sub>DD</sub> or Floating	Counter Enabled
		V <sub>SS</sub>	Counter Disabled
33	RESET	V <sub>DD</sub> or Floating	Inactive
		V <sub>SS</sub>	Counter Reset to 0000
34	STORE	V <sub>DD</sub> or Floating	Output Latches not Updated
		V <sub>SS</sub>	Output Latches Updated

## Control Input Definitions

In Table 1,  $V_{DD}$  and  $V_{SS}$  are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

## Detailed Description

The ICM7224 provides outputs suitable for driving conventional  $4\frac{1}{2}$  digit by seven segment LCD displays. It includes 29 individual segment drivers, a backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency (See Functional Block Diagram).

The segment and backplane drivers each consist of a CMOS inverter, with the N-Channel and P-Channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any DC component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output can be disabled by connecting the OSCILLATOR input (pin 36) to  $V_{SS}$ . This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption, is to keep the rise and fall times less than about 5 microseconds. The backplane driver of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5 $\mu$ s (i.e., 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external backplane signal should be capable of driving very large capacitive loads with short (1-2 $\mu$ s) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19kHz, at microampere power levels. The oscillator frequency is divided by 126 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and  $V_{DD}$ ; see the plot of oscillator/back-plane frequency in "Typical Performance Curves" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not

disabled during the negative portion of the overdriving signal (which could cause a DC component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

## Counter Section

The ICM7224 implements a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a CARRY output. Also included is an extra D-type flip-flop, clocked by the  $\overline{\text{CARRY}}$  signal which controls the half-digit segment driver. This output driver can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the COUNT input, while the  $\overline{\text{CARRY}}$  output provides a negative-going edge following the count which increments the counter from 9999 to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the  $\overline{\text{RESET}}$  terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent  $\overline{\text{CARRY}}$  outputs will not be affected.

A negative level at the  $\overline{\text{COUNT INHIBIT}}$  input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

Each decade of the counter directly drives a four-to-seven segment decoder which develops the required output data. The output data is latched at the driver. When the  $\overline{\text{STORE}}$  pin is low, these latches are updated, and when it is high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When it is low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

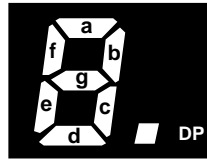
For example, in an eight-decade counter with overflow using two ICM7224 devices, the Leading Zero Blanking OUTput of the high order digit would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

The  $\overline{\text{STORE}}$ ,  $\overline{\text{RESET}}$ ,  $\overline{\text{COUNT INHIBIT}}$ , and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The  $\overline{\text{CARRY}}$  and Leading Zero Blanking OUTputs are suitable for

interfacing to CMOS logic in general, and are specifically designed to allow cascading of the devices in four-digit blocks.

**Applications**

Figure 8 shows an 8-digit precision frequency counter. The circuit uses two ICM7224s cascaded to provide an 8-digit display. Backplane output of the second device is disabled and is driven by the first device. The 1/2 digit output of the second device is used for overflow indication. The input signal is fed to the first device and the COUNT input of the second is driven by the CARRY output of the first. Notice that leading zero blanking is controlled on the second device and the LZB OUT of the second one is tied to LZB IN of the first one. An ICM7207A device is used as a timebase generator and frequency counter controller. It generates count window, store and reset signals which are directly compatible with ICM7224 inputs (notice the need for an inverter at COUNT INHIBIT input). The ICM7207A provides two count window signals (1s and 0.1s gating) for displaying frequencies in Hz or tens of Hz (x10Hz).



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FIGURE 7. SEGMENT ASSIGNMENT AND DISPLAY FONT

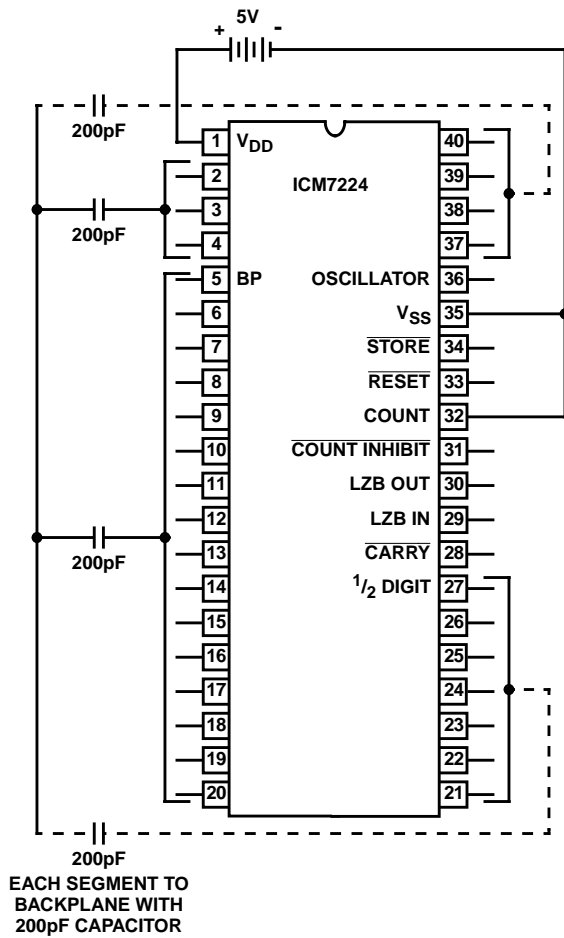


FIGURE 6. TEST CIRCUIT

# ICM7224

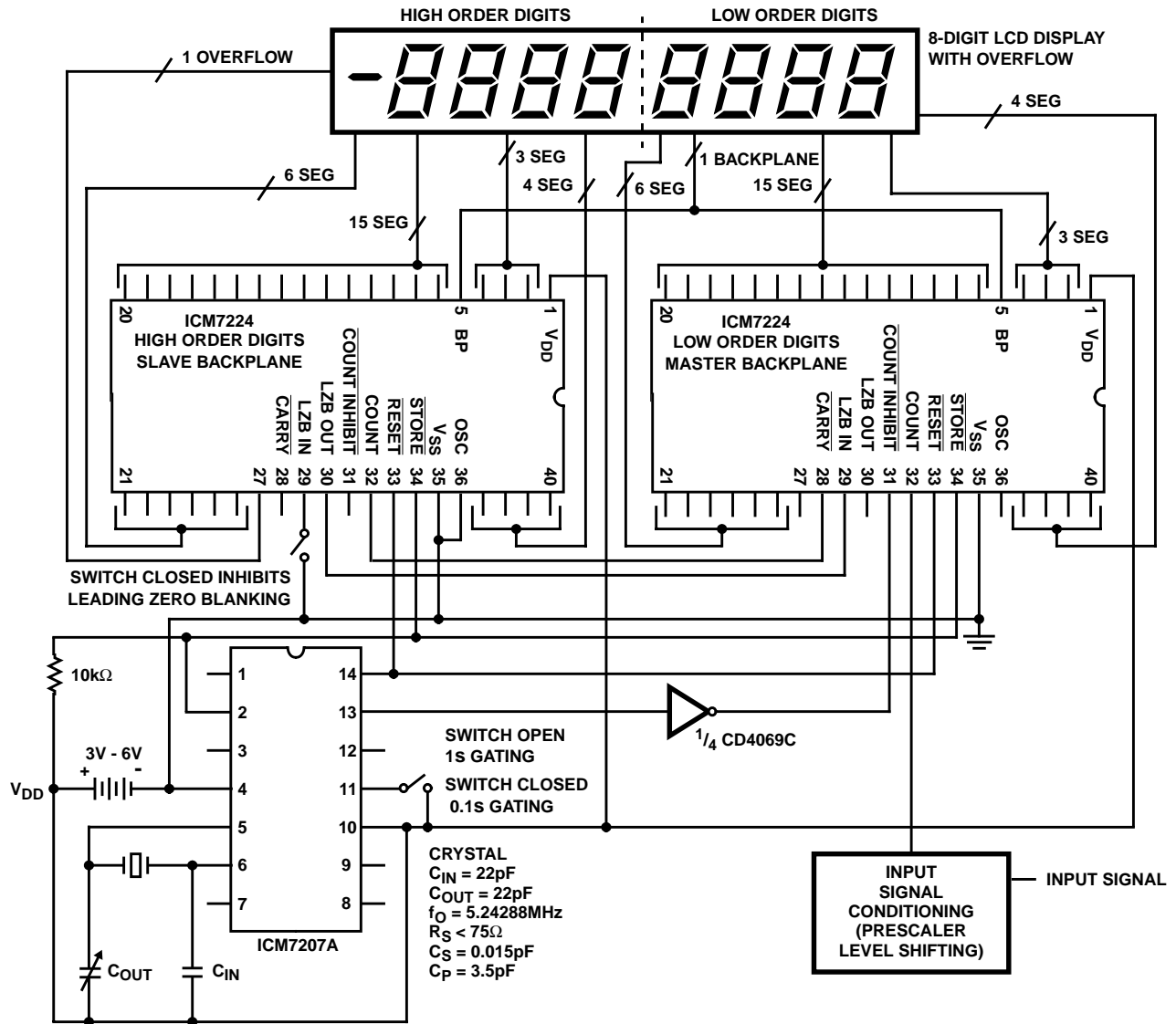


FIGURE 8. EIGHT-DIGIT PRECISION FREQUENCY COUNTER

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