



## SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTERS

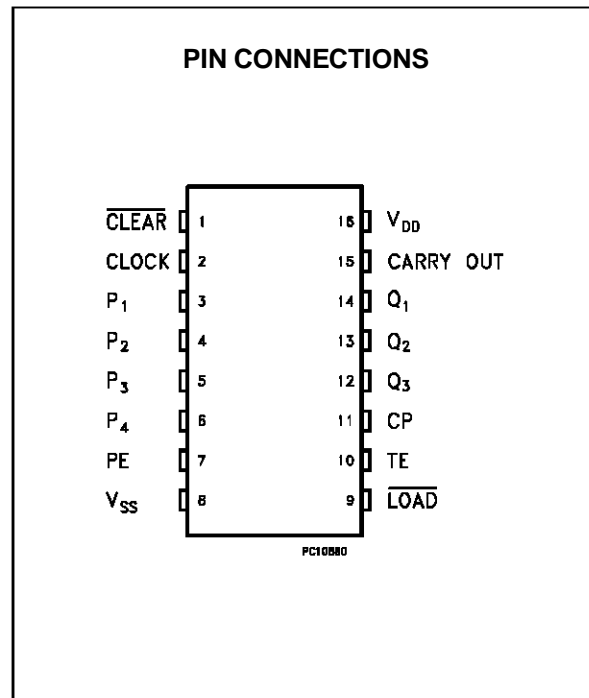
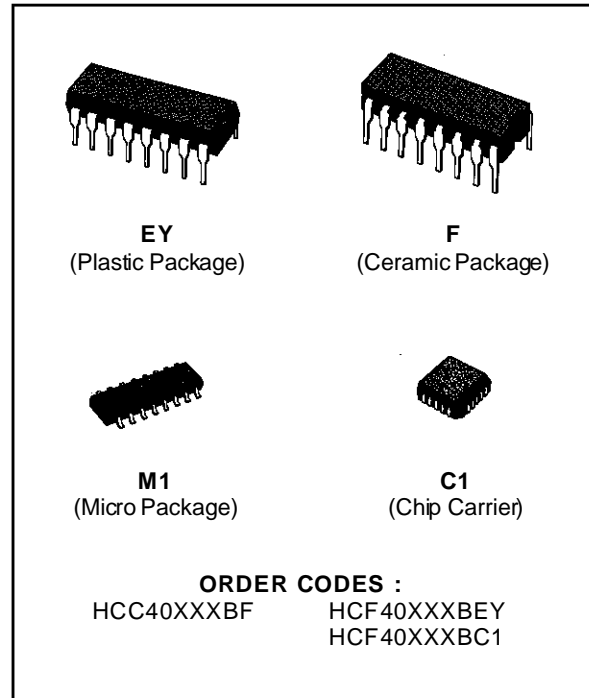
- 40160B - DECADE WITH ASYNCHRONOUS CLEAR**
- 40161B - BINARY WITH ASYNCHRONOUS CLEAR**
- 40162B - DECADE WITH SYNCHRONOUS CLEAR**
- 40163B - BINARY WITH SYNCHRONOUS CLEAR**

- INTERNAL LOOK-AHEAD FOR FAST COUNTING
- CARRY OUTPUT FOR CASCADING
- SYNCHRONOUSLY PROGRAMMABLE
- LOW-POWER TTL COMPATIBILITY
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100nA AT 18V AND 25oC FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD N. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

The **HCC40160B, 40161B, 40162B, 40163B** (extended temperature range) and **HCF40160B, 40161B, 40162B, 40163B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in line plastic or ceramic package and plastic micropackage.

**HCC/HCF40160B, 40161B, 40162B** and **40163B** are 4-bit synchronous programmable counters. The CLEAR function of the **HCC/HCF40162B** and **40163B** is synchronous and a low on the at the clear CLEAR input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the **HCC/HCF40160B** and **40161B** is asynchronous and a low level at the CLEAR input sets all four outputs low regardless of the state of the CLOCK, LOAD or ENABLE inputs. A low level at the LOAD input disables the counter and causes the output to agree with the set-up data after the next CLOCK pulse regardless of the conditions of the ENABLE in-



## HCC/HCF40160B-40161B-40162-40163

cascading counter for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable input and a carry output (COUT). Counting is enable when both PE and TE inputs are high. The TE input is fed forward to enable COUT. This enable output

produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

### ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
$V_{DD}^*$	Supply Voltage: <b>HCC Types</b> <b>HCF Types</b>	-0.5 to +20	V
		-0.5 to +18	V
$V_i$	Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_i$	DC Input Current (any one input)	$\pm 10$	mA
$P_{tot}$	Total Power Dissipation (per package)	200	mW
	Dissipation per Output Transistor for Top = Full Package Temperature Range	100	mW
$T_{op}$	Operating Temperature: <b>HCC Types</b> <b>HCF Types</b>	-55 to +125	°C
		-40 to +85	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

\* All voltage values are referred to  $V_{SS}$  pin voltage.

### RECOMMENDED OPERATING CONDITIONS

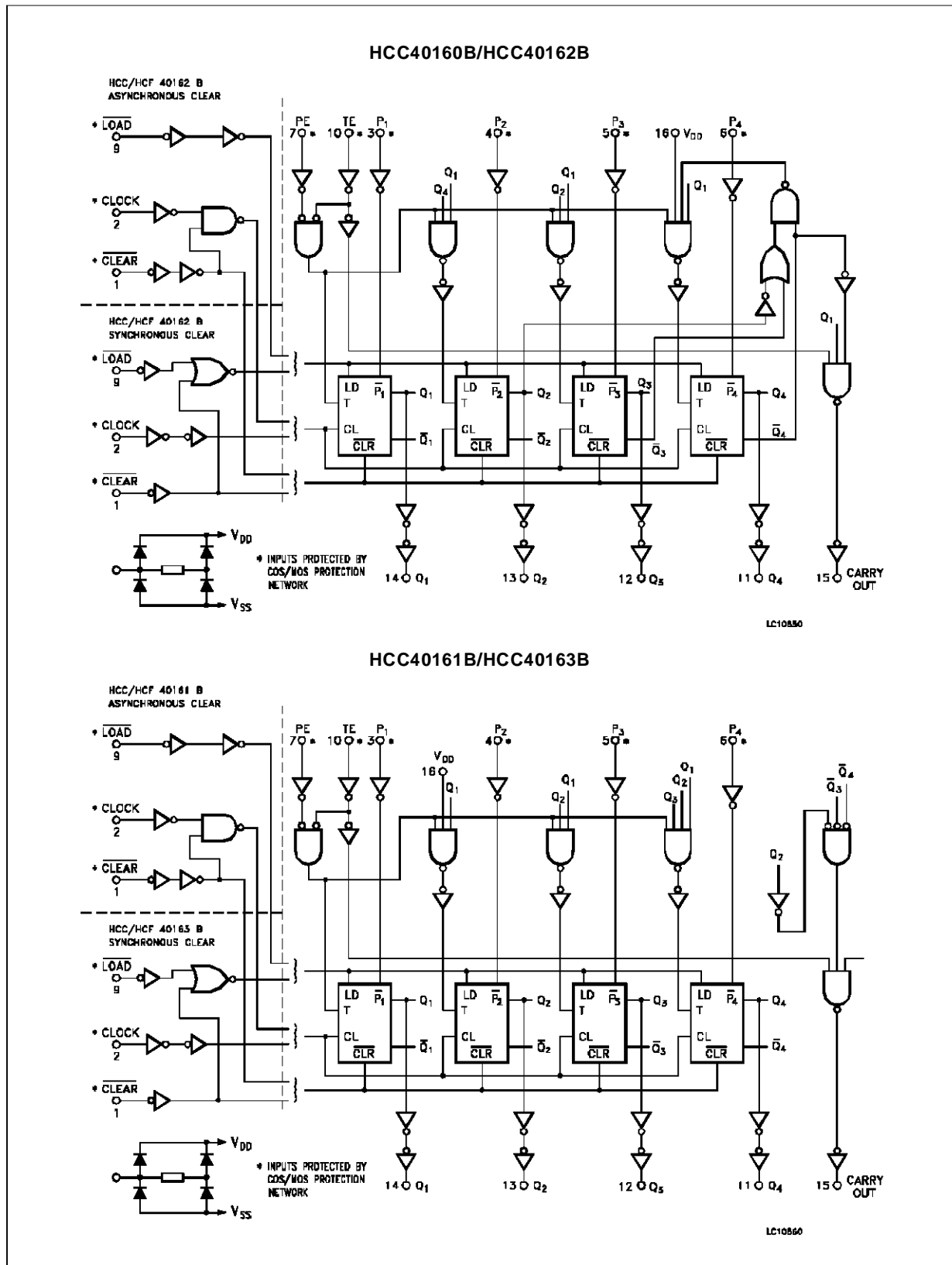
Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage: <b>HCC Types</b> <b>HCF Types</b>	3 to 18	V
		3 to 15	V
$V_i$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature: <b>HCC Types</b> <b>HCF Types</b>	-55 to +125	°C
		-40 to +85	°C

### TRUTH TABLE

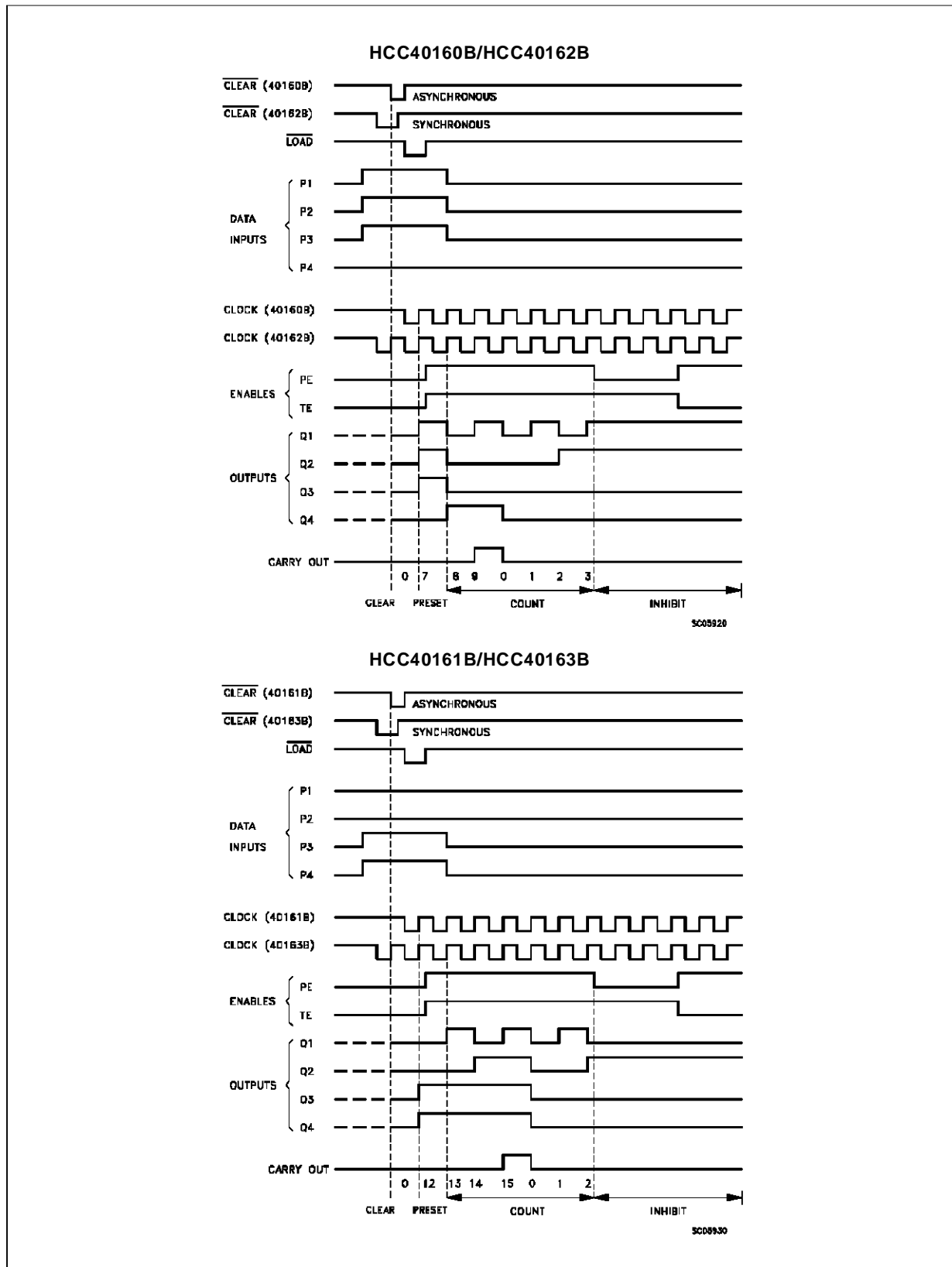
Clock	CLR	LOAD	PE	TE	Operation
	1	0	X	X	Preset
	1	1	0	X	NC
	1	1	X	0	NC
	1	1	1	1	Count
X	0	X	X	X	Reset (HCC/HCF40160B, HCC/HCF40161B)
	0	X	X	X	Reset (HCC/HCF40162B, HCC/HCF40163B)
	1	X	X	X	NC (HCC/HCF40162B, HCC/HCF40163B)

1 = HIGH LEVEL, 0 = LOW LEVEL, X = DON'T CARE, NC = NO CHANGE

LOGIC DIAGRAMS



TIMING DIAGRAMS



**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)

Symbol	Parameter		Test Conditions				Value						Unit	
			V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>LOW</sub> *		25 °C			T <sub>HIGH</sub> *		
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	HCC Types	0/5			5		5		0.04	5		150	$\mu$ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF Types	0/5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
V <sub>OH</sub>	Output High Voltage		0/5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V <sub>OL</sub>	Output Low Voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V <sub>IH</sub>	Input High Voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V <sub>IL</sub>	Input Low Voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I <sub>OH</sub>	Output Drive Current	HCC Types	0/5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF Types	0/5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I <sub>OL</sub>	Output Sink Current	HCC Types	0/5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF Types	0/5	0.4		5	0.53		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I <sub>IH</sub> , I <sub>IL</sub>	Input Leakage Current	HCC Types	0/18	Any Input		18		$\pm$ 0.1		$\pm$ 10 <sup>-5</sup>	$\pm$ 0.1		$\pm$ 1	$\mu$ A
		HCC Types	0/15											
C <sub>i</sub>	Input Capacitance			Any Input					5	7.5			pF	

\* T<sub>LOW</sub> = -55 °C for HCC device; -40 °C for HCF device.

\* T<sub>HIGH</sub> = +125 °C for HCC device; +85 °C for HCF device.

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub> = 5V, 2V min. with V<sub>DD</sub> = 10V, 2.5V min. with V<sub>DD</sub> = 15V

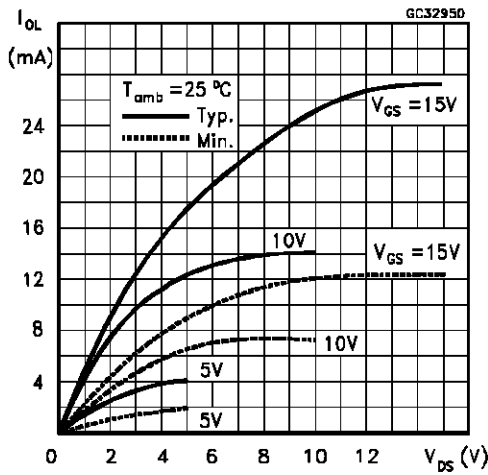
## HCC/HCF40160B-40161B-40162-40163

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ K}\Omega$ , typical temperature coefficient for all  $V_{DD}$  values is  $03\text{ } \%/^{\circ}\text{C}$ , all input rise and fall times =  $20\text{ ns}$ )

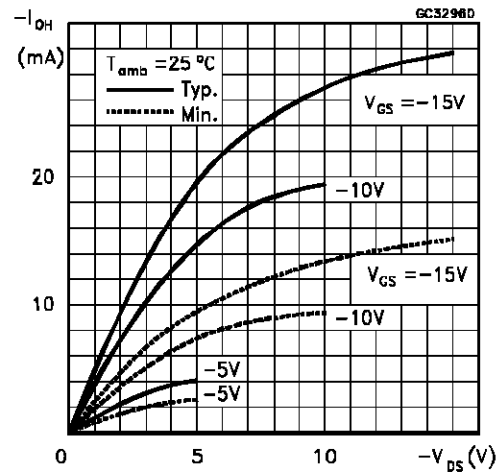
Symbol	Parameter	Test Conditions		Value			Unit
			$V_{DD}$ (V)	Min.	Typ.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time Clock to Q		5		200	400	ns
			10		80	160	
			15		60	120	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time Clock to $C_{OUT}$		5		225	450	ns
			10		95	190	
			15		70	140	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time TE to $C_{OUT}$		5		125	250	ns
			10		55	110	
			15		40	80	
$t_{setup}$	Setup Time Data to Clock		5	240	120		ns
			10	90	45		
			15	60	30		
$t_{setup}$	Setup Time Load to Clock		5	240	120		ns
			10	90	45		
			15	60	30		
$t_{setup}$	Setup Time PE or TE to Clock		5	340	170		ns
			10	140	70		
			15	100	50		
$t_{hold}$	Hold Time		5	0			ns
			10	0			
			15	0			
$t_{THL}$ $t_{TLH}$	Transition Time		5		100	200	ns
			10		50	100	
			15		40	80	
$t_w$	Clock Input Pulse Width		5	170	85		ns
			10	70	35		
			15	50	25		
$f_{CL}$	Maximum Clock Input Frequency		5	2	3		MHz
			10	5.5	8.5		
			15	8	12		
$t_r$ $t_f$	Clock Input Rise or Fall Time *					200	ns
						70	
						15	
$t_{PHL}$	Propagation Delay Time (40160B, 40161B) Clear to Q		5		250	500	ns
			10		110	220	
			15		80	160	
$t_{setup}$	Setup Time (40162B, 40163B) Clear to Clock		5	340	170		ns
			10	140	70		
			15	100	50		
$t_{hold}$	Hold Time (40162B, 40163B) Clear to Clock		5	0			ns
			10	0			
			15	0			
$t_{rem}$	Clear Removal Time (40162B, 40163B)		5	200	100		ns
			10	100	50		
			15	70	35		
$t_w$	Clear Input Pulse Width Low Level (40160B, 40161B)		5	170	85		ns
			10	70	35		
			15	50	25		

\* If more than one unit is cascaded in the parallel clocked application,  $t_r$  should be made less than or equal to the sum of the fixed propagation delay at  $50\text{ pF}$  and the transition time of the carry output driving stage for the estimated capacitance

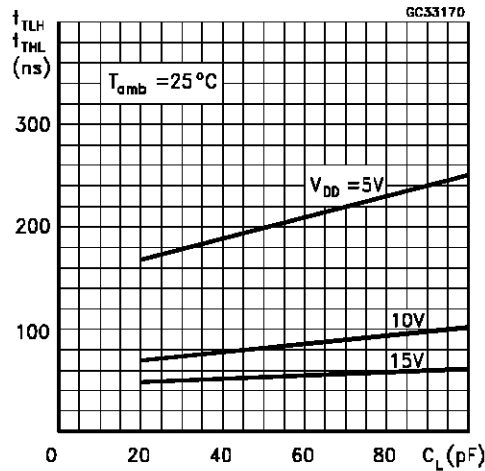
Output Low (sink) Current Characteristics



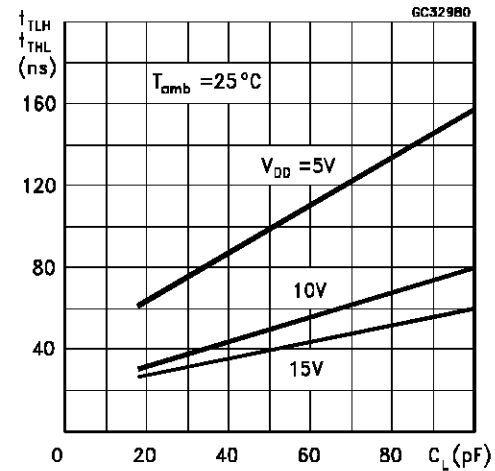
Output High (source) Current Characteristics



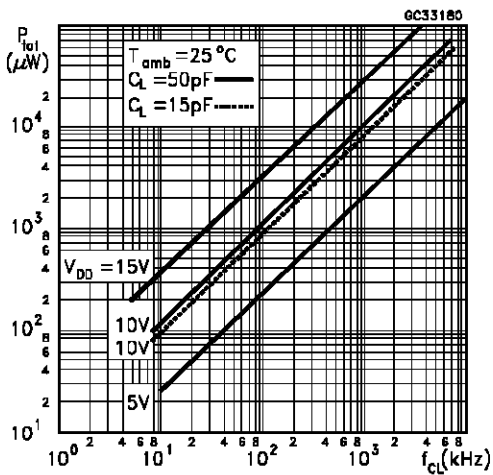
Typical Propagation Delay Time vs Load Capacitance



Typical Transition Time vs Load Capacitance

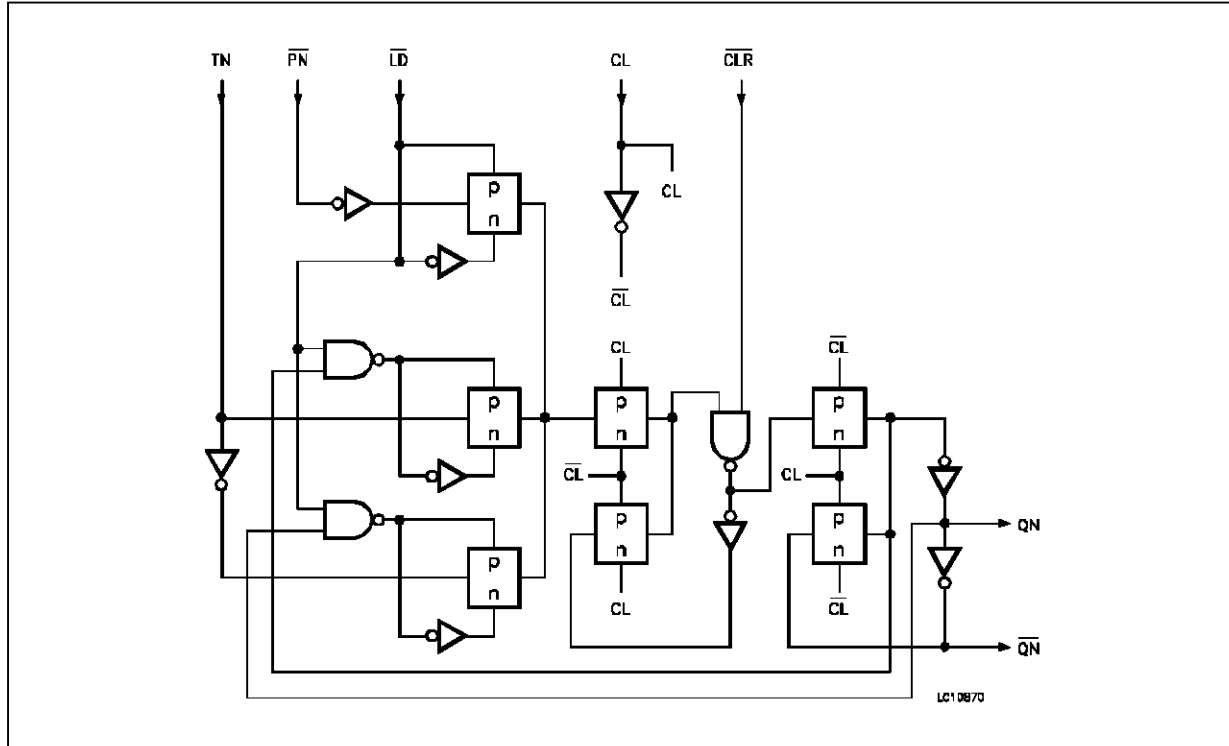


Typical Dynamic Power Dissipation vs Input Frequency

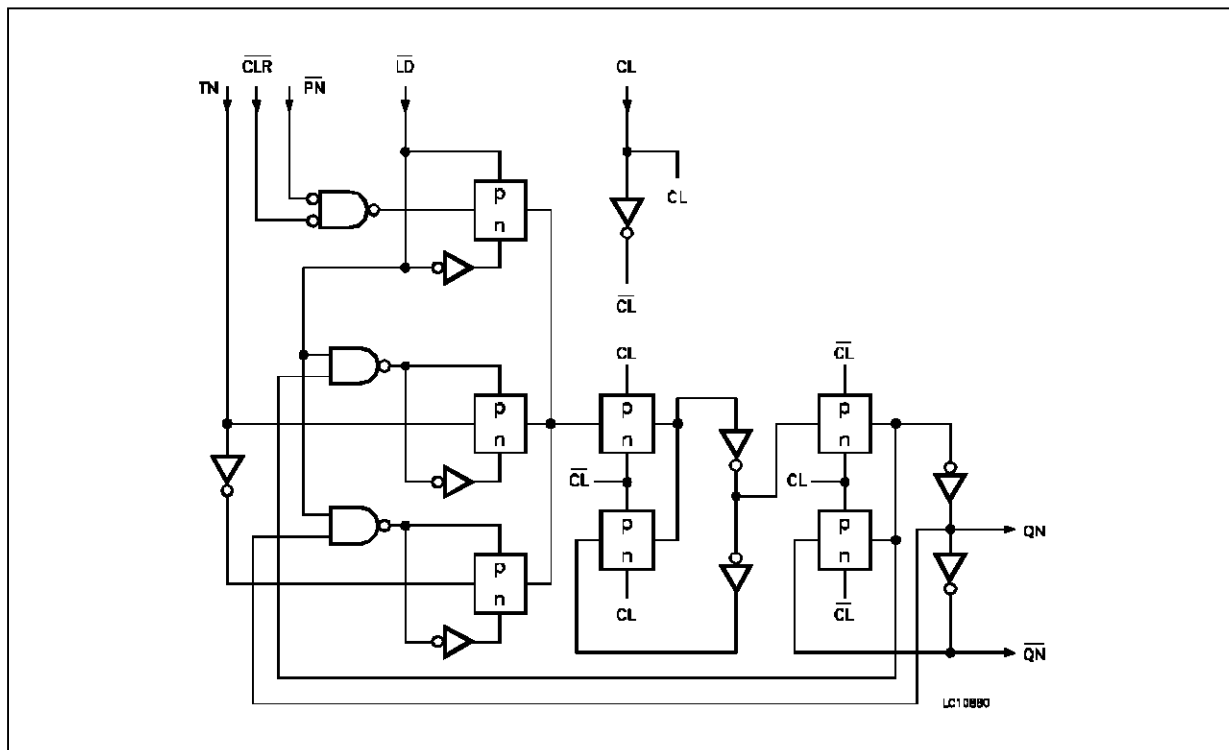


TYPICAL APPLICATIONS

Detail of Flip-flops For 40160B And 40161B (Asynchronous Clear)

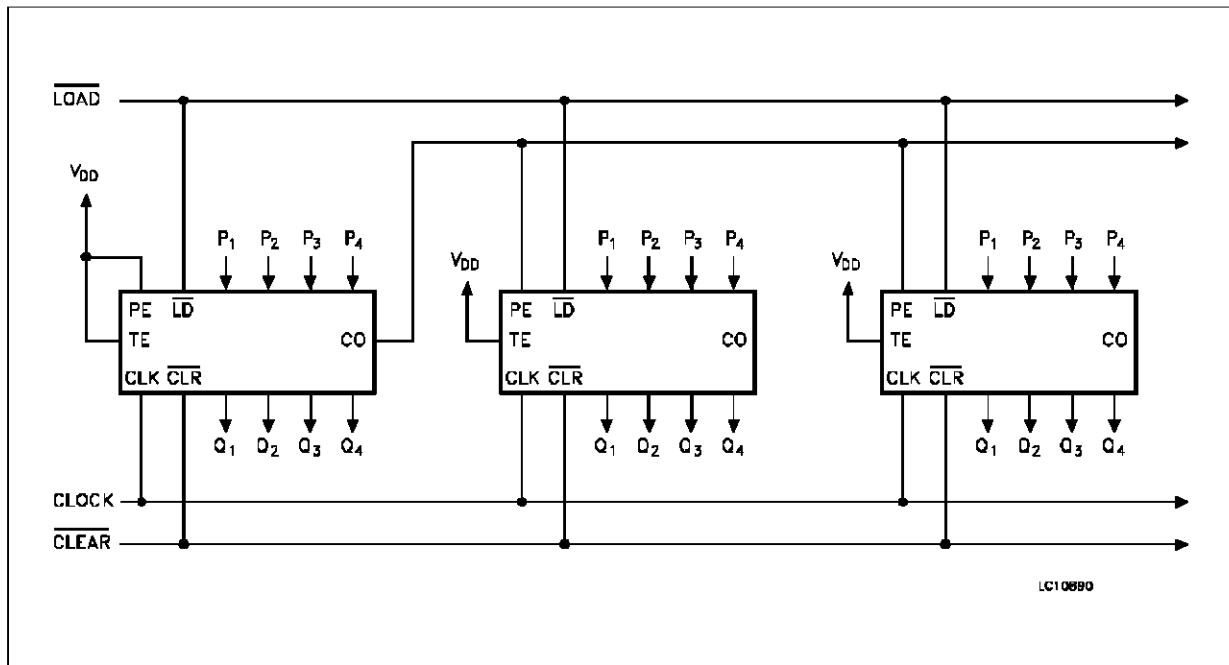


Detail of Flip-flops For 40162B And 40163B (Synchronous Clear)

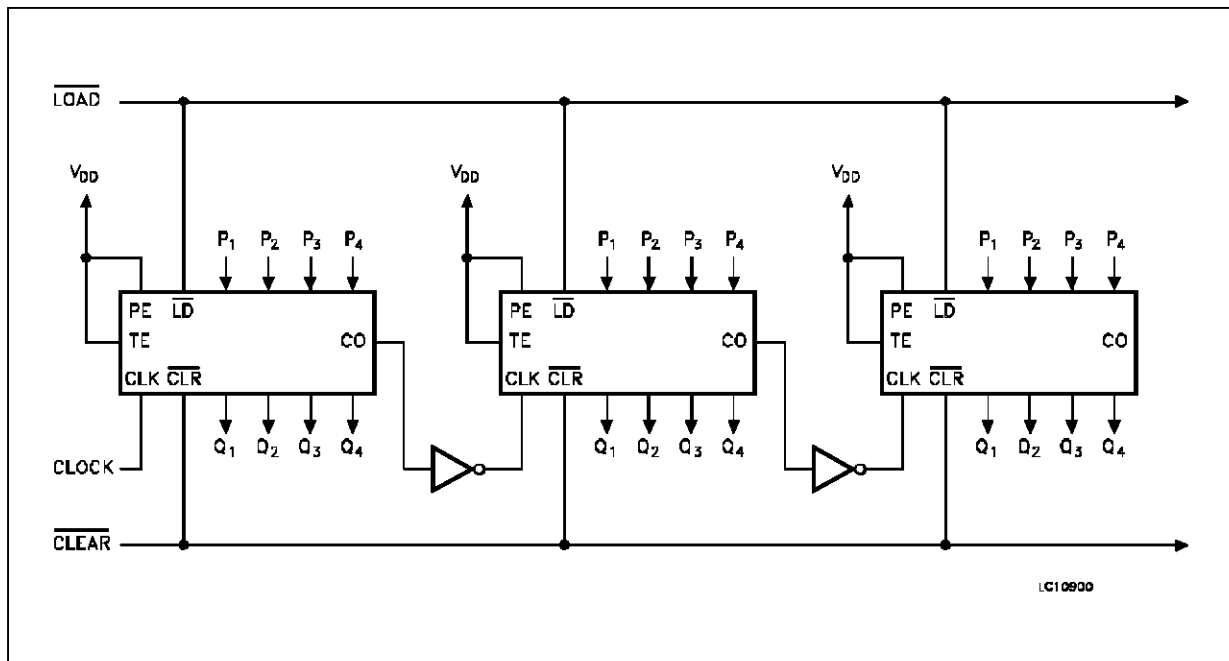




Cascading Counter Packages In The Parallel-Clocked Mode

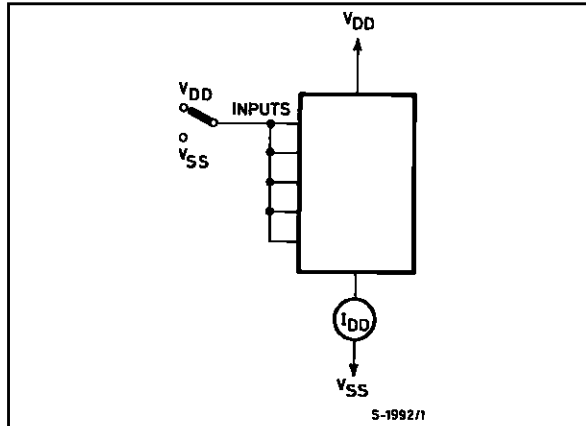


Cascading Counter Packages In The Ripple-Clocked Mode

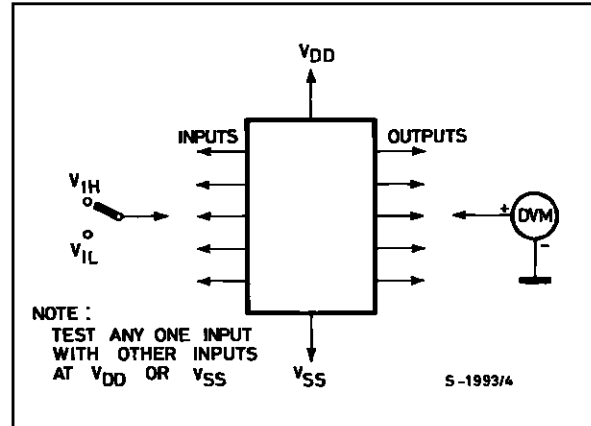


**TEST CIRCUIT**

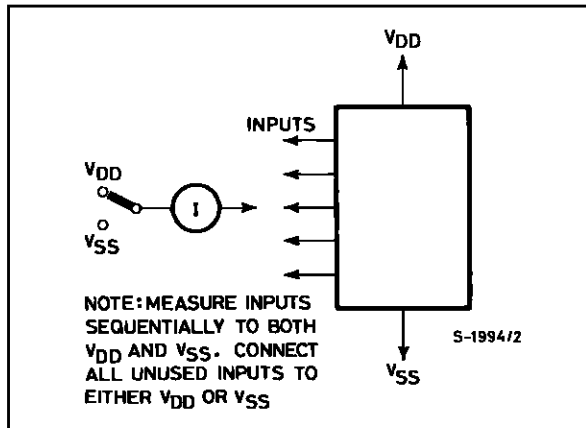
Quiescent Device Current



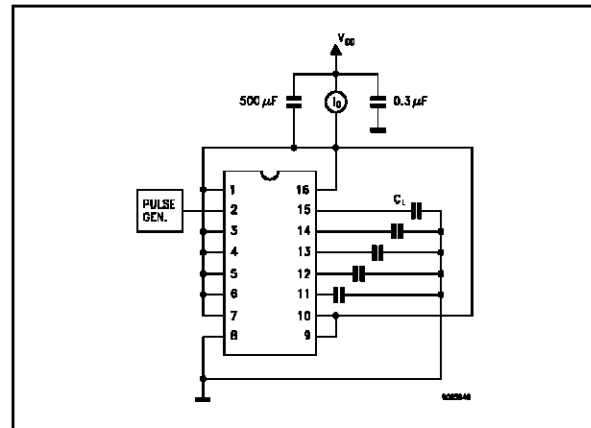
Input Voltage.



Input Leakage Current.



Dynamic Power Dissipation



**Plastic DIP16 (0.25) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



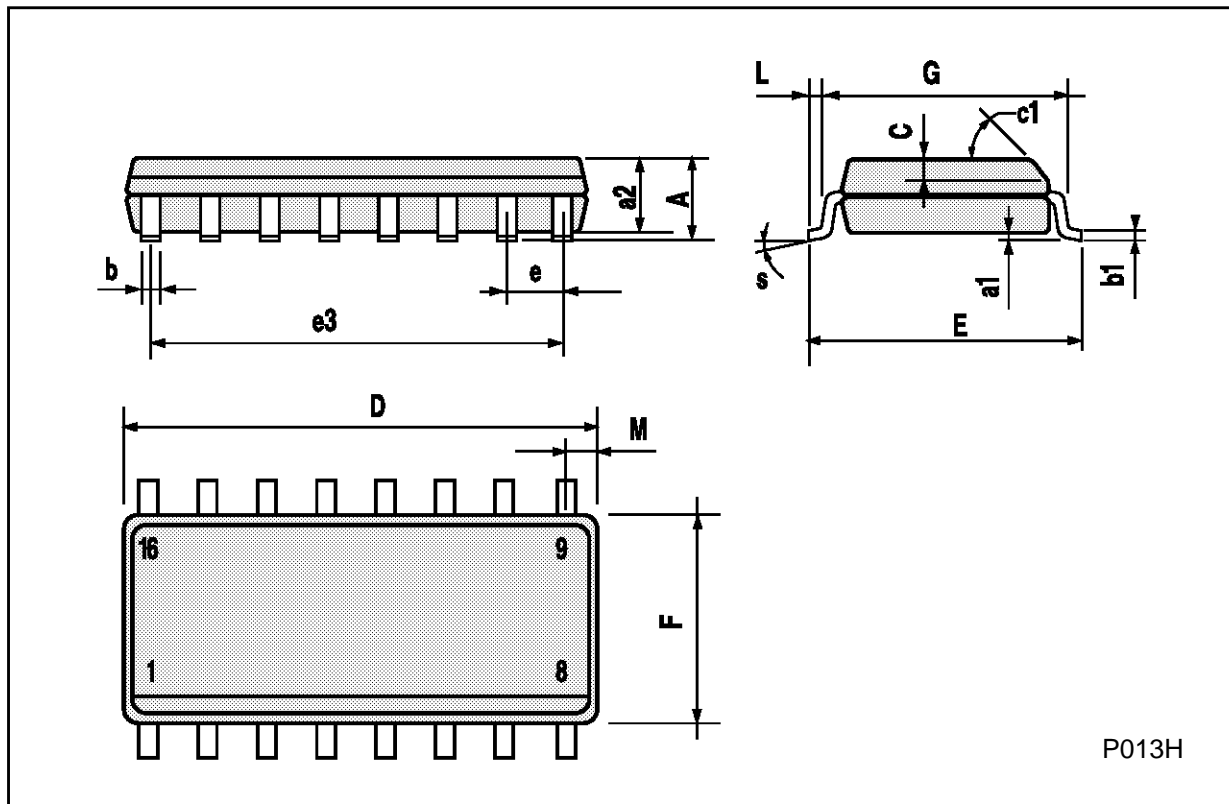
**Ceramic DIP16/1 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		17.78			0.700	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	0.51		1.27	0.020		0.050
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



**SO16 (Narrow) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



P013H

**PLCC20 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



Information furnished is believed to be accurate and reliable. However, SGS-THOMSON Microelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of SGS-THOMSON Microelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. SGS-THOMSON Microelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of SGS-THOMSON Microelectronics.

© 1994 SGS-THOMSON Microelectronics - All Rights Reserved

SGS-THOMSON Microelectronics GROUP OF COMPANIES

Australia - Brazil - France - Germany - Hong Kong - Italy - Japan - Korea - Malaysia - Malta - Morocco - The Netherlands -  
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A